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Real-Time Implementation of qZSC for MVDC to Microgrids Link

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Abstract. **Nowadays, power systems require new solutions to integrate renewable energies. In this paper, microgrids linked to MVDC are proposed through quasi-impedance-source converters to improve system reliability. Several prototypes are implemented using real-time platforms to analyze the system behavior, but the real-time implementation of the shoot-through state of the qZSC requires a very low time-step and sample time, which is not easy to achieve. The results obtained with these prototypes are included. Finally, a satisfactory solution is presented, implementing the power system in Typhoon HIL-402, the qZSC control in dSPACE MicroLabBox, and generating the gate signals in the FPGA included in the MicroLabBox platform.**

Key words. **Quasi-impedance-source converters, MVDC, microgrids, real-time implementation.**

1. Introduction

In the last decades, much attention has been paid to photovoltaic and wind energy sources, as they are considered some of the most viable solutions for microgrids (μGs) integration [1]. One of the main factors limiting renewable generation is the variability of voltage and current due to changing weather conditions [2]. Conventional conversion of DC-to-AC (or vice versa) usually requires two stages, while the impedance-source converters (ZSCs) make the same task using only one stage. ZSCs adapt the voltage using short circuits (switching the upper and lower switches of the same leg of a three-phase bridge) and pulse width modulation (PWM) in a single stage, thus improving system reliability [3], [4]. In contrast to the traditional converters, the ZSC short-circuit feature also improves the system reliability faults management. A topology derived from the ZSC is the quasi-impedance-source inverter (qZSC), which, compared with the ZSC, reduces stress at the source, lowers the nominal values of the inductors and the capacitors, and simplifies control strategies [5].

Fig. 1 shows several microgrids linked to an MVDC, illustrating that the qZSC can be used in the DG and the microgrid integration [6]-[9]. Due to the system's complexity, it can be implemented in several steps. The Hardware-in-the-Loop (HIL) platform is an interesting prototyping tool for real-time applications [10]. This paper only focuses on the real-time implementation of the MVDC to an AC microgrid subsystem using a HIL.

qZSC has a buck-boost function with reduced passive component ratings, which makes it suitable for photovoltaic systems as well as for the link to AC microgrids. The control of the buck-boost function involves high computational capabilities. The critical point in system prototyping is the real-time control of the qZSC as the shoot-through condition requires a low sample time.

Several solutions for converter rapid prototyping applied to MVDC can be implemented. The main advantages of environments such as dSPACE or Typhoon are fast prototyping due to high-level programming [11].

The minimum simulation step of the HIL-402 platform from Typhoon to represent IGBTs in qZSC applications is 1 μs, where the converter switching frequency is above 10 kHz [12]. However, the minimum sample time for the control allowed in HIL-402 is a multiple of the time-step (10 μs in our application), which is insufficient to control the shoot-through condition accurately. Something similar is true from the real-time processor of MicroLabBox platform from dSPACE, where the minimum time-step and sample time are 30 μs for this application.

The control of the shoot-through state requires speed-up computations which can be achieved with a FPGA (Field-Programmable Gate Array) [13]. This paper proposes the use of the FPGA contained in MicroLabBox to implement the qZSC control [14], [15]. If necessary, the clock time and the sample time in the FPGA platform could be diminished until 10 ns (such high speed is unnecessary in our application). As logic designers develop FPGA, they are traditionally programmed using hardware description languages such as VHDL and Verilog. These languages require the knowledge and training of a logic designer, take months to learn, and far longer to code efficiently. On the contrary, the environment of MicroLabBox uses a Xilinx Blockset to program the FPGA, which is a bit friendlier than previously mentioned low-level languages.

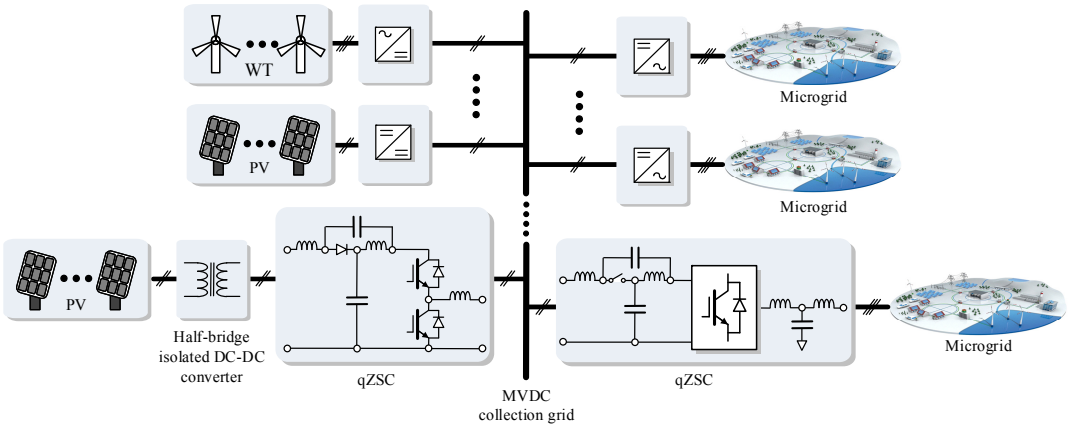

Fig. 1. Microgrids integration into the MVDC by means of qZCs.

This paper presents a real-time implementation of a qZSC-based power system. To outcome the successively arose problems, four implementations in HIL-402 and MicroLabBox are tested. The experimental results accuracy of the different prototypes has been validated by comparing the results with those obtained in MATLAB-Simulink running in asynchronous mode. Finally, conclusions are provided.

2. Analyzed System

A. System Description

As commented in the introduction, this paper deals with the link between the MVDC collection grid and a microgrid through a qZSC. The system is shown in Fig. 2. The MVDC grid is modeled as a constant voltage source in series with the equivalent inductance of the MVDC cables. The qZSC main components are two capacitors, C_1 and C_2, two inductors, L_1 and L_2, and a bidirectional switch, S, composed of a controlled electronic switch in antiparallel with a diode. In this paper, it has been considered that the power only flows from the MVDC link to the microgrid. In this unidirectional operation mode of the qZSC, only the diode is considered in switch S as the controlled electronic switch is inactive. The voltage across the capacitors is nearly constant during its operation, while the inductor currents depend on the delivered power. The front end of the qZSC is a three-phase inverter bridge that modulates a DC voltage, u_{DC}, to the microgrid. Such DC voltage is maintained constant by controlling the shoot-through state duration.

An LCL grid filter is connected between the qZSC and the primary winding of the power transformer, which links to the microgrid.

L_1, L_2, C_1 and C_2 are used to increase the input DC voltage by means of a shoot-through state caused when two IGBTs of the same leg are switched simultaneously. In this state, the diode is not conducting, and the input voltage source and the capacitors charge the inductors. During the non-shoot-through state, the diode is conducting, and the operation of the inverter is as usual. In this state, the DC input voltage and the inductors charge the capacitors and provide the power to the AC grid.

The I/O signals employed by the qZSC control are shown in Fig. 2. The DC voltage, u_{DC}, is regulated with the duty cycle, D. The duty cycle is the ratio between the intervals of the shoot- and non-shout-through states. The u_{DC} control loop uses the C_1 capacitor voltage, u_{C1}, to estimate of the actual u_{DC} and contains an internal loop for the L_2 inductance current, i_{L2}. The control of currents d and q manage the delivered active

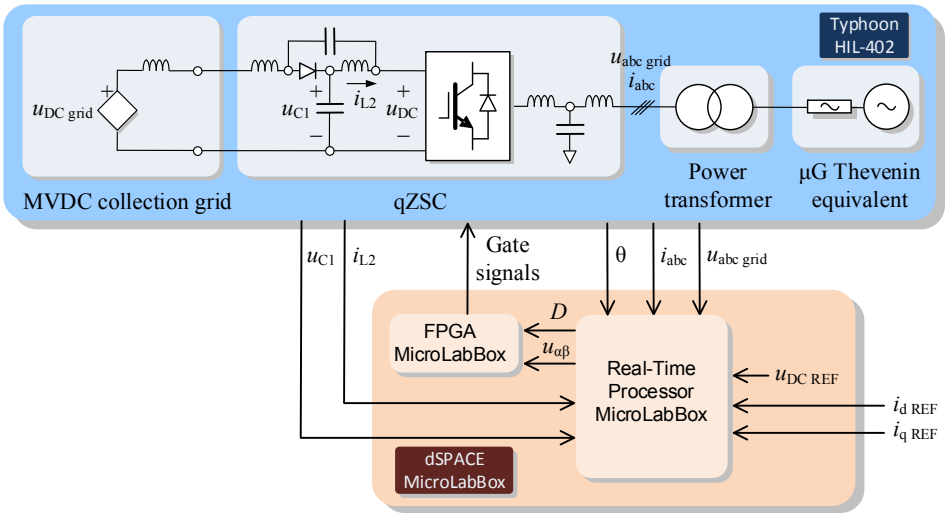

Fig. 2. Power system implemented in Typhoon and qZSC control implemented in dSPACE.

and reactive powers. Lastly, the implemented modulation for the IGBTs is the well-known Simple Boost Control (SBC).

The rated features of the real-time implemented power system are summarized in Table I on a per-unit (pu) basis. The MVDC is rated 6 kV, and their equivalent cable inductance is neglected in this case. The qZSC is rated at 1 MVA, and the delivered power from the DC link to the microgrid is a small fraction of the total microgrid loads consumption, around a seventh part. Lastly, the 3.6/0.4 kV power transformer adapts the qZSC output voltage to the microgrid voltage.

B. Time-Step and Sample Time Requirements

The time-step selection in real-time mode is critical to avoid multiple switching events (i.e., when the switch acts multiple times in one time-step). This is the case of the qZSC because the small duration of the shoot-through states makes the results very sensitive to chosen time-step and sample time.

In this paper, the analyzed system has been implemented in two different platforms, Typhoon HIL-402 and dSPACE-MicroLabBox, and the results of the different real-tiem implementations are validated by comparison with a Simulink model running in non-real-time mode. This Simulink model has also provided a boundary for the time-step, $t_s \leq 1$ µs, and for the sample time, $T_S \leq 1$ µs, to achieve accurate results.

3. HIL-402 Implementation

A. Main Features of Typhoon HIL-402

HIL-402 is a Hardware-in-the-Loop (HIL) environment from Typhoon, which is focused on real-time testing and verification of power converters in a wide range of applications. A relevant feature of HIL-402 is its low time-step, t_s, for power system implementation, which can be set from 0.5 to 20 µs. The control of the power system can also be modeled in HIL-402, but the sample time, T_S, must be a multiple of the time-step, being $T_S \geq 2 \cdot t_s$, as the control signals are generated in a slower dedicated processor. These ranges for t_s and T_S are adequate for most power converters and algorithms. However, they are invalid for the qZSC modeling in HIL-402, as the shoot-through state requires maximum values of $t_s = 1$ µs and $T_S = 1$ µs, and HIL-402 provides computing interval overrun if $t_s \leq 1$ µs. This will be shown in next Subsections.

TABLE I
SYSTEM PARAMETERS

MVDC GRID			
Rated voltage	6 kV		
qZSC			
Rated power	1 MVA		
$L_1 = L_2$	0.0205 pu	$L_{F1} = L_{F2}$	0.2052 pu
$C_1 = C_2$	0.1443 pu	C_F	0 pu
POWER TRANSFORMER			
Rated power	1.25 MVA		
Voltage ratio	3.6/0.4 kV		
Impedance	0.04 pu (on a 1.25 MVA base)		
MICROGRID			
Rated voltage	400 V		
Short-circuit power	6.8 MVA		
BASE VALUES			
Base power S_B	1 MVA		
Base AC voltage $U_{B\,(AC)}$	3.6 kV	Base AC current $I_{B\,(AC)}$	160.4 A
Base DC voltage $U_{B\,(DC)}$	6 kV	Base DC current $I_{B\,(DC)}$	166.7 A
Base pulsation ω_B	314.16 rad/s	Base inductance L_B	41.3 mH
Base impedance Z_B	12.96 Ω	Base capacitance C_B	246 µF

B. Switches Modeling in HIL-402

In HIL-402, the controlled (or uncontrolled) electronic switches can only be modeled as ideal; that is, with null/infinite resistance in conduction/blocking state. As the commutation of ideal switches will result in different circuit topologies, the platform pre-calculates all possible state-space matrices of the system (for all possible topologies due to all possible ideal switch states) before real-time operation. During the real-time operation, the different state-space matrices are picketed out.

However, this methodology easily overruns the computational capability of any platform as the memory space required to store the matrices rises exponentially with the number of switches. For example, consider a power system that contains 12 electronic switches. As the number of permutations is $2^{12} = 4096$, a total of 4096 different state-space matrices should be stored.

Typhoon has solved this handicap by truncating the modeled power system into different cores (e.g., the HIL-402 is composed of 4 cores) and limiting the number of blocks of electronic switches, given a different "weight" to each electronic switch block. The weight at any core is limited to 3 or 4 (depending on the configuration chosen by the user). For example, the weight of a discrete diode, an IGBT, or an IGBT with an antiparallel diode is 1. On the other hand, a single-phase diode bridge (with four ideal switches) or a single-phase inverter (with eight ideal switches, four IGBTs plus four antiparallel diodes) also have weights of 1, while a three-phase diode or inverter (with six or twelve ideal switches, respectively) have weights of 3. If the weight of the circuit is higher than 3 or 4, it must be partitioned between the different cores. The different partitions are executed on separate cores, and interact among them with a delay of t_s.

If the previous 12 electronic switches circuit example is split into two subcircuits (or two cores), the overall number of switch permutations per core is reduced to $2^6 = 64$. In this case, the overall number of matrices to be stored for both circuits is $2 \times 64 = 128$, which is significantly lower than 4096.

C. Prototype #1: All in HIL-402 with qZSC Modeled Using Individual Blocks

As the qZSC model contains 7 electronic switch blocks (the six switches of the inverter and the diode), its implementation in HIL-402 has a total weight of 7, and must be partitioned. This implementation suffers next two limitations: (a) the $t_s = 1$ µs delay among the two cores is invalid as it is in the same order of the shoot-through state duration, (b) the sample time of $T_S = 10$ µs is also excessive. The partition can be

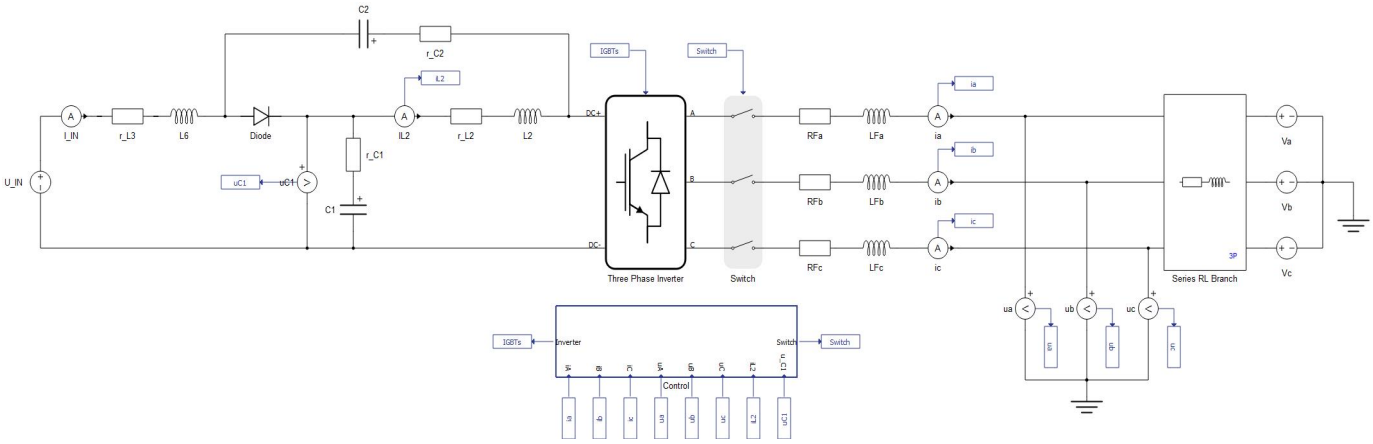

Fig. 3. Prototype #1 (all in HIL-402 with qZSC modeled using individual blocks): power system modeling.

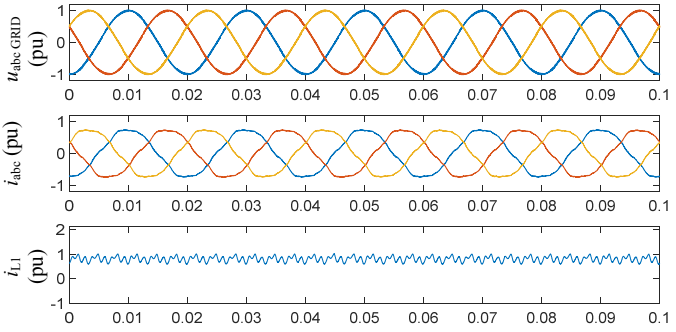

Fig. 4. Prototype #1: simulation results.

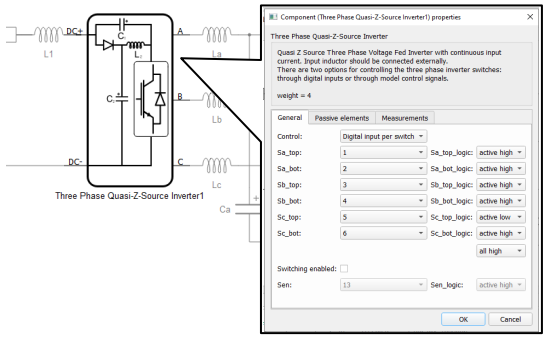

Fig. 5. Prototype #2 (all in HIL-402 using the customized qZSC): detail of the qZSC block and parameters.

avoided if the inverter is modeled with a specific block whose weight is 3, see Fig. 3. Despite the total weigh is reduced to 4 (inverter 3, diode 1), the minimum sample time is still T_S = 10 µs.

To illustrate the reliability of the different implementations, the AC grid voltages and currents, as well as the DC input current are chosen in this paper. The simulation results for prototype #1 are shown in Fig. 4.

D. Prototype #2: All in HIL-402 Using Customized qZSC Block

Fortunately, Typhoon team provides customized solutions. In our case, they have developed a qZSC implemented as a single block (including the three-phase inverter, and the diode and the components L_2, C_1 and C_2) with a weight of 3. The resulting electrical circuit is shown in Fig. 5, where the qZSC block parameters are detailed. With this solution, the minimum time-step to avoid computing overrun is 1 µs, while the minimum sample time is again 10 µs. The solution is not satisfactory due to the lack of sampling frequency to control the shoot-through condition. The simulation results for this prototype are not included as they are very similar to Fig. 4.

4. HIL-402 and MicroLabBox Implementation

A. Main Features of dSPACE MicroLabBox

dSPACE MicroLabBox is a real-time platform for laboratory prototyping, which combines high computation power with very low I/O latencies. The processor time-step, t_s, is a few microseconds. In higher requirements, as happens in the qZSC control of this paper, the platform also includes a user-programmable FPGA, where the control algorithms can be offloaded. The use of the FPGA will be described in Section 5.

The model is developed in MATLAB/Simulink, taking advantage of the Simulink libraries as well as specific libraries from dSPACE. Finally, the model is downloaded to the MicroLabBox target to be accessed in real-time with the software ControlDesk.

B. Prototype #3: Power System in HIL-402 and Control in MicroLabBox

As HIL-402 samples the external inputs at the same frequency as mades calculations, i.e., $t_s = T_{S\ (I/O)}$, a possible improve to the previous prototype is that HIL-402 samples the IGBT triggering from external inputs, instead of calculating them in the slower dedicated processor. By this reason, the qZSC control of prototype #3 has been implemented in the real-time processor of MicroLabBox, while the power system components remain in HIL-402, Fig. 6. As the minimum time-step in MicroLabBox to avoid overrun is 30 µs, the results remain inaccurate despite the time-step and the sample time in HIL-402 are $t_s = T_{S\ (I/O)}$ = 10 µs. This is illustrated in Fig. 7.

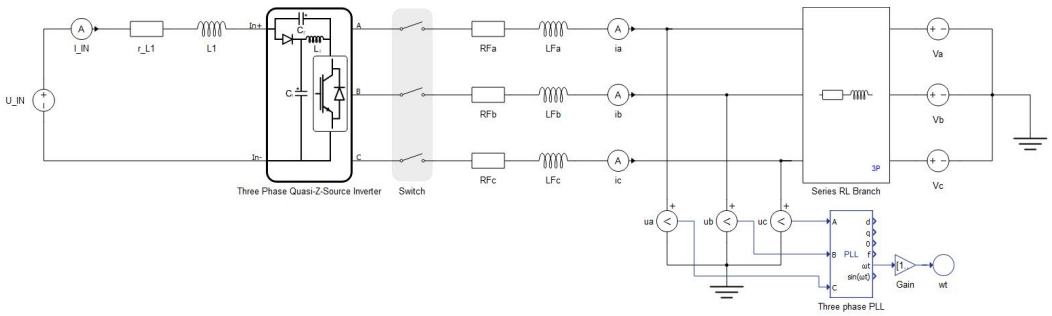

Fig. 6. Prototype #3 (power system in HIL-402 and qZSC control in MicroLabBox): power system modeling.

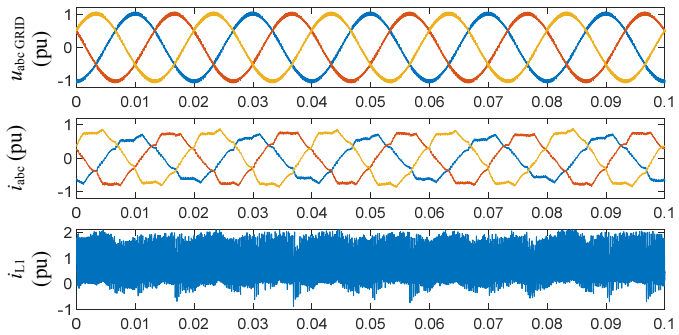

Fig. 7. Prototype #3: simulation results.

5. HIL-402, MicroLabBox, and FPGA-MicroLabBox Implementation

A. Main Features of FPGA-MicroLabBox

As commented previously, MicroLabBox contains the user-programmable FPGA Xilinx Kintex-7 XC7K325T, which lets run extremely fast control loops, as required by the qZSC. The FPGA is programmed via the RTI FPGA Programming Blockset of Xilinx, inside the Simulink environment. The minimum time-step which can be achieved with this FPGA is around several nanoseconds (clock frequency is 320 MHz).

B. Prototype #4: Power System in HIL-402, Control in MicroLabBox and Gate Signals in FPGA-MicroLabBox

As shown in Fig. 2, the converter gate signals in this prototype are generated by the FPGA of MicroLabBox, while the qZSC control remains implemented in the real-time processor of MicroLabBox and the power system in HIL-402 (identical to that shown in Fig. 6a). The time-steps are 10 ns in FPGA-MicroLabBox, 20 µs in MicroLabBox, and 1 µs in HIL-402. Fig. 8a shows the real-time results, which are reasonably accurate when compared to the Fig. 8b results of the Simulink variable step model (see Subsection B) running in non-real-time mode. The differences are not significant; the error is less than 7%, although a small oscillation is observed on the DC input.

6. Lab Setup

The layout of Fig. 9 has been carried out to operate the real-time prototypes in remote mode as, e.g., during pandemic situations. In the research laboratory, the I/O channels of the platforms HIL-402 and MicroLabBox are connected to each other. The required software is installed on the server, which allows the remote operation of both platforms.

7. Conclusions

Microgrids integration in MVDC can be achieved through qZSCs to improve the power system reliability. In the analysis of qZSC integration, four prototypes were implemented using real-time platforms. The real-time implementation of the shoot-through state of the qZSC requires a maximum time-step of t_s = 1 µs and a maximum sample time of T_S = 1 µs.

Despite the HIL-402 platform from Typhoon is friendly and valuable, and it is focused on real-time simulation of power systems, the qZSC strict requirements are not fulfilled as time-step can be set to t_s = 1 µs but the minimum sample time is T_S = 10 µs.

As HIL-402 samples external signals at the frequency of the time-step, the control of the qZSC has been built in the real-time processor of the MicroLabBox platform from dSPACE, while the power system components remain implemented in HIL-402. The results are not satisfactory either, as the minimum time-step in MicroLabBox to avoid an overrun error is t_s = 30 µs.

Finally, a satisfactory solution has been found by implementing the gate signals generation in the FPGA included in the MicroLabBox platform but maintaining the power system in HIL-402 and the qZSC control in MicroLabBox. The time-steps are 10 ns in the FPGA of MicroLabBox, 20 µs in the processor of MicroLabBox, and 1 µs in HIL-402. As HIL-402 samples the IGBT signals from external inputs, the sample time is also $T_{S\ (I/O)}$ = 1 µs.

This work has highlighted the difficulty of implementing the shoot-through state of the qZSC and describes a satisfactory solution to achieve it.

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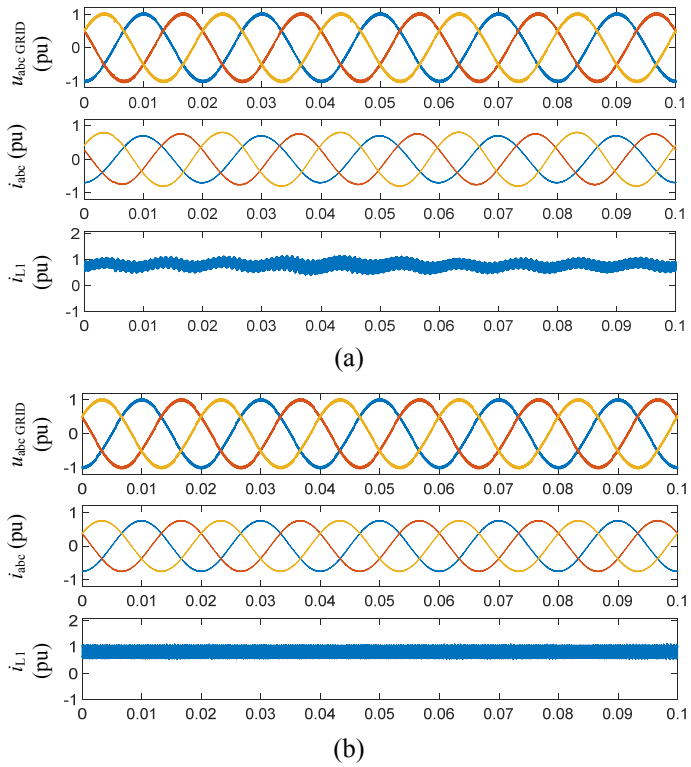

Fig. 8. Comparison of Prototype #4 with the Simulink model (running in non-real-time mode).

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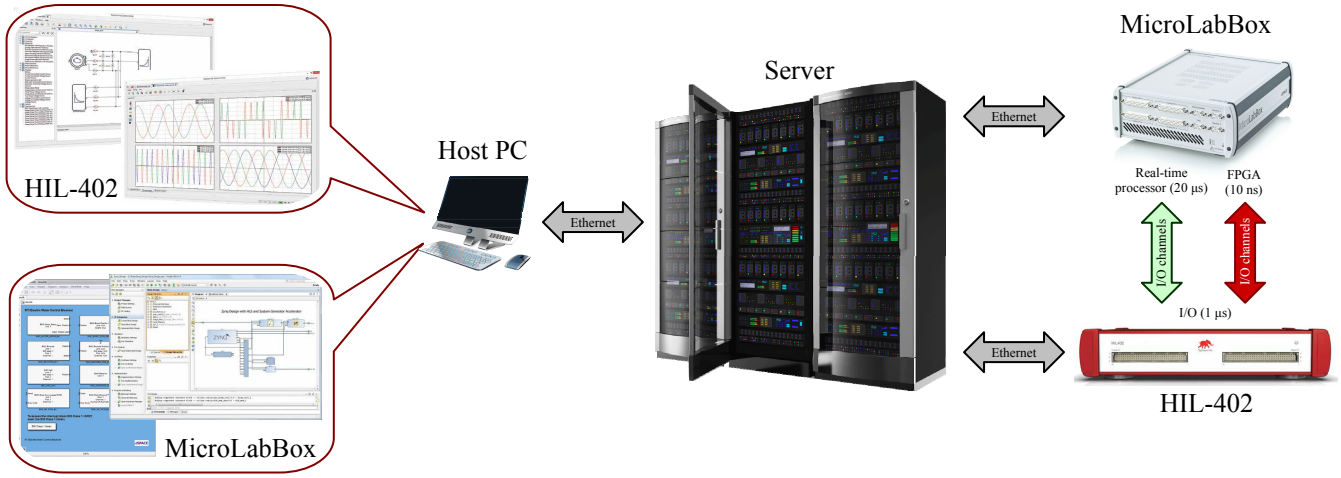

Fig. 9. Layout of prototype #4.