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# Multilevel inverter with active clamping diodes for energy efficiency improvement

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**Abstract.** Multilevel inverters can replace commonly used two-level inverters for three-phase electrical drives. In this low-voltage range new wide-bandgap power switches (SiC MOSFET, GaN FET) are available. In the four-, five- and seven-level inverters, the majority of the power losses are caused by the threshold voltage of the clamping diodes. The new idea is the replacement of the clamping diodes by active switches, since they only have low on-resistance in the forward direction. In this case freewheeling paths of the clamping diodes would have to be actively switched. However, the control signals for the clamping switches can be generated by logic operations from the control signals for the main switches. The use of active clamping switches has significant potential to reduce semiconductor losses, but requires the development of wide-bandgap power semiconductors with reverse blocking capability. At nominal motor operation point of the 5.5 kW induction motor a loss reduction of 56 % between active clamping switches and clamping diodes is possible. With a higher number of inverter levels, the size of the motor filter can be reduced by about 70 % and also the losses can be reduced by 73 %.

**Key words.** Multilevel inverter, Active clamping diode, Wide-bandgap semiconductor, Energy efficiency.

## 1. Introduction

The application of multilevel inverters for three-phase induction motor drives is a new idea. This inverter topology can have three, four, five or even seven levels. In this voltage range new wide-bandgap power switches (SiC MOSFETs, GaN FETs) are available. Multilevel topologies could outperform the classical two-level inverter with fewer conduction and switching losses and increase the energy efficiency of the drive system. Further advantages of multilevel topologies are: reduction of voltage transients at the motor windings especially with long shielded motor cables, reduced stresses on the power switches, lower harmonic distortion content in the output voltage and current, smaller output filter and inverter size. Multilevel inverters are predestined for e-mobility applications, because its focus is high power density, high efficiency and large battery range. Although the multilevel inverter is actually used for high power, new wide-bandgap power switches enable it to be used for small powers of just a few kilowatts. Although the number of power semiconductors is greater, the effort of cooling them (heat sink, fan) is reduced. Therefore the inverter size can be reduced.

A large amount of conduction losses is caused by the clamping diodes inside the multilevel inverter. This results from the forward voltage drop. The idea is the replacement of the clamping diodes by active switches (SiC MOSFETs, GaN FETs), because they only have small on-resistance in forward direction.

## 2. Multilevel Inverter with Active Clamping Diodes

Fig. 1 and 2 show the bridge legs of the four-level, five-level and seven-level inverter with active clamping switches (T7 to T22). The active clamping switches are SiC MOSFETs or GaN FETs with very small on-resistance.

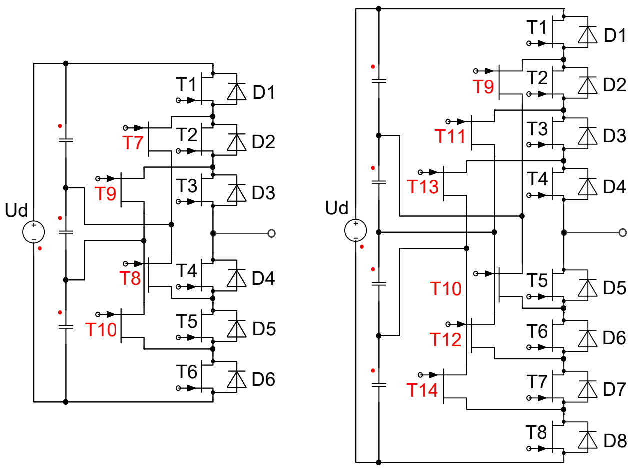


Fig. 1. Bridge legs of the four-level and five-level inverter with active clamping switches (red: T7 to T14).

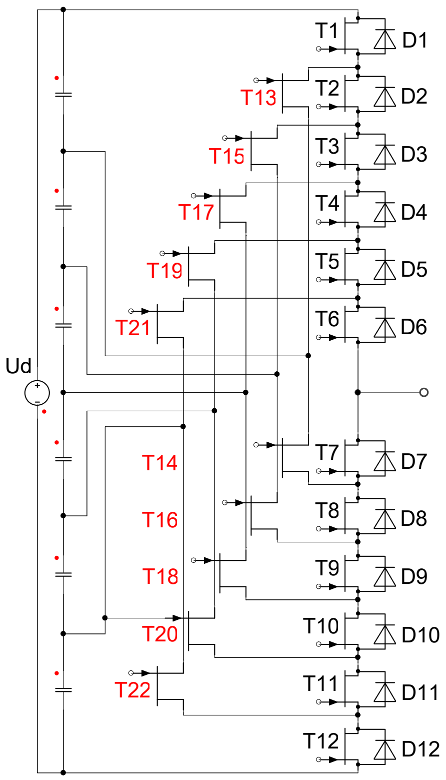


Fig. 2. Bridge leg of the seven-level inverter with active clamping switches (red: T13 to T22).

Fig. 3 compares the forward voltage drop of clamping diode and active clamping switch. At rated current ($I_F = 20$ A) the forward voltage can be reduced from 0.83 to 0.2 V, this means a reduction of conduction losses by 76 %.

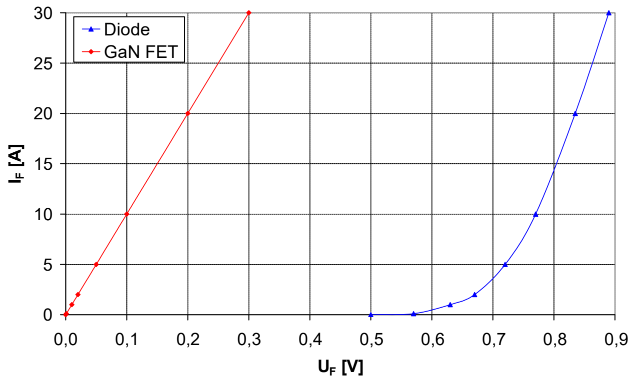


Fig. 3. Forward characteristics of clamping diode SBR40300CT and clamping switch 2xEPC2033 at 25°C junction temperature.

### A. Control Signals for Active Clamping Switches

While clamping diodes switch on automatically, active clamping switches need a control signal for the freewheeling paths. This requires knowledge of the free running times.

Fig. 4 and 5 show the currents through the clamping diodes and the control signals for the main switches of the three-level inverter (Fig. 4) and the four-level inverter (Fig. 5). A connection can be seen here, so that the control signals for the active clamping switches can be generated from the control signals for the main switches.

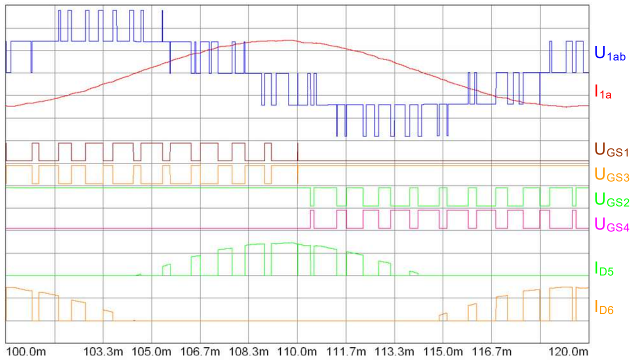


Fig. 4. Control signals (main switches) and clamping diode currents (D5, D6) of three-level inverter.

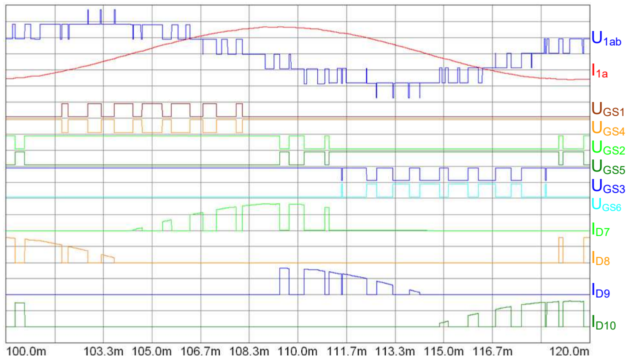


Fig. 5. Control signals (main switches) and clamping diode currents (D7, D8, D9, D10) of four-level inverter.

There is a relationship between the control signals for the main switches and the currents through the clamping diodes. This means that the control signals for these active clamping switches can be generated from the control signals for the main switches by means of a corresponding AND logic operation (Tab. I).

Table I. – Control Signals for Active Clamping Switches

| | Active clamping Switches | Control signals |
|---|---|---|
| Three-level | S5 and S6 | $U_{GS2} \bullet U_{GS3}$ |
| Four-level | S7 and S8<br>S9 and S10 | $U_{GS2} \bullet U_{GS4}$<br>$U_{GS3} \bullet U_{GS5}$ |
| Five-level | S9 and S10<br>S11 and S12<br>S13 and S14 | $U_{GS2} \bullet U_{GS5}$<br>$U_{GS3} \bullet U_{GS6}$<br>$U_{GS4} \bullet U_{GS7}$ |
| Seven-level | S13 and S14<br>S15 and S16<br>S17 and S18<br>S19 and S20<br>S21 and S22 | $U_{GS2} \bullet U_{GS7}$<br>$U_{GS3} \bullet U_{GS8}$<br>$U_{GS4} \bullet U_{GS9}$<br>$U_{GS5} \bullet U_{GS10}$<br>$U_{GS6} \bullet U_{GS11}$ |

### B. Conduction and Switching Losses

For estimation of conduction and switching losses ($P_{VL} + P_{VS}$) a simulation model was developed that can be integrated into the model of the complete induction motor drive system. To simulate the conduction losses, the power semiconductors (SiC MOSFETs, GaN FETs, diodes) are provided with their respective static characteristics $I_C = f(U_{CE})$. The mean value of the power over a period of the motor frequency is formed from the time curves of voltage and current at each power semiconductor; this corresponds to the conduction losses. Dynamic models of the power semiconductors are usually required to simulate the switching losses. These are insufficiently available, complex to parameterize and require very small simulation time steps (less than 1 ns). The new idea is to simulate the switching losses by means of a static model. This allows a much larger simulation time step (100 to 500 ns) to be used. In addition, the required parameters are the usual data sheet information from power semiconductor manufacturers. The simulation of conduction and switching losses was done for a 5.5 kW high-efficiency induction motor with the best 100 V to 600 V power electronic switches (SiC MOSFETs, GaN FETs) on the market (Tab. II).

Table II. – Power Switches for Multilevel Inverters

| | | | | |
|---|---|---|---|---|
| Three -level | SiC MOSFET | C3M00 60065J | 650 V 60 mΩ | 3L-SiC |
| | GaN FET | GS66508B | 650 V 50 mΩ | 3L-GaN |
| Four-level | GaN FET | 2 x EPC2034 | 2x 200 V 10 mΩ | 4L-GaN |
| Five-level | GaN FET | 2 x EPC2033 | 2x 150 V 7 mΩ | 5L-GaN |
| Seven -level | GaN FET | 2 x EPC2053 | 2x 100 V 3.8 mΩ | 7L-GaN |

## 3. Energy Efficiency Improvement

Fig. 6 shows the potential for reducing semiconductor losses for the 5.5 kW induction motor as function of the motor power (0 to 125 %) when using active clamping switches instead of clamping diodes. The precondition for this is the implementation of reverse blocking capability in the clamping switches. The conduction and switching losses for the three-level, four-level, five-level and seven-level inverter with active clamping switches (3L-GaN CD, 4L-GaN CD, 5L-GaN CD, 7L-GaN CD) are compared with those with clamping diodes (3L-GaN, 4L-GaN, 5L-GaN, 7L-GaN) at 10 kHz switching frequency.

Overall, there is significant potential for loss reduction for all inverter levels. However, the four-level inverter (4L-GaN CD) shows the greatest potential, since the currently available clamping diodes are particularly unfavorable. The seven-level inverter (7L-GaN CD) has greater potential for loss reduction compared to the five-level inverter (5L-GaN CD) and would generate the lowest losses of all analyzed multi-level inverters using this new circuit topology. At nominal motor operation point a loss reduction of 56 % between active clamping switches and clamping diodes is possible.

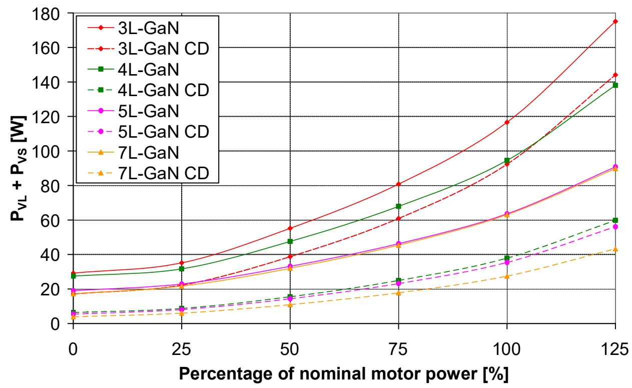


Fig. 6. Conduction and switching losses of the three-level, four-level, five-level and seven-level inverter with active clamping switches (CD) as function of motor power at 25 °C junction temperature.

## 4. Inverter Output Filter

### *C. Analyses of Inverter Output Voltage*

Fig. 7 and 8 contain the output voltages of the two-level and seven-level inverter at 10 kHz switching frequency. With a higher number of levels, the output voltage approaches the sinusoidal shape and the harmonic spectrum decreases. This visual impression is quantified by the total harmonic distortion content ($THD_u$) according to equation (1), the indices OS denoting the harmonic component and GS denoting the fundamental component. The harmonic content indicates the quality of the inverter output voltage. The smaller the $THD_u$, the more sinusoidal is the voltage. The harmonic content depends on the number of inverter levels and the inverter modulation index (m) (Fig. 9). The higher the number of inverter levels, the lower the harmonic content. For example, with m = 0.67, the harmonic content is reduced by 84 % for seven levels compared to two levels. The smaller the inverter modulation index, the higher the harmonic content. However, the harmonic content is not dependent on the switching frequency and not on the motor operation point.

$$THD_U = \frac{\tilde{U}_{WRab\,OS}}{\tilde{U}_{WRab\,GS}} = \frac{\sqrt{\tilde{U}^2_{WRab} - \tilde{U}^2_{WRab\,GS}}}{\tilde{U}_{WRab\,GS}} \qquad (1)$$

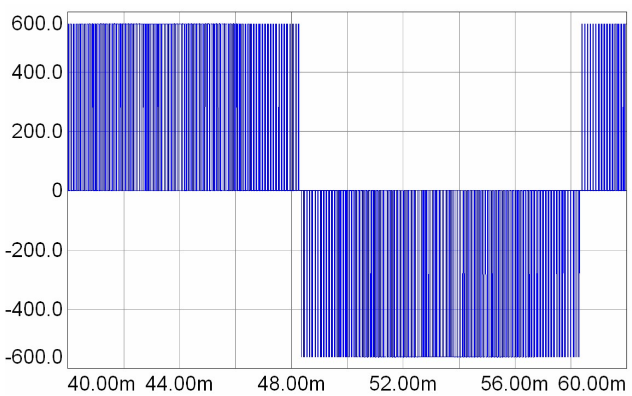


Fig. 7. Output voltage of the two-level inverter at 10 kHz switching frequency (m = 0,97).

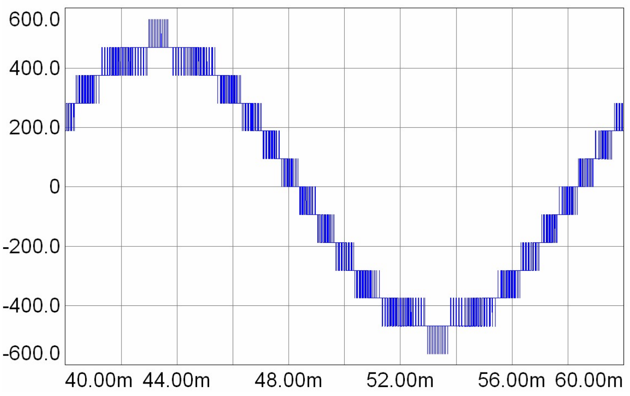


Fig. 8. Output voltage of the seven-level inverter at 10 kHz switching frequency (m = 0,97).

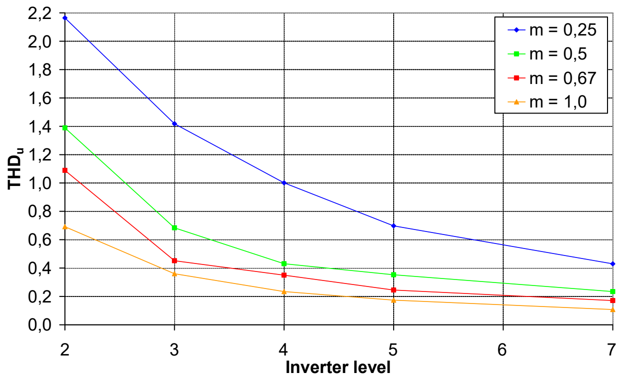


Fig. 9. Total harmonic distortion content of the inverter output voltage for different modulation index as function of inverter levels.

*D. Filter Design and Losses*

Fig. 10 shows a three-phase inverter output filter (motor filter) that is installed on the inverter output terminals. It consists of the three-phase choke with an iron core and three AC capacitors. The three-phase choke covers the majority of the size, weight and losses. The associated electrical circuit (Fig. 11) consists of the inductors $L_F$ and the capacitors $C_{FY}$, which form a 2nd order low-pass filter for the inverter output voltage. The natural frequency and damping result from equation (2).

$$f_0 = \frac{1}{2\pi\sqrt{L_F \cdot C_{FY}}} \quad ; \quad d = \frac{R_F}{2}\sqrt{\frac{C_{FY}}{L_F}} \qquad (2)$$

Fig. 10. Three-phase inverter output filter (motor filter).

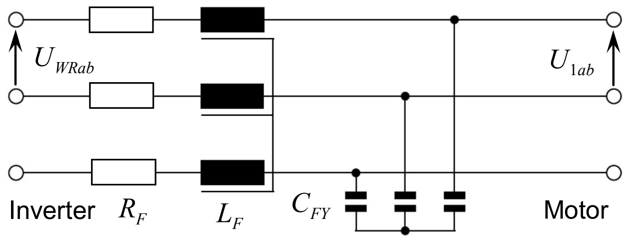


Fig. 11. Electric circuit of the three-phase motor filter.

The frequency-dependent attenuation (frequency response) between the inverter output voltage ($U_{WRab}$) and the motor voltage ($U_{1ab}$) is shown in Fig. 12 for different inverter levels. The fundamental component of the inverter output voltage ($f_1 \leq 100$ Hz) passes through the filter without amplification or attenuation. At the switching frequency of 10000 Hz (10 kHz), the required damping is marked. The higher the number of levels, the lower the harmonic content of the inverter output voltage, so that the required attenuation is lower. As a result, the natural frequency of the filter $f_0$ can be higher, which reduces the inductances and capacitors and the size of the filter.

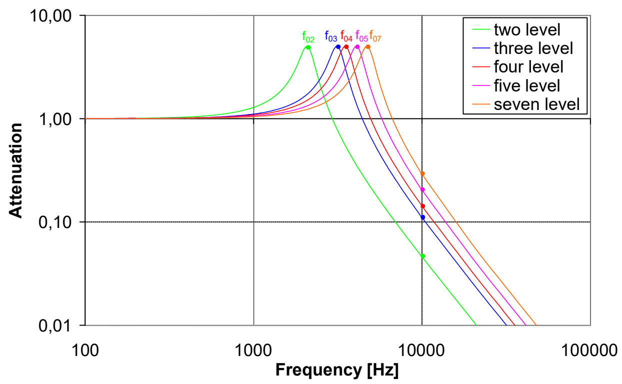


Fig. 12. Amplitude-frequency characteristic of the motor filter for different inverter levels.

The required natural frequency of the filter depends on the number of levels and the switching frequency and is calculated according to equation (3). The harmonic content permitted in the motor voltage is usually $THD_{u\,ref} = 0.1$ (10 %).

$$f_0 = \frac{f_p}{\sqrt{1-2d^2+\sqrt{\left(1-2d^2\right)^2-1+\frac{1}{|G|^2}}}} \quad ; \quad |G| = \frac{THD_{u\,ref}}{THD_u} \tag{3}$$

For a motor filter for the 5.5 kW induction motor, Tab. III contains the values of the inductances $L_F$ and capacitors $C_{FY}$ for various inverter levels and switching frequencies.

Table III. – Filter Design for Different Levels and Switching Frequencies for 5.5 kW induction motor

| level | $f_p$ [Hz] | $f_0$ [Hz] | $L_F$ [mH] | $C_{FY}$ [µF] |
|---|---|---|---|---|
| two | 5000 | 904 | 3.1 | 10 |
| two | 10000 | 2095 | 1.34 | 4.31 |
| three | 10000 | 3156 | 0.89 | 2.86 |
| four | 10000 | 3536 | 0.79 | 2.56 |
| five | 10000 | 4117 | 0.68 | 2.20 |
| five | 20000 | 8234 | 0.34 | 1.10 |
| five | 30000 | 12351 | 0.23 | 0.73 |
| seven | 10000 | 4757 | 0.59 | 1.90 |
| seven | 20000 | 9513 | 0.29 | 0.95 |

The dimensioning of the three-phase choke was carried out with appropriate special software. Fig. 13 shows the calculated volume and losses. The three-phase choke amounts nearly 80% of the total volume and losses of the motor filter. By increasing the number of levels from two to five and the switching frequency from 5 kHz to 20 kHz, the volume and weight can be reduced by 70 %. A further increase in the number of levels and switching frequency does not result in any further reduction in volume and weight. The increase of levels and switching frequency leads to a continuous reduction of filter losses. By increasing the number of levels to seven and the switching frequency to 20 kHz, the losses can be reduced by 73 %. A further increase in the switching frequency results in a slight increase in the losses.

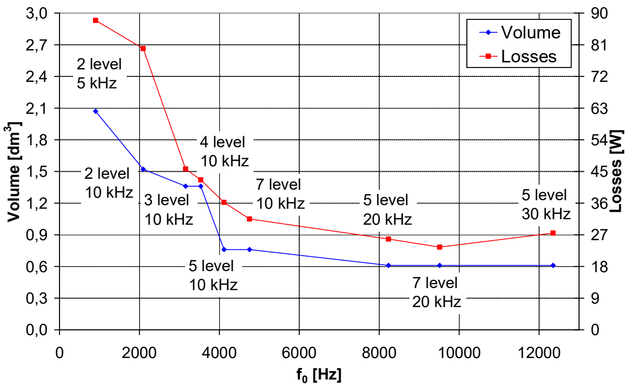


Fig. 13. Volume and losses of the three-phase choke for various inverter levels and switching frequencies for 5.5 kW induction motor.

## 5. Conclusion

Low-voltage wide-bandgap power semiconductors (SiC MOSFETs, GaN FETs) are now available for multilevel inverters with 560 to 750 V DC link voltages. In the four-, five- and seven-level inverters, the majority of the losses are caused by the threshold voltage of the clamping diodes. This resulted in the idea of replacing the clamping diodes with active switches (SiC MOSFETs, GaN FETs), since only the low on-resistance acts in the forward direction. In this case, freewheeling paths made possible by the clamping diodes would have to be actively switched. For this purpose, the control signals for the clamping switches can be generated by logic operations from the control signals for the main switches. The use of active clamping switches has significant potential to reduce semiconductor losses, but requires the development of wide-bandgap power semiconductors with reverse blocking capability. Moreover, lower inverter power losses would lead to a reduction of cooling effort and to smaller inverter size.

With a higher number of inverter levels and higher inverter switching frequencies, the size of the motor filter can be reduced. For the investigated 5.5 kW induction motor, the seven-level inverter with 20 kHz switching frequency is an optimum topology. . Compared to the state of the art (two-level with switching frequency), volume and weight of the motor filter can be reduced by 70 %. The losses can be reduced by 73 %.

The application of multilevel inverters can make a contribution to efficiency improvement in electrical drives for new applications as e-mobility or renewable energy conversion.

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