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Performance Evaluation of Grid Connected T-Type Multilevel Inverters

Kevin ACADINE[1], Augustin MPANDA MABWE[2] and Ahmed EL HAJJAJI[1]
[1]Laboratoire MIS, UPJV
33 rue Saint Leu, 80039 Amiens, France
e-mail : kevin.acadine@unilasalle.fr, ahmed.hajjaji@u-picardie.fr
[2]SYMADE, UniLaSalle Amiens
14 Quai de la Somme, 80082 Amiens, France
e-mail : augustin.mpanda@unilasalle.fr

Abstract. This paper deals with performance of three and five level grid-connected T-type inverters. T-Type structure requires fewer power devices than Neutral-Point-Clamped and Flying-Capacitor inverters for the same power level.
First, mathematical model of grid connected T-Type inverters is demonstrated. The PI controller is used to control the d-axis and q-axis currents, respectively. The sine Pulse Width Modulation (PWM) technique is used to control the MOSFET switches. The simulation of the complete system has been performed on MATLAB/Simulink.

Key words. Multilevel inverters, T-type five level, PI controller, closed loop.

1. Introduction

The increase in global energy demand, the dependence on fossil fuels, the depletion of these fuels and the gradual increase in their prices lead to massive economic and intellectual investment in the development of new technologies for sustainable energy resources [2]. The stakes are therefore energy, economic and environmental. The investment in renewable energy sources is today the best alternative to manage the demands of the energy market. In this respect, Renewable Energy Sources (RES) have increased in recent decades throughout the world. The energy produced by these sources is exploited by power converters, DC/AC or AC/AC type, especially for grid injection and energy storage.

Traditionally, grid tie RES is done through classical two-level inverters such as the H-bridge structure, the most used. However, this structure is physically limited by its power components, at medium and high powers [1]. Research to overcome these limiting factors has led to new multilevel converter topologies. The interest of these structures is to have a flexible and adaptable to needs injection of energy in the network and to obtain sinusoidal output voltages. Cost, bulkiness, voltage and current THD and energy efficiency are then optimized: making the multilevel converter a substantial solution [2].

The first multilevel inverter version is the Neutral-Point-Clamped inverter (NPC), which appeared in 1981. Flying-Capacitor (FC) and Cascaded H-Bridge (CHB) inverter topologies appeared a few years later [3]. These topologies have become common [1] [2] [4] [5]. In recent years, we have seen the emergence of hybrid multilevel topologies aimed at optimizing the number of semiconductors. For example, five level (5L) ANPC (Active-Neutral-Point-Clamped) inverter. The T-Type 5L structure, studied in this article, is the combination of two converters [6].

Control and optimization methods, modulation techniques and capacitor voltages balancing, are part of these complex issues of the multilevel inverters. NPC, CHB, FC, Type-T, ANPC structures are grid connected multilevel inverters for renewable energy integration. Each have their own advantages and disadvantages [1] [7].

Table I. – Comparison of multilevel inverter topologies

	NPC	FC	T-Type	CHB
Switches per phase	2 (n-1)	2 (n-1)	2 (n-1)	2 (n-1)
Flying Diodes	(n-1) (n-2)	0	0	0
Flying Capacitors	0	(n-1) (n-2)	0	0
DC Capacitors	(n-1)	(n-1)	(n-1)	(n-1) / 2
Modularity	Low	High	Low	High

In this paper, the performance evaluation of two grid-connected T-Type inverters, 3L and 5L, is carried out. The DC bus voltage is considered perfect. We first present the dynamic behaviour of this association in the form of mathematical equations. A PI controller is used to control the d-axis and q-axis currents respectively. The sine Pulse Width Modulation (PWM) technique is used to control the MOSFET switches. The simulation of the complete system has been performed on MATLAB/Simulink and is presented at the end.

2. T-Type inverter structures

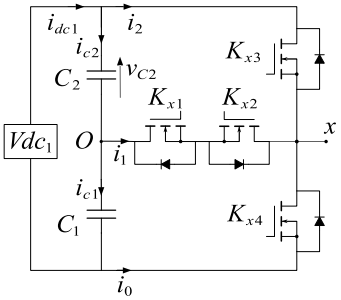


Fig. 1. T-Type 3L structure

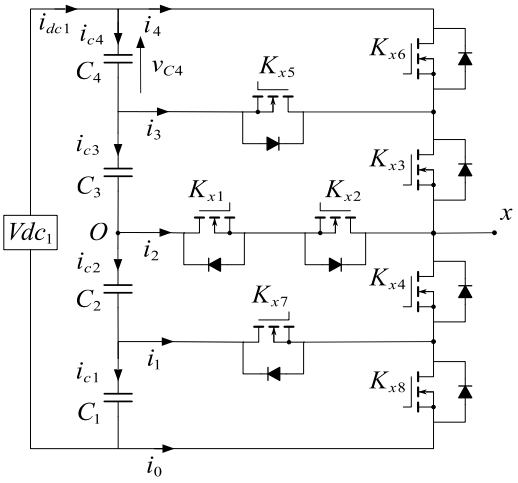


Fig. 2. T-Type 5L structure

Fig. 1 and 2 show the power electronics circuits of 3L and 5L T-Type inverters (T3 and T5) respectively. T-Type inverter structures is configured with (*n-1*) equal DC link capacitors C_k, 2*(n-1)* power switches K_x per phase *x*. Where *n* the inverter level, *x* summarizing phase *a*, *b* and *c*, *and k=1, …, (n-1)*.

We denote S_{wx} as possible switching states per phase. Then, for a T3, three possible switching states $S_{x,2}$, $S_{x,1}$, et $S_{x,0}$. For a T5, five possible switching states per phase $S_{x,4}$, $S_{x,3}$, $S_{x,2}$, $S_{x,1}$ and $S_{x,0}$. As a matter of principle:

$$\sum_{j=0}^{n-1} S_{x,j} = 1 \qquad (1)$$

Table II. – 3L T-Type switching states

Output voltages	K_{x4}	K_{x2}	K_{x1}	K_{x3}	$S_{x,j}$
V_{dc1} / 2	0	0	1	1	$S_{x,2}$
0	0	1	1	0	$S_{x,1}$
-V_{dc1} / 2	1	1	0	0	$S_{x,0}$

Table III. - 5L T-Type switching states

Output voltages	K_{x8}	K_{x4}	K_{x2}	K_{x5}	K_{x7}	K_{x1}	K_{x3}	K_{x6}	$S_{x,j}$
V_{dc1} / 2	0	0	0	0	1	1	1	1	$S_{x,4}$
V_{dc1} / 4	0	0	0	1	1	1	1	0	$S_{x,3}$
0	0	0	1	1	1	1	0	0	$S_{x,2}$
-V_{dc1} / 4	0	1	1	1	1	0	0	0	$S_{x,1}$
-V_{dc1} / 2	1	1	1	1	0	0	0	0	$S_{x,0}$

V_{dc1} is a perfect DC voltage source, $v_{g,x}$ are grid phase-to-neutral voltages and $i_{i,x}$ are inverter output currents.

The switching states of both 3L and 5L inverters are summarized in Table II and Table III respectively.

3. Modelling of T-Type inverter

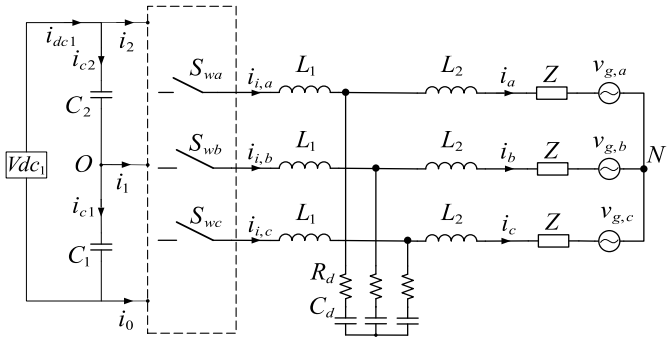


Fig. 3. Synthetized T-Type 3L structure

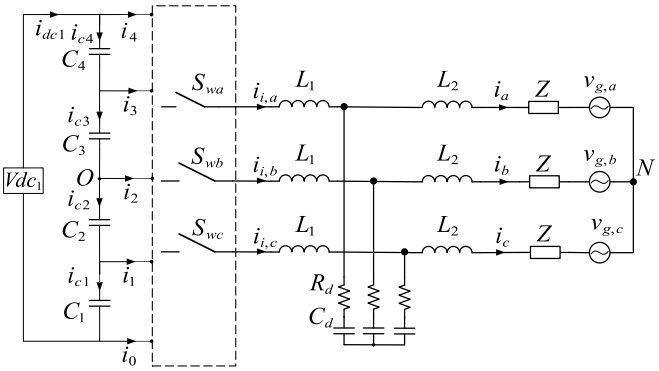


Fig. 4. Synthetized T-Type 5L structure

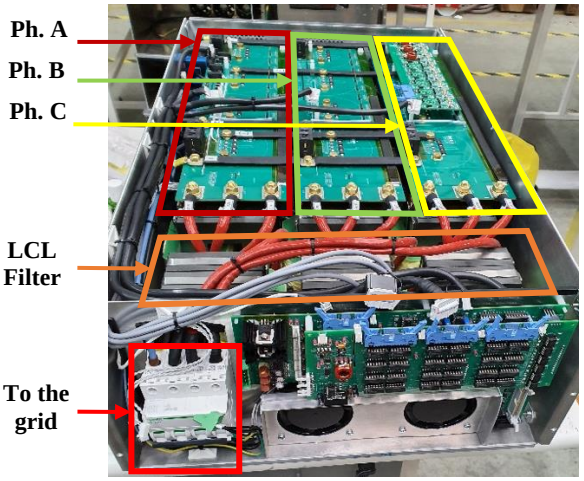


Fig. 5. Realization of T-Type 5L inverter structure

The LCL filter is made of L_1 and L_2 inductors, C_d capacitors and R_d damping resistors. We define *Z* as the inverter-to-grid impedance. At fundamental frequency, the LCL filter can be summarized as the sum of the inductances L_1 and L_2 [8], and in addition, the grid inductor. We denote L and R as the total inductor and resistor, respectively. The Fig. 3 and Fig. 4 shows the synthetized structure of the T-Type 3L and T-Type 5L inverters, respectively. The Fig. 5 depicts the realization of this T5L converter, which is currently undergoing experimental testing and will be the subject of result comparisons in future publications.

Assuming the grid balancing: $v_{g,a}+v_{g,b}+v_{g,c}=0$. The dynamic model of grid-tied T-Type inverters can be made. We denote $x=[a,b,c]^T$. According to Kirchhoff's voltage law [9]:

$$L\frac{d\,i_{i,x}}{dt} = -R\,i_{i,x} + v_{i,x\_O} + v_{O\_N} - v_{g,x} \quad (2)$$

$$L\frac{d\,i_{i,x}}{dt} = -R\,i_{i,x} + v_{i,x\_N} - v_{g,x} \quad (3)$$

By considering v_{i,x_O}, measured voltage between one phase at the inverter output and the neutral point O; $v_{O\_N,}$ measured voltage between the neutral point and N; v_{i,x_N} measured voltage between one phase at the inverter output and N.

A. Dynamic model of grid-tied 3L T-Type inverter

$$v_{i,x\_O} = S_{x2}\,v_{C2} - S_{x0}\,v_{C1} \quad (4)$$

$$v_{i,x\_N} = M_x v_{i,x\_O} \quad (5)$$

$$M_x = \begin{bmatrix} M_a \\ M_b \\ M_c \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix}$$

Note that the matrix M_x is common to T3 and T5 equations.

$$A_3 = \begin{bmatrix} -R & 0 & 0 & M_aS_{a2} & M_aS_{a0} \\ 0 & -R & 0 & M_bS_{b2} & M_bS_{b0} \\ 0 & 0 & -R & M_cS_{c2} & M_cS_{c0} \\ -S_{a2} & -S_{b2} & -S_{c2} & 0 & 0 \\ S_{a0} & S_{b0} & S_{c0} & 0 & 0 \end{bmatrix};$$

$$B_3 = \begin{bmatrix} -2/3 & 1/3 & 1/3 & 0 \\ 1/3 & -2/3 & 1/3 & 0 \\ 1/3 & 1/3 & -2/3 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \end{bmatrix} X_3 = \begin{bmatrix} i_{i,a} \\ i_{i,b} \\ i_{i,c} \\ v_{C2} \\ v_{C1} \end{bmatrix} U_3 = \begin{bmatrix} v_{g,a} \\ v_{g,b} \\ v_{g,c} \\ i_{dc1} \end{bmatrix}$$

$$\begin{bmatrix} \dot{L}i_{i,a} & \dot{L}i_{i,b} & \dot{L}i_{i,c} & \dot{C}v_{C2} & \dot{C}v_{C1} \end{bmatrix}^T = A_3\,X_3 + B_3U_3 \quad (6)$$

B. Dynamic model of grid-tied 5L T-Type inverter

$$v_{i,x\_O} = S_{x4}(v_{C4}+v_{C3}) + S_{x3}v_{C3} - S_{x1}v_{C2} - S_{x0}(v_{C2}+v_{C1}) \quad (7)$$

$$A_5 = \begin{bmatrix} -R & 0 & 0 & M_aS_{a4} & M_aS_{a3} & M_aS_{a1} & M_aS_{a0} \\ 0 & -R & 0 & M_bS_{b4} & M_bS_{b3} & M_bS_{b1} & M_bS_{b0} \\ 0 & 0 & -R & M_cS_{c4} & M_cS_{c3} & M_cS_{c1} & M_cS_{c0} \\ -S_{a4} & -S_{b4} & -S_{c4} & 0 & 0 & 0 & 0 \\ -S_{a43} & -S_{b43} & -S_{c43} & 0 & 0 & 0 & 0 \\ S_{a10} & S_{b10} & S_{c10} & 0 & 0 & 0 & 0 \\ S_{a0} & S_{b0} & S_{c0} & 0 & 0 & 0 & 0 \end{bmatrix}$$

With $S_{a43} = S_{a4} + S_{a3}$ and $S_{a10} = S_{a1} + S_{a0}$

$$B_5 = \begin{bmatrix} -2/3 & 1/3 & 1/3 & 0 \\ 1/3 & -2/3 & 1/3 & 0 \\ 1/3 & 1/3 & -2/3 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \end{bmatrix}; X_5 = \begin{bmatrix} i_{i,a} \\ i_{i,b} \\ i_{i,c} \\ v_{C4} \\ v_{C3} \\ v_{C2} \\ v_{C1} \end{bmatrix}; U_5 = \begin{bmatrix} v_{g,a} \\ v_{g,b} \\ v_{g,c} \\ i_{dc1} \end{bmatrix};$$

$$\begin{bmatrix} \dot{L}i_{i,a} & \dot{L}i_{i,b} & \dot{L}i_{i,c} & \dot{C}v_{C4} & \dot{C}v_{C3} & \dot{C}v_{C2} & \dot{C}v_{C1} \end{bmatrix}^T = A_5\,X_5 + B_5U_5 \quad (8)$$

The Park transformation (9) is used here for a better control of the active and reactive powers [9]. Considering the Sine-based Park transformation with the q-axis aligned to the a-axis at t = 0, leads to d-q state equation below.

$$T_\theta = \frac{2}{3}\begin{bmatrix} \sin(\theta) & \sin\left(\theta-\frac{2\pi}{3}\right) & \sin\left(\theta+\frac{2\pi}{3}\right) \\ \cos(\theta) & \cos\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta+\frac{2\pi}{3}\right) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \quad (9)$$

Eq. (3), is then written:

$$\begin{cases} \dfrac{L\,di_{i,d}}{dt} = -Ri_{i,d} + Lwi_{i,q} + v_{i,d\_N} - v_{gd} \\ \dfrac{L\,di_{i,q}}{dt} = -Ri_{i,q} - Lwi_{i,d} + v_{i,q\_N} - v_{gq} \end{cases} \quad (10)$$

$$\begin{cases} v_{i,d\_N} = \left(L\dfrac{di_{i,d}}{dt} + Ri_{i,d}\right) + \left(-Lwi_{i,q} + v_{g,d}\right) \\ v_{i,q\_N} = \left(L\dfrac{di_{i,q}}{dt} + Ri_{i,q}\right) + \left(Lwi_{i,d} + v_{g,d}\right) \end{cases} \quad (11)$$

Better signals can be obtained by replacing the measured dq-axis currents with referenced dq-axis currents, in the decoupled component terms [11]. By considering:

$$v_{i,dq}^{\ *} = L\frac{di_{i,dq}}{dt} + Ri_{i,dq} \quad (12)$$

The control of the dq-axis currents is therefore based on Eq. (11). The structure of the inverter is scalable to higher levels, as well as its dynamic mathematical model.

4. T-Type inverters control strategy

Classical Sine PWM technique control satisfies the v_{ck} balancing of three-level structures (T-Type, NPC, FC) quite well [2]. At the higher level, the switching states increase and have more degrees of "freedom" - due to the increase of switches - which is an advantage but also a disadvantage. Algorithmic modulation strategies, such as Space Vector Modulation (SVM), allow to take benefit of redundant states (or these degrees of freedom) [12] [13]. However, the equations quickly become complex, and the high computational burden. The unbalance shows a non-zero current at each capacitor [14]:

$$i_{Ck}dt = C_k\left(V_{Ck} - \frac{V_{dc1}}{n-1}\right) \quad (13)$$

The mathematical equations of T5 allow to evaluate the possible variables influencing the unbalance of the input voltages and on which we could interact.

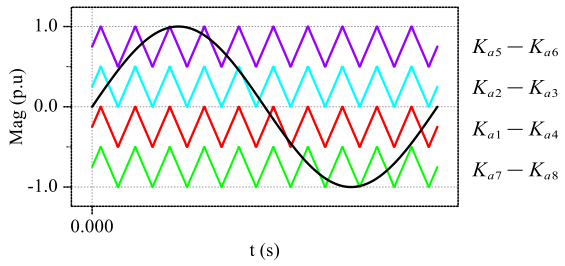


Fig. 6. Level Shifted PWM for 5L T-Type inverter

The modulation technique used in this paper is Level Shifted PWM, where the carriers are shifted in amplitude. Each carrier corresponds to a switching arm and a voltage level of the inverter. In this paper, capacitor voltages are assumed to be perfectly balanced.

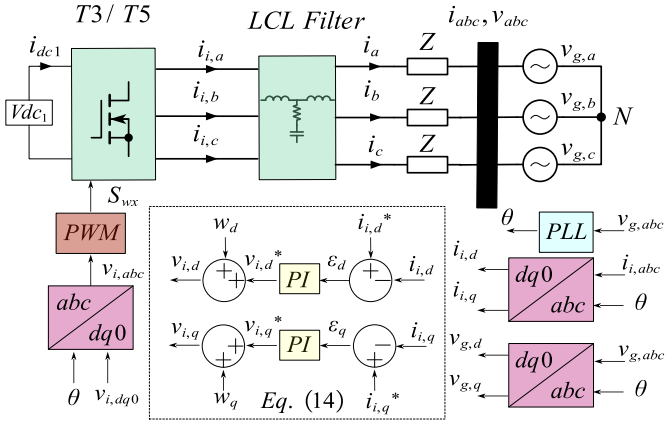


Fig. 7. *Grid connected T-Type inverter, PI Controller*

A. PI Controller

We can express Eq. (11) in this form:

$$\begin{cases} v_{i,d}^{\ *} = v_{i,d} + w_d \\ v_{i,q}^{\ *} = v_{i,q} + w_q \end{cases} \quad (14)$$

The calculation of the PI controller gains, K_p and K_I, is based on the reference model $v_{i,dq}$* [15]. The objective is to have $i_{i,dq} = i_{i,dq}$*. Let the reference system be denoted S(p) by applying the Laplace transform:

$$S(p) = \frac{K_S}{\tau_S.p+1} = \frac{1}{L.p+R} \quad (15)$$

The PI controller transfer function is then given by (16):

$$C_{PI}(p) = K_P\left(\frac{\tau_C.p+1}{\tau_C.p}\right) = K_P + \frac{K_I}{p} \quad (16)$$

By applying the dominant pole compensation (τ_C=τ_S), the system is summarized in a function of first order in closed loop. Thus, and according to the desired system speed c, the gains K_p and K_I can be determined:

$$K_P = \frac{c}{K_S}; K_I = \frac{K_P}{\tau_S.p} \quad (17)$$

5. Simulation results

The simulations were performed on MATLAB/Simulink in closed loop with the PI controller. The table below shows parameters defined for the simulation.

Table IV. – Simulation parameters

T-Type parameters	***LCL filter parameters***	***Grid parameters***	***PI gains***
P_n=35 kW	L_1=450 µH	U_n=400 V	K_P=10
f_d =20 kHz	L_2=350 µH	f_n=50 Hz	K_I =179 p^{-1}
V_{dc1}=1 kV	R_d =1 Ω	L_g=0.1 mH	
C=3000 µF	C_d=20 µF		

Rated voltage U_n and rated power P_n are defined as base for per unit conversion. For simulations, d-axis current step is applied at:

- t = 0 s, $i_{i,d}^*$ = 0.8 p.u ;
- t = 0.3 s, $i_{i,d}^*$ = 1 p.u ;
- t = 0.5 s, $i_{i,d}^*$ = 0.6 p.u.

A. Graph results

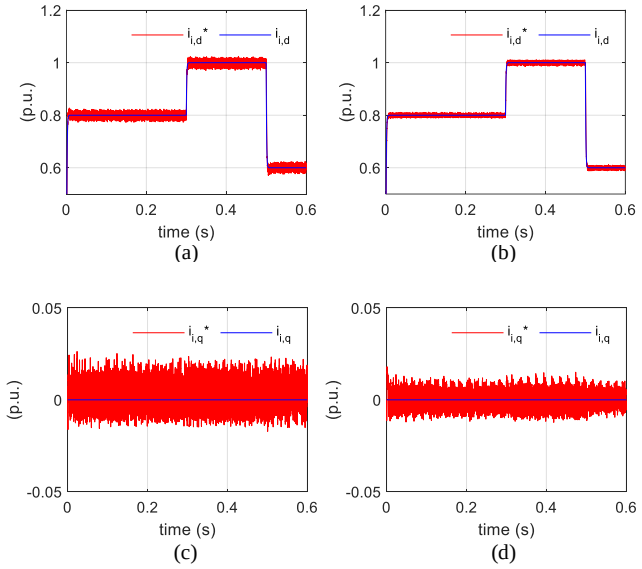
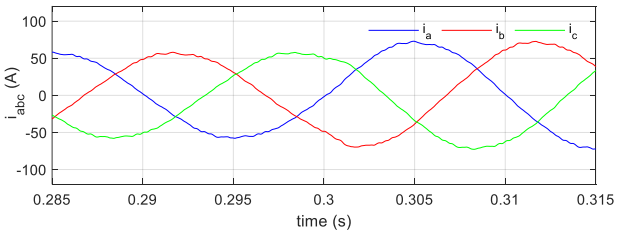
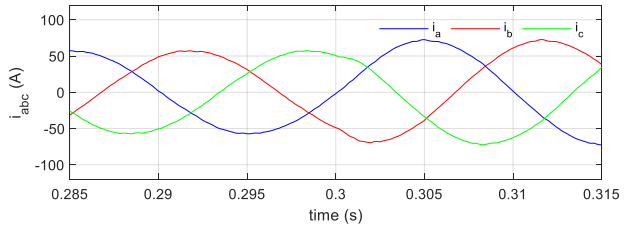


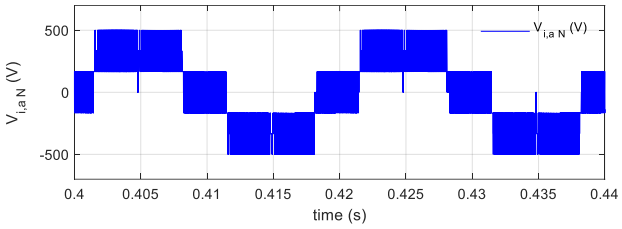
Fig. 8. T3: d-axis (a) and q-axis currents (c) ; T5: d-axis (b) and q-axis currents (d) ;



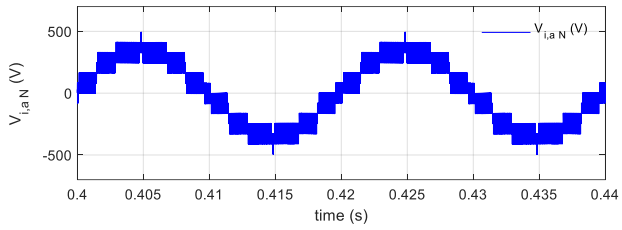


(b)

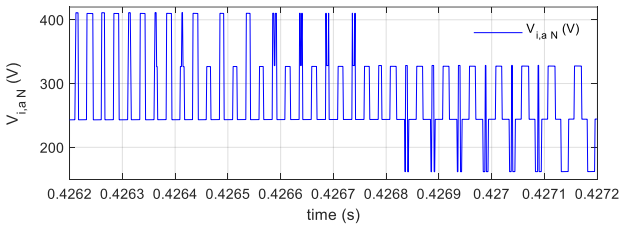
Fig. 9.T3 : abc-axis currents (a) ; T5 : abc-axis currents



(a)

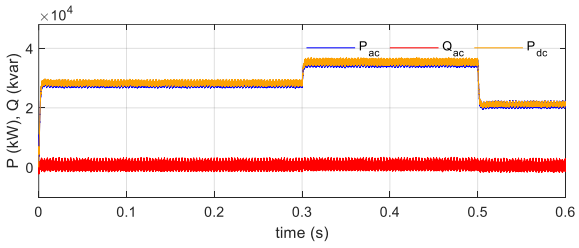


(b)

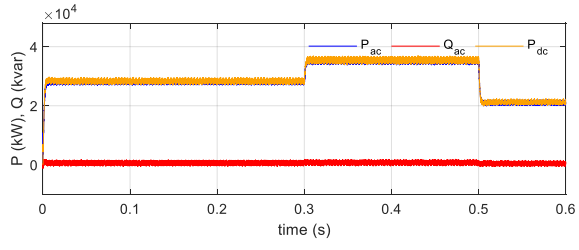


(c)

Fig. 10. T3: Inverter output voltage (a); T5 : Inverter output voltage (b); T5: Inverter output voltage (1ms) (c)

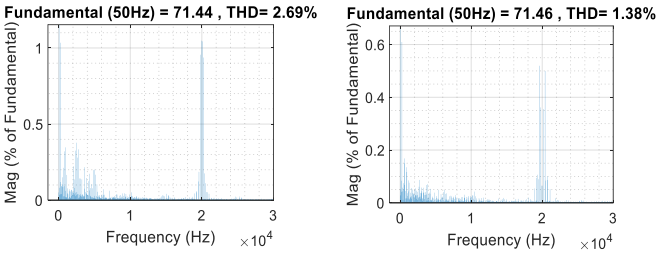


(a)



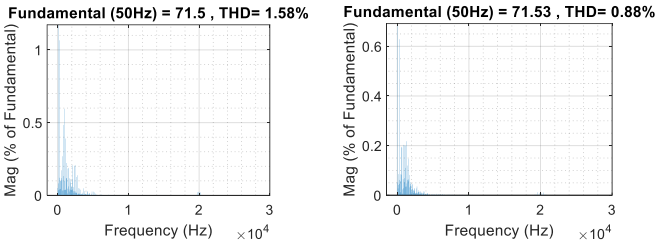
(b)

Fig. 11. T3: Active, reactive and bus power (a) ; T5: Active, reactive and bus power (b) ;



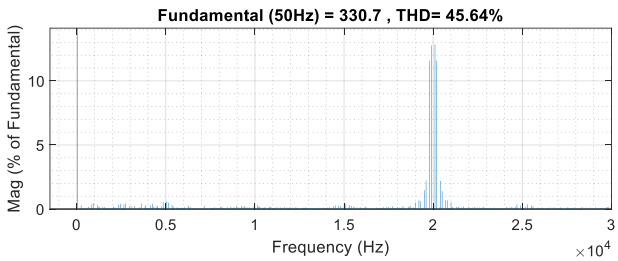
(a) (b)

Fig. 12. Total Harmonic Distorsion of phase a current (Before Filter), T3 (a) and T5 (b), respectively.



(a) (b)

Fig. 13. Total Harmonic Distorsion of phase a current (After Filter), T3 (a) and T5 (b), respectively



(a)

(b)

Fig. 14. Total Harmonic Distorsion of phase a-to-neutral inverter voltage, T3 (a) and T5 (b), respectively.

Active P and reactive Q powers control is possible through dq-axis currents $i_{i,d}$* and $i_{i,q}$* , respectively [9] [15]. Since the reactive power is desired setting to zero, the q-axis current $i_{i,q}$* p.u. According to Park transform the d and q axis grid voltages are set to $v_{g,d} = 1p.u$ and $v_{g,q}=0$ p.u, respectively. Given the following active and reactive power formulas, respectively:

$$P_{3\varphi}=\frac{3}{2}\left(v_{g,d}\, i_{i,d} + v_{g,q}\, i_{i,q}\right) ; Q_{3\varphi}=\frac{3}{2}\left(v_{g,d}\, i_{i,q} - v_{g,q}\, i_{i,d}\right)$$

$$P_{3\varphi}=\frac{3}{2} v_{g,d}\, i_{i,d} \; ; Q_{3\varphi}=0 \; ; \qquad (18)$$

The modulation index is given by the following formula.

$$m = \frac{2\sqrt{2}U_n}{\sqrt{3}V_{dc1}} \quad (19)$$

There is no significant difference in the reference tracking of the d- and q-axis currents between the three-level and five-level inverters (Fig. 9). The difference is mainly in the harmonics. With the T5 structure, the inverter output voltages (v_{i,x_N}) THD, are divided by two, compared to the T3 structure. The harmonic distortions of (v_{i,x_N}) Fig. 10, are shown in Fig. 14 at the fundamental frequency of 50 Hz. Current ($i_{i,x}$) harmonics are clearly higher with the T3 structure than T5 structure, both before and after the filter. Current $i_{i,x}$ harmonics are shown in Fig. 12 and Fig. 13, at the fundamental frequency of 50 Hz. The active and reactive powers are proportional to the d and q axis currents, respectively. Losses due to switching and conducting were not considered in the simulation, the output power is then equal to the input power. The T5 structure is more efficient, the reactive power fluctuation is lower compared to the T3 structure. The obtained signals with T5 attest to his relevance of this structure. In accordance with the IEEE 519-1992 code requirements, the grid side inductance is designed to reduce the grid current THD which should not exceed 5%.

6. Conclusion

This study compares the performance of grid-tied T-Type three-level and five-level inverters utilizing a closed-loop strategy. The PI linear controller is employed for d- and q-axis current reference tracking, and the analysis is conducted without considering any disturbances. The simulation results indicate that both inverter structures show satisfactory dynamic performance, with the T5 inverter structure exhibiting superior signal quality concerning AC side current and voltage total harmonic distortion. This paper confirms the validity of the T-type inverter grid-connected mathematical model, and it also facilitates the identification of potential variables that are susceptible to intrinsic imbalance. The classic sine Pulse Width Modulation technique was utilized to control the MOSFET switches, under the assumption of perfectly balanced capacitor voltages. However, to overcome the issue of imbalanced DC-side capacitor voltages, a forthcoming article will employ a Space Vector Pulse Width Modulation algorithm. The latter will be integrated with closed loop strategies. In addition, A further experimental phase will implement the algorithms in a real-time system to control the T-Type five-level inverter. The experimental results will be presented as well as the hardware design of the inverter, which is composed of SiC MOSFETs.

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References

[1] A. Hassan, X. Yang, W. Chen, et M. A. Houran, « A State of the Art of the Multilevel Inverters with Reduced Count Components », *Electronics*, vol. 9, nº 11, p. 1924, nov. 2020, doi: 10.3390/electronics9111924.

[2] J. Rodriguez, J. Leon, S. Kouro, et R. Portillo, « The Age of Multilevel Converters Arrives. Industrial Electronics », *IEEE Power Engineering Society Summer Meeting*, p. 28-39, janv. 2008.

[3] J.-S. Lai et F. Z. Peng, « Multilevel converters-a new breed of power converters », *IEEE Transactions on Industry Applications*, vol. 32, nº 3, p. 509-517, mai 1996, doi: 10.1109/28.502161.

[4] T. A. Meynard et H. Foch, « Multi-level conversion: high voltage choppers and voltage-source inverters », in *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, juin 1992, p. 397-403 vol.1. doi: 10.1109/PESC.1992.254717.

[5] P. Chaturvedi, « Conventional Multilevel Inverter », in *Modeling and Control of Power Electronics Converter System for Power Quality Improvements*, Elsevier, 2018, p. 85-120. doi: 10.1016/B978-0-12-814568-5.00003-X.

[6] J. Zhang, S. Xu, Z. Din, et X. Hu, « Hybrid Multilevel Converters: Topologies, Evolutions and Verifications », *Energies*, vol. 12, nº 4, p. 615, févr. 2019, doi: 10.3390/en12040615.

[7] V. Yaramasu, A. Dekka, et S. Kouro, « Multilevel converters for renewable energy systems », in *Multilevel Inverters*, Elsevier, 2021, p. 155-184. doi: 10.1016/B978-0-323-90217-5.00007-1.

[8] M. Said-Romdhane, M. Naouar, I. Belkhodja, et E. Monmasson, « An Improved LCL Filter Design in Order to Ensure Stability without Damping and Despite Large Grid Impedance Variations », *Energies*, vol. 10, nº 3, p. 336, mars 2017, doi: 10.3390/en10030336.

[9] D. Zhang, L. Zhang, J. Jiang, J. Li, B. Wang, et Z. Zhou, « Design of T-type three-level energy storage inverter and grid-connected control strategy », in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, oct. 2017, p. 1072-1076. doi: 10.1109/IECON.2017.8216184.

[10] F. Sebaaly, H. Vahedi, H. Y. Kanaan, N. Moubayed, et K. Al-Haddad, « Sliding Mode Fixed Frequency Current Controller Design for Grid-Connected NPC Inverter », *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, nº 4, p. 1397-1405, déc. 2016, doi: 10.1109/JESTPE.2016.2586378.

[11] Z. Yao, L. Xiao, et J. M. Guerrero, « Improved control strategy for the three-phase grid-connected inverter », *IET Renewable Power Generation*, vol. 9, nº 6, p. 587-592, août 2015, doi: 10.1049/iet-rpg.2014.0350.

[12] D. Lalili, E. M. Berkouk, F. Boudjema, et N. Lourci, « Self balancing of DC link capacitor voltages using redundant vectors for SVPWM controlled five-level inverter », in *2008 5th International Multi-Conference on Systems, Signals and Devices*, Amman, juill. 2008, p. 1-6. doi: 10.1109/SSD.2008.4632822.

[13] O. Bouhali, B. Francois, E. M. Berkouk, et C. Saudemont, « DC Link Capacitor Voltage Balancing in a Three-Phase Diode Clamped Inverter Controlled by a Direct Space Vector of Line-to-Line Voltages », *IEEE Trans. Power Electron.*, vol. 22, nº 5, p. 1636-1648, sept. 2007, doi: 10.1109/TPEL.2007.904174.

[14] M. Marchesoni, M. Mazzucchelli, et P. Tenca, « An optimal controller for voltage balance and power losses reduction in MPC AC/DC/AC converters », in *2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018)*, Galway, Ireland, 2000, vol. 2, p. 662-667. doi: 10.1109/PESC.2000.879896.

[15] A. Darkawi, T. Kovaltchouk, H. Ben Ahmed, B. Multon, et S. Hamonic, « Modélisation, Commande et Mise en Oeuvre de deux Ponts Triphasés Back-to-Back avec Contrôle des Flux de Puissance et de la Tension du Bus DC : Application à l'émulation de la chaîne de conversion électrique des houlogénérateurs directs », juill. 2015.