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Development and testing midpoint voltage balance algorithms of three-level inverters

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Abstract. Nowadays, the use of inverters is increasing in more and more applications. Environmental awareness is becoming a trend, so more and more people install solar energy systems on their houses, which also require the use of inverters. Higher power levels have led to the emergence of three-level inverters which has opened up new challenges, such as the issue of midpoint voltage balancing. This paper discusses voltage balancing and voltage ripple reduction techniques for three-level inverters with Neutral-Point Clamped (NPC) topology. The balancing is based on injecting zero-sequence voltage component in carrier-based modulation. The viability of the modulation techniques are verified by computer simulation and then tested on hardware.

Key words. Multi level, Inverter, Midpoint, Balance, Low ripple, Modulation, Simulation, Simulink code generation

1. Introduction

The main advantages of three-level inverters over the more common two-level ones are their lower output current ripple and lower switching noises. the disadvantage is that unbalanced voltages can cause damage to the semiconductors so care must be taken to avoid the case. Different modulation techniques can provide an economical software solution to this problem [1]. Various applications may require a minimum midpoint voltage ripple, so besides the balancing, ripple minimization is also a new challenge of the three-level inverter usage.

In this paper the Neutral-point Clamped (NPC) topology is studied, but the balancing methods can be utilized in other topologies e.g. in T-type three-level topology. An NPC topology three-level inverter consists of four switching devices in each phase, as shown in Fig. 1 [2][3]. Hereafter, we consider the midpoint voltage of the DC link capacitors (U_N) against a virtual reference point. The reference point is chosen in such a way that, in case of voltage balance ($U_{DCP} = U_{DCN} = \frac{U_{DC}}{2}$), the midpoint voltage should equal to zero. This can also be imagined like two serial DC voltage sources with a value of $\frac{U_{DC}}{2}$, and their common output is taken as the reference point [4].

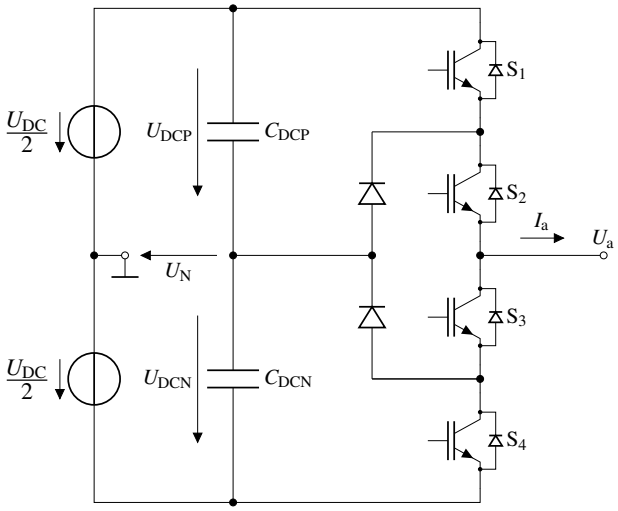


Fig. 1. Circuit of the NPC topology

There are different solutions to keep the midpoint voltage equal to zero. One way of balancing is injecting a properly determined zero-sequence voltage into the reference voltages of carrier-based modulation [5]. In this case the output voltage levels, and thus the control signals of the semiconductors, can be determined by comparing the reference voltage signals with two triangular carrier signals. By shifting the reference signals up or down, the power from the positive and negative rails can be controlled and therefore the midpoint voltage also can be controlled.

An alternative way is the space vector approach, where a voltage vector is assigned to each switching state, and then a modulation algorithm generates the required rotating voltage space vector as a weighted sum of several space vectors in a switching period. The $3^3 = 27$ switching states produce 19 voltage vectors, these vectors can be classified by their magnitude: zero vectors, small vectors, middle vectors, and large vectors. The space vector based balancing methods mostly adjusting the redundant switching states of small vectors and their dwelling time, which is practically the process of deciding the zero-sequence voltage [6].

In this paper, carrier-based balancing methods are studied

conceptually, by means of simulations and by hardware tests. First, the balancing problem with simple sinusoidal modulation is introduced in section 2. After that, section 3. presents that using symmetrical modulation the balancing is automatically implemented in motoring mode. In section 4. balancing based on the active power direction is introduced. The deficiency of this method at purely reactive operating points can be eliminated by considering current and voltage directions. The zero-sequence voltage is extended with a component to reduce the midpoint voltage ripple in section 5. Finally, the most promising algorithm is implemented in a model-based way by generating codes from MATLAB/Simulink models, and tested in a hardware environment.

2. Sinusoidal modulation

The switching signals of voltage inverters are usually defined by the output voltage reference. This can be done in several ways, called *modulations*. In case of an NPC topology, S_2 switch is permanently on at the positive half-period of the reference voltage, and the duty cycle of S_1 and S_3 is continuously varying [7]. Sinusoidal modulation is the most basic type of modulation, where the duty cycles can be calculated from the following equations:

$$d_1 = d_{S1} = \begin{cases} \dfrac{U_{ref}}{U_{DCP}}, & \text{if } U_{DCP} \geq U_{ref} > 0 \\ 0, & \text{otherwise} \end{cases} \tag{1}$$

$$d_2 = d_{S4} = \begin{cases} \dfrac{U_{ref}}{-U_{DCN}}, & \text{if } U_{DCN} \leq U_{ref} < 0 \\ 0, & \text{otherwise} \end{cases} \tag{2}$$

The only advantage of this modulation is its simplicity, although it has several disadvantages. The peak value of the phase voltage can only reach half of the DC voltage, even though the topology allows the line voltage to be as high as U_{DC}, which corresponds to a phase voltage of $\frac{U_{DC}}{\sqrt{3}}$ [8]. The use of this modulation causes an imbalance between the two DC link capacitor voltages. The explanation for this is in the equations above. In the positive half-period, the duty cycle d_1 is divided by the positive DC voltage. When U_{DCP} increases (U_N decreases), the duty cycle decreases, so in motoring mode, less current is drawn from C_{DCP} capacitor, which will cause an increased U_{DCP}, thus a positive feedback is formed.

A simulation was created in MATLAB Simulink to investigate this effect. The DC voltage was chosen to 800 V, from which a sinusoidal phase voltage was generated with a peak value of 400 V and a fundamental frequency of 100 Hz at 10 kHz switching frequency. The load was simulated by a three phase current generator with a peak value of 200 A. The DC link capacitors both have a capacitance of 10 mF. The simulation results are shown in Fig. 2. As explained above, the mean value of the midpoint voltage increases significantly after only a few fundamental harmonic period times. Applying larger capacitance can delay unbalancing,

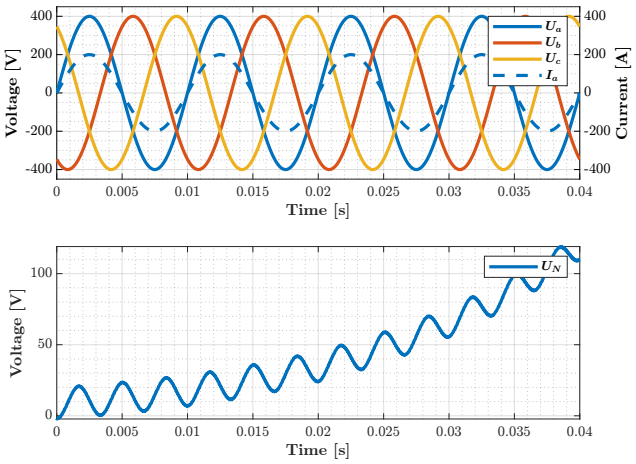


Fig. 2. DC midpoint voltage (U_N) in motoring mode, using sinusoidal modulation.

but it cannot be stopped, only with additional balancing hardware.

The simulation also shows the oscillation of the midpoint voltage. The frequency of this oscillation equals three times the fundamental harmonic frequency of the output phase voltage. This is a normal effect of the topology. If we investigate a 60° angular range where one phase voltage is positive and the other two are negative, we can see that in motoring mode the current of C_{DCP} capacitor is proportional to $cos^2(\omega t)$, since the phase shift between the positive phase voltage and current equals to zero.

3. Symmetrical modulation

Symmetrical modulation (space vector modulation) is commonly used instead of sinusoidal modulation. The basic idea behind this method is to shift the reference phase voltages so that the maximum of the three phase voltages gets exactly as far from the positive DC voltage as the minimum is from the negative DC voltage [9] [10]. Expressing this mathematically leads us to the equation for the required offset:

$$U_0 = -\frac{U_{max} + U_{min} + U_{DCN} - U_{DCP}}{2} = -\frac{U_{max} + U_{min}}{2} - U_N, \tag{3}$$

where,

U_0	is the required offset,
U_{max}	is the maximum value of the phase voltages,
U_{min}	is the minimum value of the phase voltages.

The advantage of this modulation is that the line voltage waveform is sinusoidal and its peak value can reach U_{DC} value. It is also an advantage that in motoring mode, the DC midpoint voltage remains balanced, which is concluded from eq. (3). If U_{DCP} increases (U_N decreases), then U_0 increases, therefore duty cycle d_1 also increases, so in motoring mode, more current is drawn from C_{DCP} capacitor, which will cause lower U_{DCP}, thus a negative feedback is created.

To demonstrate this effect, another simulation was performed with the same parameters as above. The results are

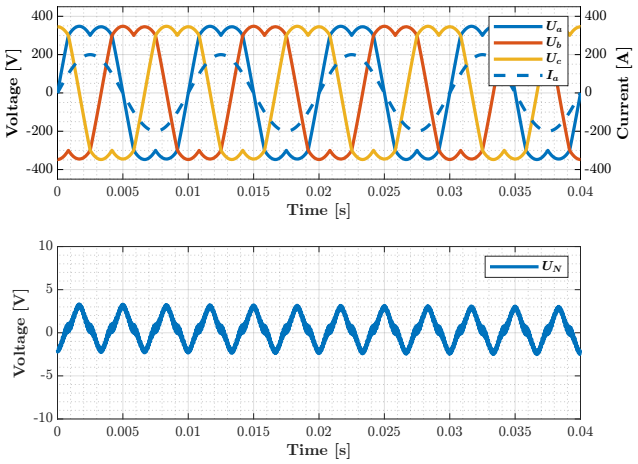


Fig. 3. DC midpoint voltage (U_N) in motoring mode, using symmetrical modulation.

shown in Fig. 3. It can be seen that the mean value of the midpoint voltage equals to zero, so stability is achieved. It can also be observed that the voltage ripple is significantly smaller compared to the case of sinusoidal modulation. In generating mode, the positive feedback returns, since the phase shift between the phase voltage and current changes sign, so the current of C_{DCP} capacitor also changes its sign [11].

4. Balancing methods

A. *Method based on power direction*

Using symmetrical modulation causes negative feedback in motoring mode and positive feedback in generating mode as the midpoint voltage changes. Therefore, it would be a reasonable solution to apply an additional offset to the reference phase voltages with the opposite direction of the midpoint voltage change for positive active power, and with the same direction for negative active power. This way, in generating mode, if U_{DCP} increases (U_N decreases), U_0 decreases, thus the duty cycle d_1 also decreases, so C_{DCP} capacitor is charged with a lower current, which will cause a decreased U_{DCP}. The required offset can be written by the following equation:

$$U_0 = -\frac{U_{max}+U_{min}}{2} - U_N - sign(P)\cdot K_P \cdot U_N, \qquad (4)$$

where,

P	is the active power,
K_P	is a proportional gain factor.

According to eq. (4), with the right K_P parameter, the $-U_N$ component, which is responsible for the positive feedback, can be eliminated. A major disadvantage of this method is that sign determination of the low active power is unreliable because of measurement noise or sensor accuracy, so the positive feedback may not be eliminated but even increased. Such operating points occur when there is almost only reactive power.

B. *Method based on the current direction*

The basic idea of this method is almost the same as the previous one, but the sign of the proportional gain depends on the phase current sign which phase's voltage sign is different from the other two phases. Let us assume a purely reactive current flowing in one of the phases and investigate the 60° angular range where only U_a is positive (shown in Fig. 4). The current of this phase is negative at half of the range and positive at the other half.

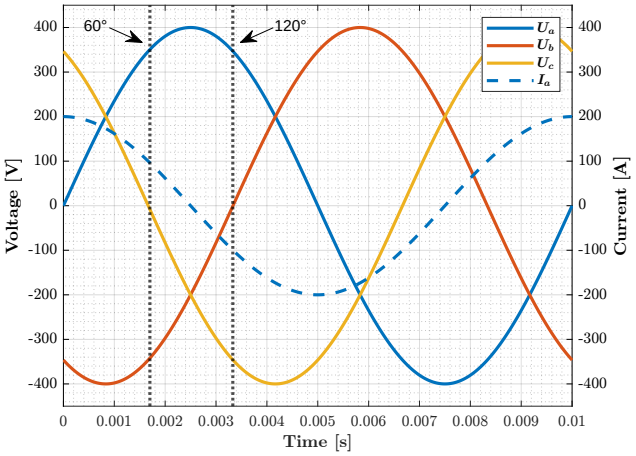


Fig. 4. Illustration of the method based on the current sign when only U_a phase voltage is positive.

In the 30° time slice where the current is negative, U_0 offset should be lowered to reduce the injected power into the positive rail, which prevents C_{DCP} from charging and thus the midpoint voltage from dropping. In case of positive current, the reverse should be done. If U_a phase voltage is negative, the current sign should be considered reversed for both current directions, because the current of C_{DCP} capacitor is also reversed. The equation for this method is the following:

$$U_0 = -\frac{U_{max}+U_{min}}{2} - U_N + f(U,I)\cdot K_P \cdot U_N, \qquad (5)$$

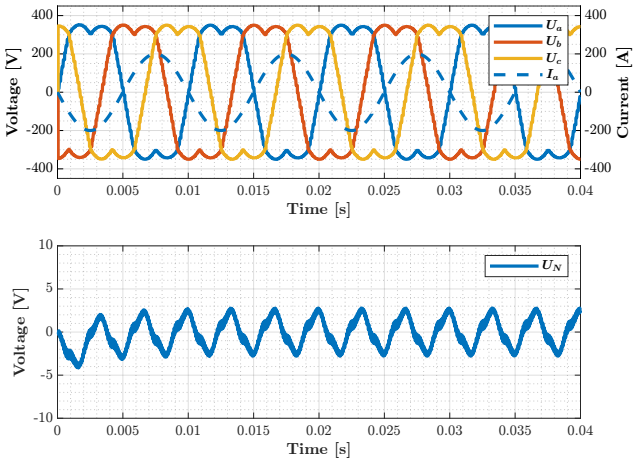
where,

$f(U,I)$	is a sign function,
K_P	is a proportional gain factor.

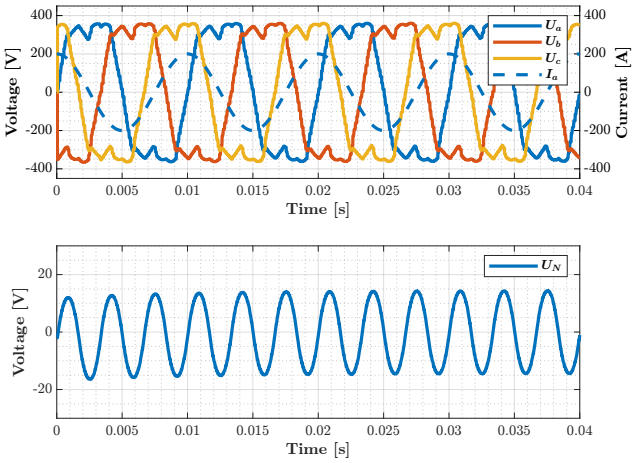
Reference voltages have positive and negative offset limits. Firstly, neither of the phase voltages can exceed the voltage of the two DC rails. Secondly, there are working points where the sign change of a phase voltage causes an opposite effect on the midpoint voltage than it was originally intended. In the following, limits are calculated for the case when Ua phase voltage is positive and the other two are negative.

In case of a positive offset, one of the possible upper limits is the voltage difference between U_a and the positive rail, due to the upper limit of the duty cycle. The other possible upper limit is the lower one of U_b and U_c phase voltages in absolute value, so the offset does not cause a sign change in either phase.

$$U_{0_{max}} = \min(U_{DCP} - U_a, |U_b|, |U_c|) \qquad (6)$$



(a) Generating mode



(b) Reactive operating point

Fig. 5. The method based on the current sign

In case of a negative offset, U_a phase voltage is one of the possible limits in signal change point of view, and the other limit is the smaller one of the voltage differences between the negative rail and U_b or U_c phase voltages.

$$U_{0_{min}} = \min(U_a, U_b - U_{DCN}, U_c - U_{DCN}) \tag{7}$$

By the limit calculation, the peak value of the line voltage can be U_{DC} even with sinusoidal modulation. If U_a phase voltage is higher than the half of the DC voltage, then $U_{0_{max}}$ will be negative due to the limits. That means the maximum phase voltage can be $\frac{U_{DC}}{\sqrt{3}}$.

The method was implemented in MATLAB/Simulink environment and tested with the same parameters as in the previous simulations. Symmetrical modulation was used as initial reference voltage. The data recorded for generating mode and for reactive operating point are shown in Fig. 5.

In both cases $K_P = 2$ proportional gain factor was used and the midpoint voltage was stabilized [12]. It can also be seen that for reactive operating point the reference voltage waveform is significantly different and the fluctuation of the midpoint voltage is larger.

5. Midpoint voltage ripple reduction

The lowest possible midpoint voltage ripple can be required because manufacturers try to reduce the cost of the components used. With lower midpoint voltage ripple, switching elements should handle a lower maximum voltage.

The midpoint voltage has a ripple frequency that is three times of the fundamental frequency. For a 60° angular range, where U_a phase voltage is positive and U_b and U_c are both negatives (shown in Fig. 4), the power of the positive rail can be calculated using the following equation:

$$P_+ = \widehat{U}\cos(\omega t) \cdot \widehat{I}\cos(\omega t - \varphi), \tag{8}$$

where,

$\widehat{U}$ is the peak value of the voltage,
$\widehat{I}$ is the peak value of the current,
ω is the angular frequency,
φ is the phase shift between voltage and current

In order to minimize the ripple of the midpoint voltage, $P_+ = \frac{P}{2}$ equation should be satisfied. The power of the whole system can be calculated by the following equation:

$$P = \frac{3}{2}\widehat{U} \cdot \widehat{I} \cdot \cos(\varphi) = P_+ + P_-. \tag{9}$$

Based on eq. (8) and eq. (9), the time function of the phase voltage (U_X) can be expressed,

$$U_X \cdot \widehat{I} \cdot \cos(\omega t - \varphi) = \frac{3}{4}\widehat{U} \cdot \widehat{I} \cdot \cos(\varphi) \tag{10}$$

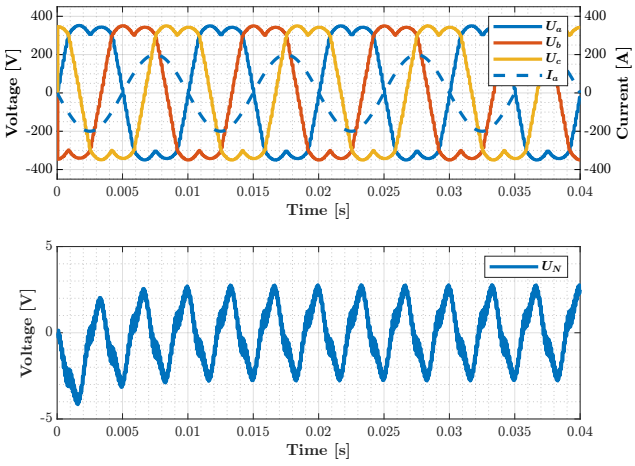
which is required to minimize the midpoint voltage ripple. From this the voltage reference offset also can be calculated as

$$U_0 = U_X - \widehat{U} \cdot \cos(\omega t) \tag{11}$$

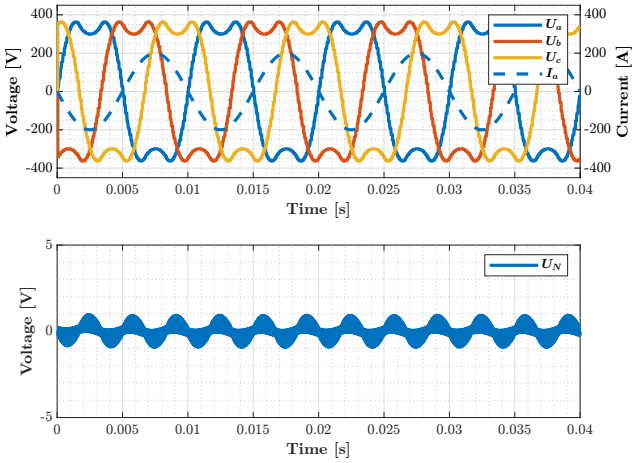
It can be seen that for an active operating point, this method can reduce the midpoint voltage to zero. However, for larger phase shifts, there is less space to offset the voltage reference, since it has physical limits.

The calculated offset was implemented in MATLAB/Simulink and added to the offset that is responsible for the balancing, and then limits were applied to this sum. Fig. 6 compare the results obtained with the previous ones, where only the balancing method based on the current sign was used with symmetrical modulation as initial voltage reference.

It can be observed that for an active operating point, the voltage ripple can actually be reduced to almost zero, only the switching noise is visible at the midpoint voltage signal. The method also can reduce the ripple at non-zero phase shifts, but not that efficiently.



(a) Without voltage ripple reduction



(b) With voltage ripple reduction

Fig. 6. Midpoint voltage ripple comparison at pure active operating point

6. Test on hardware

Since the midpoint voltage balancing based on current sign worked successfully in simulation, it was also tested on hardware. The test environment consists of a three-phase three-level inverter and a three-phase two-level inverter, with their phases connected to each other through inductors. Both inverters are powered by separate DC voltage supplies, so diodes and resistors are needed to ensure that the system does not feed back into either of the DC supplies. The circuit diagram of one phase is shown in Fig. 7.

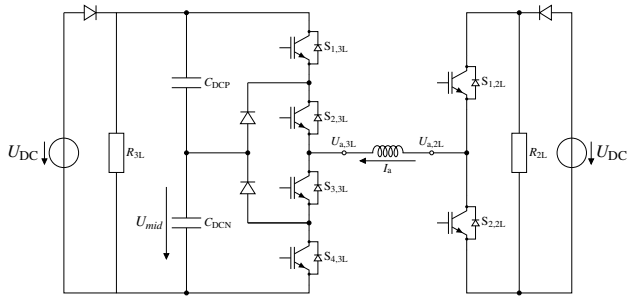


Fig. 7. Circuit of the test hardware

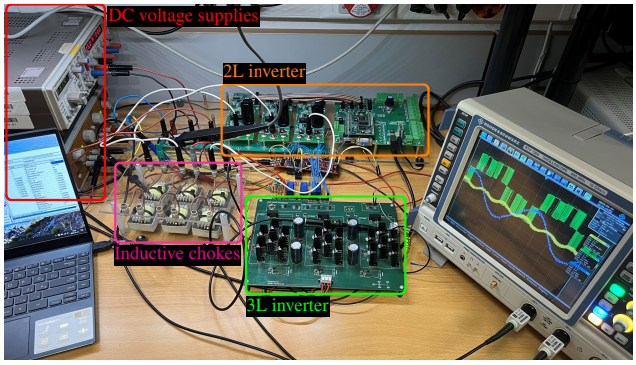


Fig. 8. Test hardware setup

The voltage control with midpoint balance of the three-level inverter was compiled to a TI C2000 microcontroller from simulation using Simulink embedded coder. The actual angle of the voltage is transmitted to the two-level inverter via CAN, which synchronizes to it using a PLL and operates in current-controlled mode with respect to that angle. Thus, the phase angle between voltage and current can be chosen freely, so the midpoint voltage balancing may be tested at any working point. Both inverters operate at 10 kHz switching frequency and their switching are synchronised in order to reduce the noise. Fig. 8 shows the test hardware setup in operation.

Table I. Parameters of the hardware test

Parameter	Value
$f_{fundamental}$	50 Hz
$f_{switching}$	10 kHz
U_{DC}	20 V
I_{ph}	2 A
U_{ph}	8 V

The method based on current sign and the ripple reduction was tested on hardware with the parameters in Table I. The phase shift between current and voltage was freely chosen from pure active to pure reactive operating points.

The requested voltage references and the measured phase currents can be seen in Fig. 9. The signals are sampled

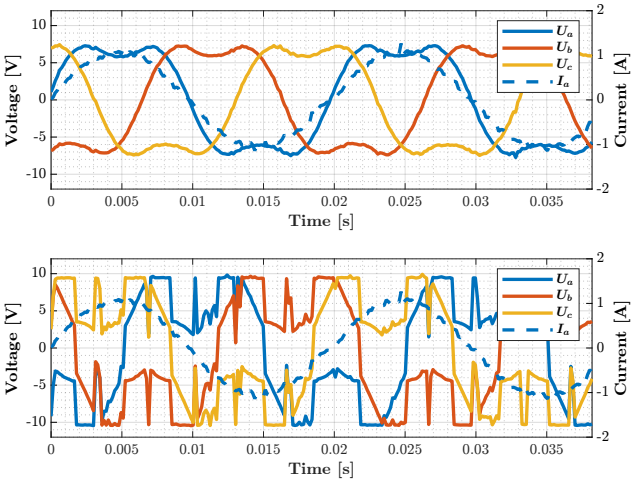


Fig. 9. Reference voltages for active and reactive operating points

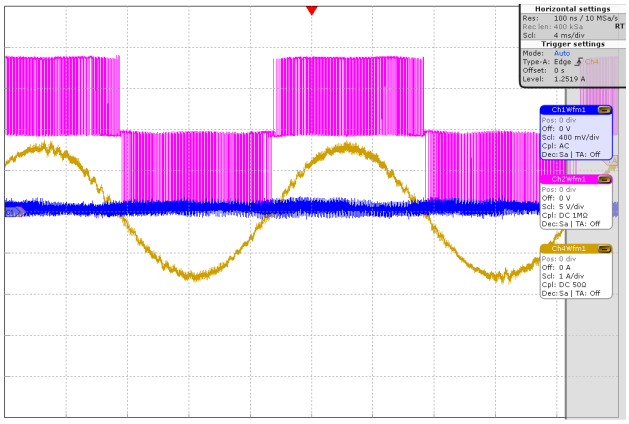


Fig. 10. Measurement at active operating point

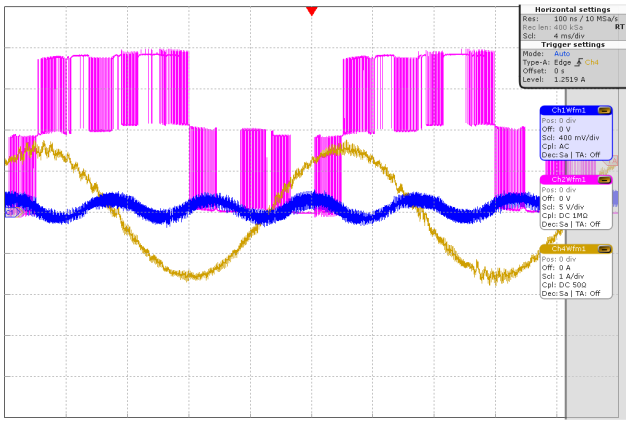


Fig. 11. Measurement at reactive operating point

in the microcontroller and the samples are transmitted to the PC through an USB link. The behavior of the three-level inverter was also monitored by a digital oscilloscope. Fig. 10 and Fig. 11 show the scope measurement results for the pure active and pure reactive operating points: midpoint voltage with blue, phase current with light brown and phase voltage with magenta. It can be observed, that the midpoint voltage remained balanced during operation, and the voltage ripple is almost reduced to zero at pure active operating point.

7. Conclusions

In this paper, the midpoint voltage balancing of three-level inverters was presented. It provides a balancing solution for motoring, generating, and also for pure reactive operating points. Based on the simulations and tests on hardware, the method based on the current sign proved to be the most successful, since it could balance the midpoint voltage at all operating points. Besides the balancing, a midpoint voltage ripple reduction method was also presented in the paper. The combination of these two methods can provide suitable modulation for NPC or TNPC topology three-level inverter applications.

Acknowledgments

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