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Real-time Simulation Framework for Validating Controllers of Virtual Synchronous Generators

M. M. R. Chowdhury[1], L. Stranyóczky[1] and Z. Sütő[1]

[1] Department of Automation and Applied Informatics, Faculty of Electrical Engineering and Informatics, Budapest University of Technology and Economics, Műegyetem rkp. 3., H-1111 Budapest, Hungary
e-mail: chowdhury.moshiur@aut.bme.hu, stranyoczky.laszlo@aut.bme.hu, suto.zoltan@aut.bme.hu

Abstract. The utilization of active rectifiers as converters in the interface between AC and DC microgrids has become a prevalent practice owing to their capacity to facilitate bidirectional power flow. The contemporary methodology for the development of power converters includes the integration of real-time simulation steps for the validation of control schemes and the assurance of safe implementation with hardware. The present study proposes a methodology for developing a real-time Hardware-in-the-Loop (HIL) simulation framework, which aims to facilitate the rapid prototyping of advanced control algorithms for an Active-Front-End (AFE) rectifier, especially a Virtual Synchronous Generator (VSG) control strategy. This approach aims to enhance the dynamic performance and stability of low-inertia power systems by mimicking the behavior of a synchronous generator, thereby providing virtual inertia to the power system. The control schemes and the primary circuit models are designed and implemented utilizing Matlab/Simulink and are optimized for code generation.

Key words. Active-Front-End (AFE) rectifier, Virtual Synchronous Generator, Microgrid, AC-DC power converters, Hardware-in-the-Loop (HIL) simulation, Simulink code generation, FPGA

1. Introduction

The utilization of Active Front End (AFE) rectifiers as interfaces between AC and DC microgrids has recently gained substantial attention as a viable solution, owing to their capacity to facilitate bidirectional power flow and provide a low harmonic content AC current. These attributes, in conjunction with the ability to control both active and reactive power, have rendered AFE rectifiers an attractive alternative for various applications [1]. For instance, in microgrids, bi-directional power flow enables the integration of renewable energy sources, such as solar and wind power equipped with energy storage capabilities, into the grid. Additionally, AFE rectifiers can be employed in electric vehicle charging and discharging systems, where the ability to support bi-directional power flow is crucial [2].

A Virtual Synchronous Generator (VSG) is a control strategy of an AFE rectifier that emulates the behavior of a synchronous generator in power systems. This includes the ability to control the frequency and voltage of the grid, provide primary and secondary control, and participate in system-level ancillary services. In terms of grid stability, the VSG can help to improve the dynamic performance of power systems with high penetration of renewable energy sources and distributed energy resources (DERs). By emulating the behavior of a synchronous generator, the VSG can provide damping control to mitigate power oscillations and improve the transient stability of the grid [3].

The methodology for developing AFE rectifiers comprises real-time simulation steps to validate control concepts and ensure safe implementation with hardware. Hardware-in-the-Loop (HIL) simulation is a widely adopted technique in electrical systems for achieving real-time system responses with minimal numerical errors [4]. HIL simulation entails connecting a physical controller to a virtual plant executed on a real-time simulator instead of a physical plant. This approach is cost-effective and time-efficient, as it eliminates the need for physical test benches and allows for the testing of controller designs [5, 6].

This paper presents a methodology for rapidly prototyping a Hardware-in-the-Loop (HIL) simulator for an Active Front End (AFE) rectifier. The proposed methodology is based on the realization of both the controlled plant model and the control concept in Matlab/Simulink, and the models are optimized for code generation. The development

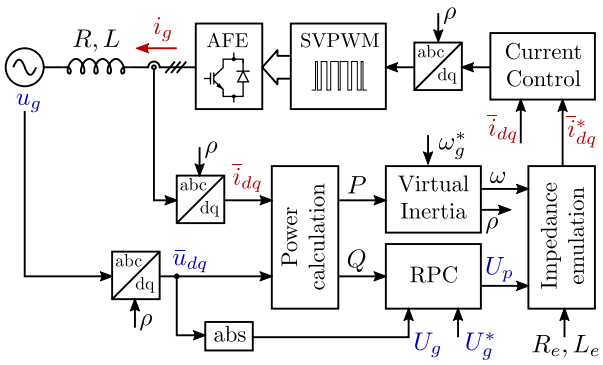


Fig. 1. Block diagram of the active front end with synchronous generator emulation.

process involves using the Embedded and Simulink coder toolboxes to generate C code from the controller model to a Digital Signal Processor (DSP). Additionally, HDL Coder generates Verilog code from the main circuit model to a Field Programmable Gate Array (FPGA). This approach enables the real-time HIL simulation of the AFE model, facilitating the validation of the control algorithms in conjunction with the controller hardware.

2. Virtual Synchronous Generator Model

Indeed, the control of a Virtual Synchronous Generator (VSG) can be divided into two main parts. The first part is the emulation of the synchronous machine dynamics, which includes the emulation of the swing equation, the regulation of real power to voltage angle, the reactive power to voltage droop, and a virtual impedance. The second part is the low level control of the AFE, which can include outer voltage and inner current controllers. The second control part receives references from the first part of the control system. There are many variants of VSG control structures, in our study the second control part contains only current control in rotating dq reference frame. The block diagram of the system is presented in Fig. 1.

Integrating the swing equation which describes the overall mechanical dynamics of the synchronous machine and the turbine, the mechanical speed of the virtual machine is obtained as

$$J\frac{d\omega_m}{dt} = \frac{P_m - P}{\omega_m} \quad \Rightarrow \quad \omega_m \cong \frac{1}{M}\int (P_m - P)\,dt \qquad (1)$$

where J is the total inertia of the synchronous machine and the turbine, P_m is mechanical power and P is the active power produced into the grid. Since $\omega_m \cong \omega^*$, the difference between the reference and the actual speed is small, the inertia constant $M = \omega^* J$. The turbine provides the active power of the system and at the same time ensures the mechanical damping through the proportional control of the mechanical speed:

$$P_m = K_P(\omega^* - \omega_m) \qquad (2)$$

and finally the angle ρ needed to the dq transformations can be obtained by integrating ω_m. K_P ensures the planned frequency droop of the VSG. The discrete-time model of the mechanical subsystem can be seen in Fig. 2. The sampling time T_s is typically the period of the switching frequency or the half of it, but the calculation of the mechanical equation can be organized into a task running with larger sampling time.

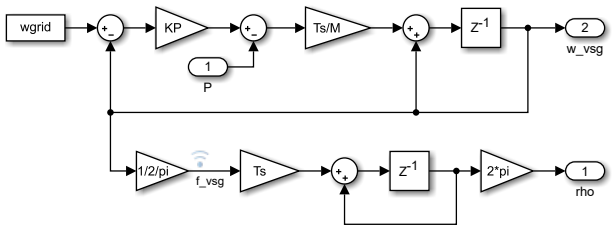


Fig. 2. The inertia model of the turbine&generator.

The voltage balance at the grid side is

$$\bar{u}_g = -\underbrace{(R_g - R)}_{R_e}\bar{i}_g - \underbrace{(L_g - L)}_{L_e}\frac{d\bar{i}_g}{dt} + \underbrace{\frac{d\psi_p e^{j\omega_m t}}{dt}}_{\bar{u}_p} \qquad (3)$$

where the complex vectors are calculated from the three-phase quantities by means of the Clarke transformation. L and R are the inductance and resistance of the choke at the AC side of AFE, L_g and R_g are the inductance and resistance of the emulated machine. Typically, $L_g \gg L$ and $R_g \gg R$. The magnitude of the pole voltage U_p depends on the excitation flux of the generator (ψ_p). U_p is obtained from a Reactive Power Controller (RPC) by integrating the difference of the reference and the measured reactive power obtained from the proportional voltage droop control with gain parameter K_Q (Fig. 3). The decrease of the grid voltage will inject reactive power to the grid by adjusting the magnitude of the pole voltage.

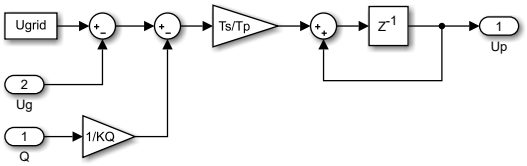


Fig. 3. Reactive power control with voltage droop.

Technically it is possible to calculate directly the voltage needed at the AC side of the AFE using eq. (3), but it is better to use inner current control loop which is capable to saturate the current instead of protection shutdown in case of overload situations. The current control is typically a proportional-integral type control implemented in dq reference frame. The structure and design of the current control loop used for the AFE can be read for example in [7].

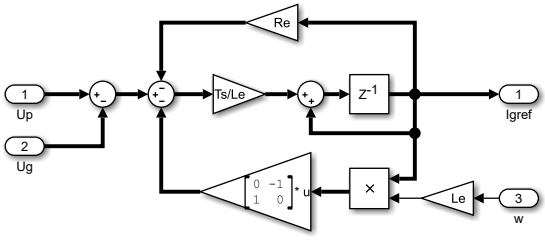


Fig. 4. Virtual impedance model of VSG in dq frame.

The reference current can be calculated for the inner loop by integrating the voltage balance differential equation:

$$\bar{i}_g^* = \frac{1}{L_e}\int \left(\bar{u}_p - \bar{u}_g - (R_e + j\omega_m L_e)\bar{i}_g\right) dt \qquad (4)$$

where all the vectors are considered as space vectors in rotating dq reference frame fixed to the pole voltage space vector $\bar{u}_p$, that is, in dq-frame $\bar{u}_p = U_p$ has only real part. Based on this equation the virtual impedance model can be constructed as shown in Fig. 4. Thick lines denote vectorial signals constructed from the d and q components.

The active and reactive power needed to the inertia model and the RPC module are calculated as the real and imagi-

nary components of the complex apparent power $\overline{S}$, respectively,

$$\overline{S} = P + jQ = \frac{3}{2}\overline{u}_g \cdot \mathrm{conj}(\overline{i}_g) \tag{5}$$

3. Simulation Results

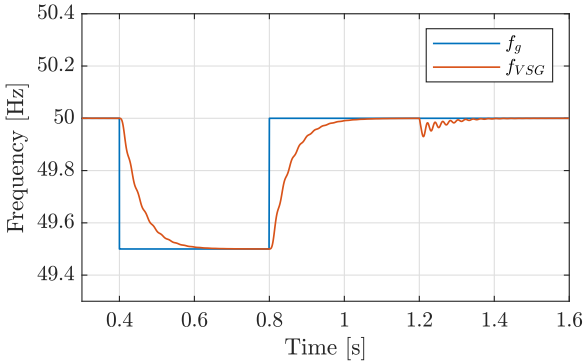
In this section the model of Virtual Synchronous Generator (VSG) is tested by off-line simulations in MATLAB/Simulink. The main parameters can be seen in Table I. The inverter is modeled with ideal switches, no dead-time effect is simulated, that is, the upper and lower switch in a converter leg are always in opposite states.

Table I. Main parameters used for the AFE model.

Name	Value
Grid peak phase voltage V_g	325 V
Grid frequency f_g	50 Hz
Choke inductance L	1 mH
Choke resistance R	40 mΩ
Switching frequency f_{sw}	10 kHz
DC bus voltage U_{dc}	600 V
VSG inductance L_g	10 mH
VSG resistance R_g	400 mΩ
Inertia constant M	20 kg · m^2/s
Frequency droop $2\pi \cdot K_P$	20 kW/Hz
Voltage droop K_Q	2 kVAr/V
RPC integral time T_p	3 ms

The signals shown in Fig. 5 are calculated to analyze the system behaviors for the grid frequency and peak voltage step responses. The grid frequency decreases at time 0.4 s by 0.5 Hz which is followed by the virtual synchronous generator (Fig. 5(a)). This transient represents an active power P demand on the grid which is balanced by the VSG. It can be seen in Fig. 5(b), that the frequency droop generated 10 kW active power as it was designed by the gain K_P. The reactive power Q only changes during the transient state, as soon as the VSG frequency f_{VSG} settles down to its steady-state at time around 0.6 s, Q tends to zero. Since the dq-frame is fixed to the pole voltage of the generator model and the emulated inductance L_g is relatively large, the q direction current is not zero (Fig. 5(c)). Due to the large L_g, the magnitude of the virtual pole voltage is also increased during the frequency droop interval, not only the angle between the grid and the pole voltage vector is responsible for the active power as shown by Fig.5(d).

At time 1.2 s, the peak of the grid voltage is decreased by 5 V corresponding to 10 kVAr reactive (inductive) power generated by the VSG, as follows from the gain K_Q. The increase of the pole voltage is more relevant in this case. Since the effect of L_g is much smaller, mainly q direction current is generated, that is the angle between the pole volt-



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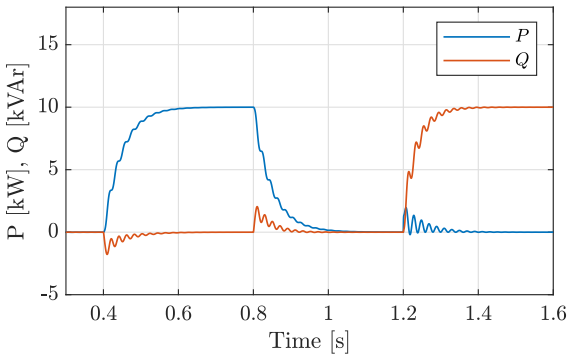

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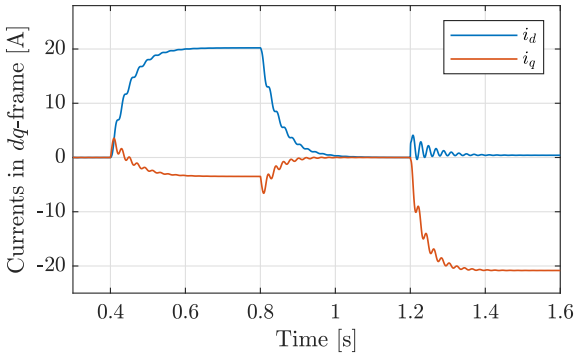

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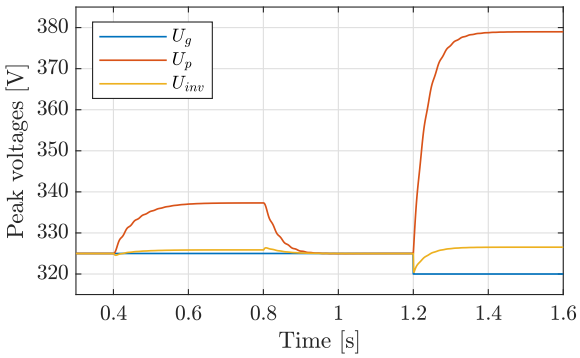


(d)

Fig. 5. Step responses for 0.5 Hz grid frequency and 5 V grid peak voltage droop. (a) Grid frequency and the VSG frequency. (b) Active and reactive power. (b) Grid side currents in dq-frame. (d) Peak values of grid voltage, VSG pole voltage and the inverter voltage.

age vector and the grid voltage vector is small, only caused by the voltage drops on the resistive parts of the impedancies.

The dynamic behaviors in Fig. 5 are set experimentally. The parameters has cross effects, but the active power and the frequency response is mainly tuned by the inertia constant M, while the reactive power and pole voltage transient response by T_p. The virtual inductance L_g has effect both on active and reactive components, it is tuned together with the virtual resistance R_g to ensure stability. The small oscillations during the transient phases can be suppressed by the increase of R_g.

The steady-state currents in the active and in the reactive power intervals are presented in Fig. 6.

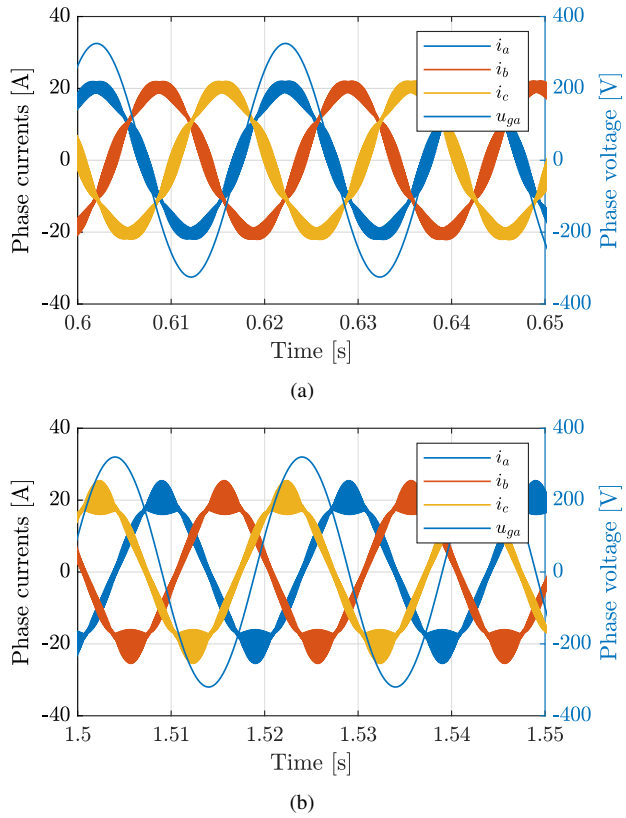


Fig. 6. Steady-state AC side phase currents. (a) Active power (a) and reactive (inductive) power is generated by the VSG.

4. HIL Platform

Fig. 7 illustrates the hardware environment used for the real-time Hardware-in-the-Loop (HIL) simulation of the system. The low-cost HIL simulator platform is partially built using commercial components, such as the Digilent Zybo board with a Xilinx Zynq-based FPGA, which is used to emulate the high-power parts or the Texas Instruments LaunchPad with F28379D dual core Digital Signal Processor (DSP) used for the control parts. Most of the HIL system is custom-made, providing 16 sigma-delta modulator based analog channels, 24 general purpose programmable digital IOs for transmitting gate signals for the power converter models or other fast logical signals, and 8 low-speed digital inputs and 8 outputs implemented by serial communication based port extension.

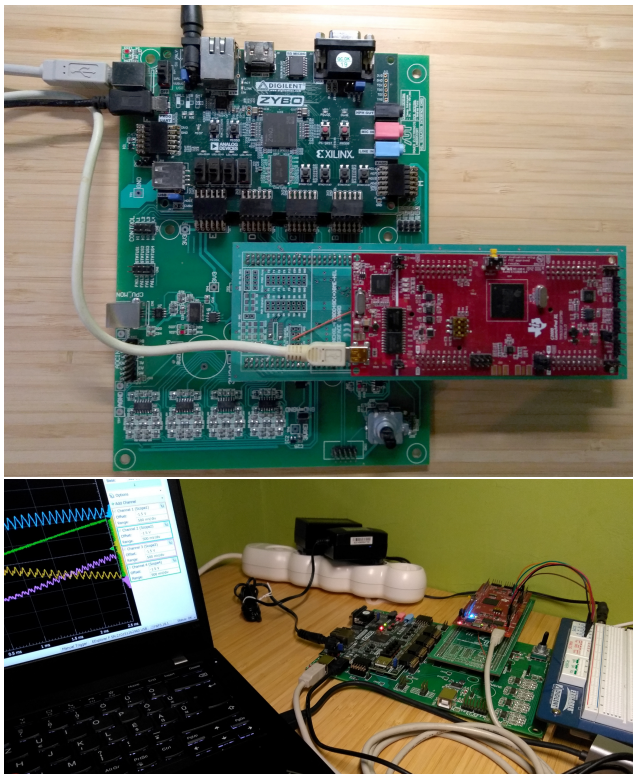


Fig. 7. The HIL hardware environment

The AFE rectifier's main circuit model and its control components are developed in Matlab/Simulink, but Xilinx Vivado tools and Texas Instruments Code Composer Studio are required to compile the Matlab-generated projects. The complete code generation workflow is run from Simulink, but software components written in C and Verilog files, both at the DSP and FPGA side, respectively, are needed to prepare a fully automatized code-generation workflow. These hand-written code components typically include communication interfaces and monitoring tools. A custom-made terminal program is dedicated to both embedded devices, the DSP and the FPGA. This software allows for recording time evolution of variables and real-time modification of parameters.

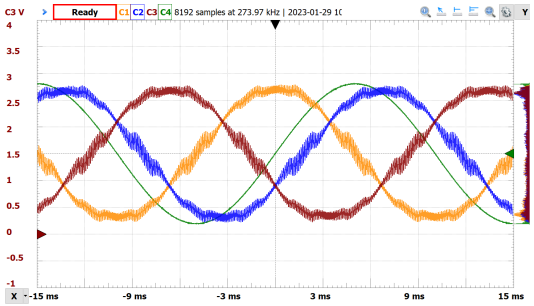
Discrete-time forward Euler integrators are used with a 40 ns time step to calculate the state variables. The fixed-point data types are adjusted to the FPGA hardware capabilities. Since the FPGA has 18×25-bit multipliers, a practical selection for the word length of variables is 25 bits and 18 bits for the gain parameters. The inner variables of integrators require a more significant word length and fractional part, as small values need to be accumulated and underflow error need to be minimized. While it is possible to use floating-point data types, which would be much simpler, it would result in a more larger time step, limited to the microseconds or tens of microseconds range.

5. Real-time Simulations

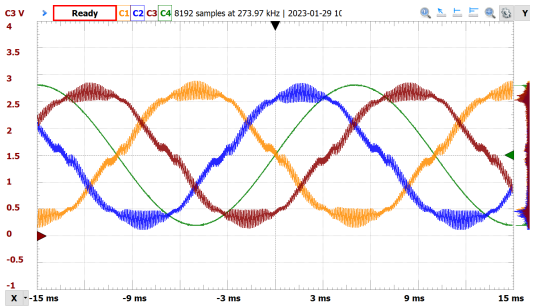
Real-time simulations are presented in this section to validate both the HIL main circuit model and the control. First

the current control loop is studied, then the control extended with the virtual synchronous generator model. In the real-time model, most design considerations must be made as in the real system. The analog channels need calibrations, there are offset and gain errors, the signals are loaded with noise. Especially the grid voltage measurement in the VSG system must be well calibrated to avoid the continuous generation of reactive power.

Fig. 8 illustrates the three-phase current time functions, and a grid line voltage in steady-state. The signals are acquired at the analog output channels of the HIL simulator by the digital oscilloscope of a Digilent Electronics Explorer board using the Waveform software. Oscilloscope channels C1, C2, C3 depict the grid phase currents a, b and c, respectively, and the signal of line voltage $u_{gA} = u_{gb} - u_{gc}$ is connected to channel C4. The 3 V full-scale of analog channels corresponds to ±25 A for currents, ±650 V for line voltages, and 1000 V for the DC link voltage.



(a)

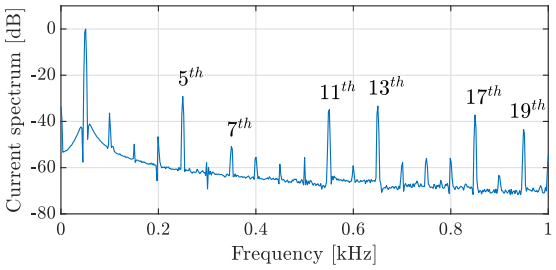


(b)

Fig. 8. The output currents recorded at the analog channels of the HIL (dead-time is 2 μs). (a) Active ($I_d^* = 20$ A) and (b) reactive (capacitive) currents ($I_q^* = 20$ A).

Fig. 8(a) and 8(b) shows situations when the grid side power is purely active or reactive, respectively. The real-time model appears to be functioning as expected. Note, that line voltage u_{gA} lags the phase voltage u_{ga} by 90°. The current shapes are similar to the off-line simulation case shown in Fig. 6, except that 2 μs dead-time is also emulated, and the control side does not try to compensate it. The distortion of phase currents are investigated further by calculating frequency spectra (Fig. 9). The typical low frequency harmonics components can be observed. In the reactive power case, the 7^{th} harmonics is increased while the 11^{th} and 13^{th} harmonics are decreased compared to harmonics of the active power case.

Testing the dynamics of current controller, the d-direction



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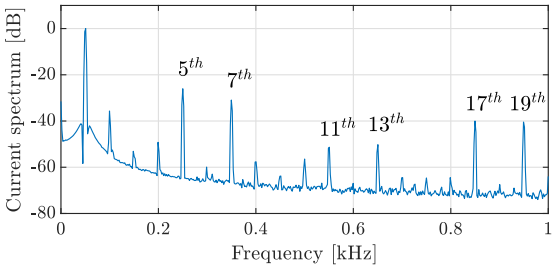
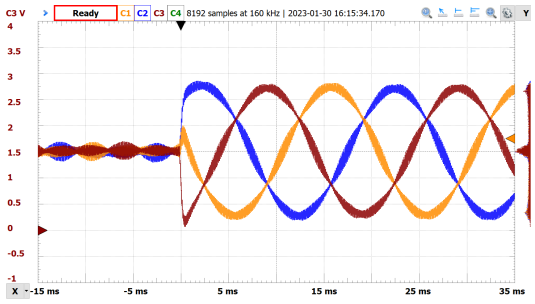


(b)

Fig. 9. Low frequency spectra of phase currents (dead-time is 2 μs). (a) Spectrum of active ($I_d^* = 20$ A) and (b) reactive current ($I_q^* = 20$ A).

reference current jumped from 0 to 20 A (Fig. 10). In this case almost ideal conditions are used, the dead-time and the choke resistance are set to zero, and the DC voltage is large enough (700 V) not to saturate the current controller. Fig. 10(a) presents the phase current signals at the analog side, while signals are captured in a four-channel recorder embedded into the DSP control code (Fig. 10(b)).



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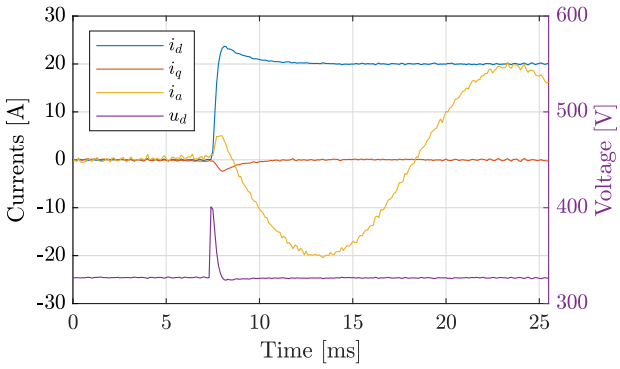

(b)

Fig. 10. Step response of $I_d^* = 20$ A with ideal conditions (dead-time is zero, $U_{DC} = 700$ V, $R = 0$). (a) Analog phase current signals. (b) Signals recorded by the controller.

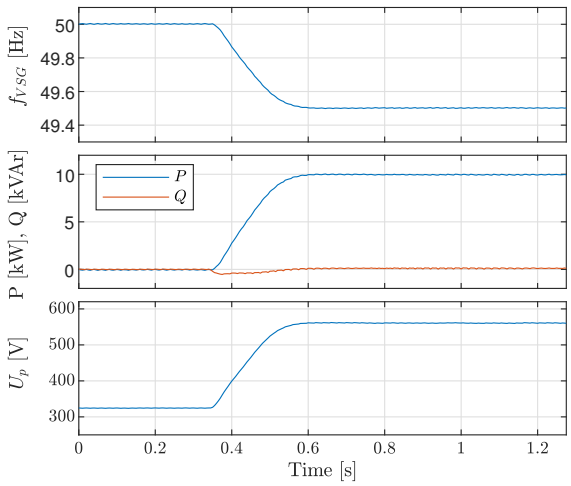

Fig. 11. Frequency droop response of VSG in the real-time HIL system.

The PI current control is designed for $\sim 60^\circ$ phase margin with $T_s = 1/f_{sw}/2$. The proportional and integral gains are $K_P = 3.49$ and $K_I = 0.107$, respectively. The algorithm runs at both peaks of the PWM triangular carrier signal. Since the sampling is synchronized to the PWM, the current ripple in phase current i_a is eliminated in Fig. 10(b), only small ripples caused by noise in the measurement can be observed. The transient of i_d is about as expected. The overshoot reflects a bit smaller phase margin, the reason is that two consequent current samples are averaged, but this delay is not considered in the design of the PI gains. The small transient in the q direction current is due to that decoupling between the d and q channels was not applied during the test. In the transient of u_d a peak can be seen during the actuation, the steady-state of voltage u_d is the same. Since both the dead-time and the choke resistance are zero, no additional voltage drop in d direction, only the 325 V grid voltage. The transient change of u_d is around 75 V, which comes from the product of the change of the current and the proportional gain.

The response of the VSG system recorded at the DSP side is shown in Fig. 11. The frequency of the grid steps from 50 Hz to 49.5 Hz. It can be seen the frequency of the VSG follows this change. Most of the signals are similar to the off-line simulations shown in Fig. 5, the active power tends to 10 kW according to the frequency droop parameter while the reactive power stays at zero. However the virtual pole voltage U_p is much larger at this operating point, since for stability reason both the virtual resistance and inductance are increased. In order to reach these smooth transients, additional filters are used in the grid voltage measurement and the power calculations. These filters change the stability borders, and required to modify the virtual impedance.

6. Conclusions

A HIL simulation framework has been developed for real-time testing of the AFE rectifier control algorithms. The model-based system development is supported by automatized code-generation. Both the main circuit HIL model and the embedded control are generated from Simulink models. The operation and current control of the AFE model were demonstrated, the system exhibited realistic behaviors, e.g. the deadtime effects are presented that may help developing deadtime compensation algorithms, harmonic elimination techniques.

The dq-frame current control is extended by a virtual synchronous generator model to serve active and/or reactive power demand of the grid from energy storage and/or renewable sources. The frequency and voltage droop characteristics of the system is studied in off-line simulation and in the HIL system. The real-time VSG control required precise voltage calibration and needed to use additional filtering, which influenced the selection of virtual impedance parameters.

In future plans, the main circuit model needs to be extended with ac side capacitor and grid impedance to obtain more realistic system behaviors. Similarly the dc side ideal voltage source also need further development both in the HIL model and in the control.

Acknowledgments

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References

[1] M. Gendrin, J.-Y. Gauthier, and X. Lin-Shi, "A Predictive Hybrid Pulse-Width-Modulation Technique for Active-Front-End Rectifiers," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5487–5496, Jul. 2017.

[2] A. Zhaksylyk, H. Rasool, E. Abramushkina, S. Chakraborty, T. Geury, M. El Baghdadi, and O. Hegazy, "Review of Active Front-End Rectifiers in EV DC Charging Applications," *Batteries*, vol. 9, no. 3, p. 150, Mar. 2023.

[3] J. Chen, M. Liu, C. Oloughlin, F. Milano, and T. Odonnell, "Modelling, Simulation and Hardware-in-the-Loop Validation of Virtual Synchronous Generator Control in Low Inertia Power System," in *2018 Power Systems Computation Conference (PSCC)*. Dublin: IEEE, Jun. 2018, pp. 1–7.

[4] A. D. Benhamadouche, F. Djahli, A. Ballouti, and A. Sahli, "FPGA-based hardware-in-the-loop for multi-domain simulation," *International Journal of Modeling, Simulation, and Scientific Computing*, vol. 10, no. 04, p. 1950020, Aug. 2019.

[5] T. Kokenyesi, Z. Suto, and I. Varjasi, "Multilevel Validation Method for Hardware-in-the-Loop Simulation Models," in *2018 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, Jun. 2018, pp. 1346–1351.

[6] E. Monmasson, L. Idkhajine, I. Bahri, M.-W. Naouar, and L. Charaabi, "Design methodology and FPGA-based controllers for Power Electronics and drive applications," in *2010 5th IEEE Conference on Industrial Electronics and Applications*, Jun. 2010, pp. 2328–2338.

[7] M. M. R. Chowdhury and Z. Sütő, "Validation of real-time simulation model of a three-phase Active-Front-End (AFE) rectifier," in *2022 8th International Youth Conference on Energy (IYCE)*, Jul. 2022, pp. 1–5.