A Novel Frequency and Positive Sequence Detector for Utility Applications and Power Quality Analysis

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Abstract – Based on multi-dimensional representation and vector calculus definitions, this paper proposes two novel and quite simple algorithms for utility applications and power quality analysis. The first one is a synchronizing procedure, based on a digital PLL (Phase Locked Loop). Its design and dynamic behavior are analyzed for single and three-phase systems. The second one is a positive sequence detector, which uses the proposed PLL to ensure that the positive sequence components can be calculated even under distorted waveform conditions or frequency variations. Since it is not based on *Fortescue*'s classical decomposition and no special input filtering are needed, its dynamic response may be as fast as one fundamental cycle. In order to validate the proposed models, simulations are shown and experimental results were obtained by means of a DSP-based system and a prototype of Power Quality Monitor. Furthermore, the PLL algorithm was implemented in a selective active filter to confirm the expectations in a closed-loop application.

Key words: Phase-locked loop, frequency detection, synchronization, fundamental component identification, positive sequence extraction.

1. Introduction

Accurate and fast detection of the utility mains frequency and fundamental positive sequence components are of great interest for power systems control and analysis. For correct action, the controllers of most electronic equipments, such as power systems relays, active power filters, uninterruptible power supplies (UPS), controlled rectifiers, FACTS devices, etc, must be synchronized with the fundamental frequency of the utility voltage [1-10]. In addition, various power quality indices and conformity factors should be based on the evaluation of the fundamental positive sequence [11-12].

For this reason, different algorithms and circuits have been proposed in the last years to provide the necessary information about the fundamental waveform. Fast dynamic response, accuracy and robustness in presence of harmonics or transients have been the most important issues to deal with.

A. Fundamental Frequency Identification

The methods of frequency identification are usually derived from zero crossing techniques, adaptive discrete Fourier transform, demodulation techniques and phase-locked loop (PLL) systems [1-3]. Each of these methods presents advantages and disadvantages, depending on the final application, utility disturbing conditions and the characteristics of the digital system on which they are implemented.

Originally the PLL systems were derived from the classical feedback control structure using a phase detector, a voltage controlled oscillator (VCO), a low-pass filter and a comparator. Their use in a vast sort of different applications showed useful results in electronic devices, power system control and communications networks [3]. However, the recent and increasing use of digitally processed systems have pointed to the necessity of an improved digital PLL design, best suited for this new context.

In the case of power system analysis and control, the most promising approaches have been derived from instantaneous power definitions [6,9,10]. However, although these methods are quite simple to implement, since they use some analogies to the instantaneous power concepts [12,15,16], they could lead to misinterpretation by those not familiarized with such relatively new concepts.

So, the first aim of this paper is to discuss a methodology to design and analyze two new PLL structures, for single and three-phase applications. In our approach, the power concepts are not necessary, making their comprehension easer not only for power system's engineers, but also for anyone interested in frequency identification methods.

The proposed digital PLL algorithm is based on instantaneous vector calculation. The PLL structure derives from inner (scalar or dot) product and properties of orthogonal functions. Since the precision and dynamic behavior of the PLL is extremely dependent on its

proportional-integral (PI) regulator, the design and practical aspects of implementing such regulator are also discussed. Simulation and experimental results validate the model.

B. Fundamental Positive Sequence Detector

Regarding the fundamental positive sequence calculation, the most frequent techniques are based on some time domain adaptation of the *Fortescue´*s decomposition [14] or on some kind of voltage peak detector [1,4,12,13].

Nevertheless, most of them are derived presuming purely sinusoidal grid voltages and do not work properly if facing distorted waveforms [4]. Some techniques also propose filtering the measured voltages in order to identify the fundamental component and calculate the positive sequence. Although, if such filters are not self adjustable to frequency variations, these techniques can be completely ineffective [1,8,12].

The second goal of this paper is to present a novel positive sequence detector, which is based on the proposed digital PLL and simple additional algebraic manipulation of the measured voltages. Since the PLL is used, the method is insensitive to frequency deviations and is quite robust to noisy utility conditions. Besides, even not been derived from *Fortescue´*s transform, its results are equivalent to those for sinusoidal steady state conditions.

2. Multi-dimensional representation and vector calculation

More and more multi-dimensional representation and vector calculus have been used in modern electrical networks analysis [15,16], particularly due to their general and well-stated mathematical basis. Accordingly, this paper deals with the definitions of inner product and orthogonality of instantaneous multi-variable vectors, in order to explain the new PLL model and the positive sequence detector.

A. Instantaneous Inner Product

According to [17], the inner product (·) of two n-dimensional instantaneous vectors $\boldsymbol{v} = [v_1\ v_2 \ldots v_n]$ and $\boldsymbol{u} = [u_1\ u_2 \ldots u_n]$ consists of summing up the products of terms with similar index in both vectors. Thus:

$$\boldsymbol{v} \cdot \boldsymbol{u} \equiv [v_1\ v_2 \ldots v_n] \cdot [u_1\ u_2 \ldots u_n] = \\ = v_1.u_1 + v_2.u_2 + \ldots v_n.u_n = \sum_{l=1}^{n} v_l.u_l \quad . \qquad (1)$$

Hence, considering tri-dimensional vectors (e.g. three-phase power system voltage or current signals), the resulting instantaneous inner product would be:

$$\boldsymbol{v} \cdot \boldsymbol{u} = [v_a\ \ v_b\ \ v_c] \cdot [u_a\ \ u_b\ \ u_c] = \\ = v_a.u_a + v_b.u_b + v_c.u_c = \sum_{l=1}^{n} v_l.u_l \quad . \qquad (2)$$

B. Orthogonality Definition

Two non-zero vectors are called orthogonal ($\perp$) over the interval $t_1 \le t \le t_2$, with respect to a strictly positive weight function $w(t) > 0$, if and only if [17]:

$$\boldsymbol{v} \perp \boldsymbol{u} \ \Leftrightarrow \ \int_{t_1}^{t_2} w(t).[\boldsymbol{v}(t) \cdot \boldsymbol{u}(t)].dt = 0 \, . \qquad (3)$$

If the weight function is assumed to be the inverse of the integration interval i.e. $w(t) = 1/(t_2-t_1)$ then (3) states that the mean dot product ($\overline{\cdot}$) of orthogonal signals is always zero, independently of their relative amplitudes:

$$\overline{\boldsymbol{v} \cdot \boldsymbol{u}_{\perp}} \equiv \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} [\boldsymbol{v}(t) \cdot \boldsymbol{u}(t)].dt = 0 \, . \qquad (4)$$

In the case of periodic signals, such as trigonometric functions, the orthogonality condition applies to the function period *T*:

$$\overline{\boldsymbol{v} \cdot \boldsymbol{u}_{\perp}} \equiv \frac{1}{T} \int_{t}^{t+T} [\boldsymbol{v}(t) \cdot \boldsymbol{u}(t)].dt = 0 \qquad (5)$$

and, considering a digital implementation, expression (5) could be represented by the discrete summation:

$$\overline{\boldsymbol{v} \cdot \boldsymbol{u}_{\perp}} = \frac{1}{T} \sum_{k-m\Delta}^{k} \left[\sum_{l=1}^{n} v_l(k).u_l(k) \right] = 0 \, , \qquad (6)$$

where "Δ" is the sampling interval and "*m*" is the number of samples per period ($T = m\Delta$).

In the signal processing area, the previous expression can also be seen as a moving average filter [18], which is quite simple to implement and represents a robust and efficient approach to calculate the mean value of time domain vectors (variables).

3. Digital PLL using Inner Product Model

The aim is to introduce a PLL design methodology valid for single and three-phase (uni or multi-dimensional structures) power system's applications, without using the instantaneous power concepts [6,9,10]. So, next section starts with the single-phase model.

A. Single-Phase PLL Model

The proposed PLL is shown in Fig. 1 and the central idea is to synthesize a unitary sinusoidal function ($u_{\perp}$), which is orthogonal to the input fundamental voltage (v) under steady conditions. Thus, the dot product result (dp) of this digitally synthesized function with the input voltage must converge to zero mean value. The instantaneous argument θ, used to synthesize the sinusoidal function $u_{\perp}$, is obtained by integrating the PI regulator output ω. While the PLL algorithm seeks to

synthesize the unitary sinusoid to satisfy the orthogonality condition with the input voltage *v*, the PI controller converts the product error (dp_{error}) into a varying correction term ($\Delta\omega$) that leads to the desired input signal frequency ω, used to render the argument function θ by simple integration.

A feed-forward reference ($\omega_n = 2p\ f_n$) may be included to improve the initial dynamic performance, where f_n is the utility nominal frequency. Since the interest is to develop a digital PLL, a sampling delay function may be added to the PLL model in order to represent the sampling process (sampling time T_{sa}). The PI regulator reaches a constant output ω if the mean input error is zero ($\overline{dp_{error}} = 0$). At this condition $q = \omega.t$ and the PLL tracks the input voltage frequency ω, with a phase-angle delay of $\pi/2$, which guarantees the orthogonality condition. Hence, the PLL is able to provide the utility's varying frequency and the synchronizing angle ($f = q + p/2$).

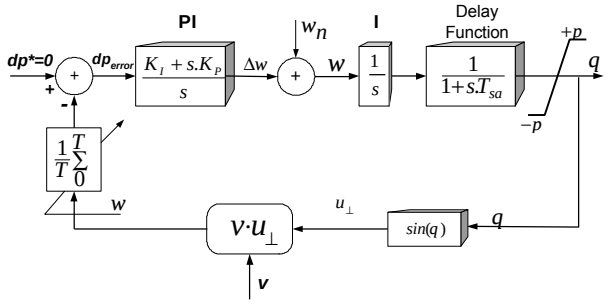


Fig. 1 – Generalized Single-Phase PLL Model.

1)Adaptive Moving Average Filter:

In order to ensure the orthogonality condition, the moving average filter (5-6) should be self-adjustable to the fundamental period and can be represented in the *Laplace*'s domain as follows:

$$\overline{dp} = \frac{1}{T}\int_0^T dp(t)dt\ , \qquad (7)$$

where T is the input fundamental period, which is dependent of the instantaneous evaluated angular frequency (ω).

Considering the filter impulse response as $h(t)$ and using the convolution property (*), its output should be:

$$dp(t) * h(t) = \int_{-\infty}^{\infty} dp(t)h(t-t)dt\ . \qquad (8)$$

Comparing (7) and (8), it is possible to notice that $h(t)$ corresponds to a rectangular pulse defined between 0 and T, with amplitude equal 1/T, i.e.:

$$h(t) = \frac{1}{T}[u(t) - u(t-T)]\ , \qquad (9)$$

where $u(t)$ is the unit step function.

Thus, the moving average filter can be represented as:

$$H_{filter}(s) = \frac{1-e^{-sT}}{sT}\ . \qquad (10)$$

Using Taylor series, the non-linear filter transfer function (10) can be simplified resulting the linear approximation as in (11). And, since the values of the terms of superior order are insignificantly small at 60Hz (50Hz), they can be neglected, rendering an almost constant and unitary gain:

$$H_{filter}(s) = \frac{1-[1-sT+\frac{(sT)^2}{2!}-\frac{(sT)^3}{3!}...]}{sT} \cong 1\ . \qquad (11)$$

In order to ensure that the number of samples in the fundamental window (period) is always constant, this strategy needs to alter the window size or the sampling frequency according to the frequency variations ($\Delta\omega$).

B. Design Methodology of the PI Regulator

As mentioned before, one important point on designing the digital PLL is the correct tuning of the proportional and integral PI controller gains, which are closely related to its precision and dynamic behavior. Although several papers have discussed this problem [5-7,9,10], there is great interest on a methodology capable of providing the best tuning for both, single and three-phase application.

Assuming that the usual sampling frequencies are considerable higher than the systems bandwidth, the non-linear feedback functions of Fig. 1 can be simplified to the linear structure of Fig. 2. This is possible because small variations of θ yield the approximation $sin(\Delta\theta) \cong \Delta\theta$ [5,6]. Thus, assuming that the digital integrator and the sampling delay function represent the plant to be regulated by the PI controller, the resulting open and close-loop transfer functions, including the controller and the plant become, respectively:

$$H_{OL}(s) = PI(s)\cdot H_{plant}(s) = \left(\frac{K_I + s.K_P}{s}\right)\cdot\left(\frac{1}{s}\right)\cdot\left(\frac{1}{1+s.T_S}\right)$$

and

$$H_{CL}(s) = \frac{H_{OL}(s)}{1+H_{OL}(s)} = \frac{K_p s + K_i}{s^3 T_S + s^2 + K_P s + K_I}\ . \qquad (12)$$

The resulting third-order system should ideally be

controlled with fast time response, good dynamic performance and small steady-state error. It should also be robust under transients and noisy input signals. However, in practical applications this tuning is very difficult to prescribe, the designer may choose to focus on the most important features of the particular project.

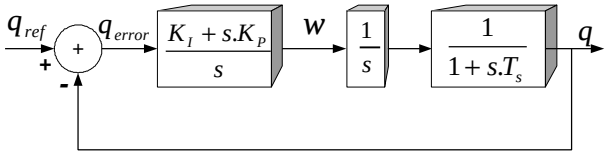


Fig. 2 - Simplified PLL model.

Different tuning methods can be applied [5,9] and, with the assumption of small sampling delays, the third order system (12) could be reduced to the *canonical form of second order system* (13), without affecting the control capabilities [19]. Such consideration is possible since the pole relative to the sampling delay, placed in the left side of the s-plane, is far from the origin and the other two dominant poles.

$$H_{CL}(s) = \frac{2\xi w_n s + w_n^2}{s^2 + 2\xi w_n s + w_n^2} = \frac{K_p s + K_i}{s^2 + K_P s + K_I} \quad . \qquad (13)$$

If the gains of the PI regulator are designed according to (13), then $K_P = 2\xi w_n$ and $K_I = w_n^2$, where w_n is the *closed-loop* crossover frequency and ξ is the damping factor (usually in the range 0.5 to 1).

C. Three-Phase PLL Model

Frequency-tracking requirements are also quite common in three-phase applications, so, it is suited to modify the previous structure in order to ensure that it works in such systems. This is possible using the multi-dimensional approach described in (2) and depicted in Fig. 3.

Furthermore, the three-phase model leads to the same expressions of the single-phase case and the plant, open loop and close-loop transfer functions yield identical (the simplified three-phase structure is equal to that presented in Fig. 2). Thus, all previously discussed procedure for tuning the PI regulator is valid for both models, as well as the stability and dynamic analysis.

However in this case, the very convenient characteristic of automatically rendering constant inner product can be achieved in balanced sinusoidal voltage conditions, even without using the moving average filter. The mean filter may also be neglected if the voltage's distortion or unbalances were not very high, since the filtering capability of the PI regulator itself ensures a good performance of the PLL.

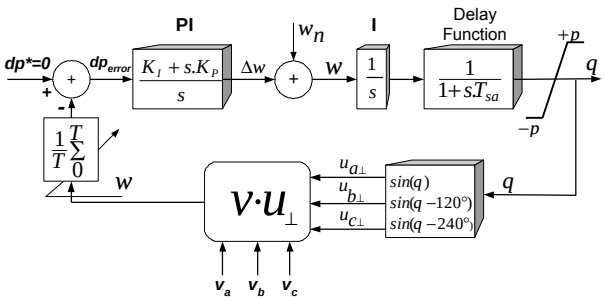


Fig. 3 -Three-phase digital PLL using instantaneous inner product of orthogonal functions.

D. Measured Voltage Conditions

Since the measured voltages are the only input data of the PLL, it is rather important to know how their conditions can affect the PLL performance or the PI tuning design.

Such analysis has to consider the variations of the mean inner product, regarding to different voltage conditions:

1) Sinusoidal and Balanced Voltages:

If the input signals constitute a balanced, three-phase sinusoidal voltages set ($\boldsymbol{v} = [v_a \; v_b \; v_c]$), then the instantaneous dot product of such voltages and the synthetic PLL signals ($\boldsymbol{u}_\perp = [u_{a\perp} \; u_{b\perp} \; u_{c\perp}]$) converges very fast to zero mean, with a slight PI regulator action. In such situation, the PI filtering capacity is not critical.

2) Influence of Voltage Distortions:

With the presence of harmonics in the input voltage set, it is necessary to substitute vector $\boldsymbol{v}$ by the corresponding harmonic series ($\boldsymbol{v} = [\Sigma v_{ah} \; \Sigma v_{bh} \; \Sigma v_{ch}]$). Now the resulting instantaneous dot product will be time variant due to the product of different frequency components:

$$\boldsymbol{v} \cdot \boldsymbol{u}_\perp = [\Sigma v_{ah} \; \Sigma v_{bh} \; \Sigma v_{ch}] \cdot [u_{a\perp} \; u_{b\perp} \; u_{c\perp}] = \Sigma v_{ah}.u_{a\perp} + \Sigma v_{bh}.u_{b\perp} + \Sigma v_{ch}.u_{c\perp} \quad . \qquad (14)$$

As long as the fundamental (h=1) input voltages are orthogonal to the PLL sinusoidal signals, the mean value of the dot product will be zero, that is:

$$v_{a1}.u_{a\perp} + v_{b1}.u_{b\perp} + v_{c1}.u_{c\perp} = \overline{\boldsymbol{v} \cdot \boldsymbol{u}_\perp} = 0 \, . \qquad (15)$$

In this case the PLL convergence is not so smooth as in the previous case and the PI regulator action should help to filter the fast oscillations of the instantaneous product around zero mean value, while keeping a good dynamic performance and precise tracking capability of the PLL.

3) Influence of Voltage Unbalances:

If the input voltage set is unbalanced, it is necessary to substitute, for this analysis, the input vector $\boldsymbol{v}$ by the corresponding sequence components ($\boldsymbol{v}=[\Sigma v_{as}\ \Sigma v_{bs}\ \Sigma v_{cs}]$), where e.g. $v_a = \Sigma v_{as} = v_a^{+} + v_a^{-} + v_a^{0}$ is the sum of the sequence components of phase "a". In this case the instantaneous dot product will also be oscillatory around zero mean, due to the product of different sequence components.

$$\boldsymbol{v}\cdot\boldsymbol{u}_{\perp} = [\Sigma v_{as}\ \Sigma v_{bs}\ \Sigma v_{cs}]\cdot[u_{a\perp}\ u_{b\perp}\ u_{c\perp}] = \\ = \Sigma v_{as}.u_{a\perp} + \Sigma v_{bs}.u_{b\perp} + \Sigma v_{cs}.u_{c\perp} \quad (16)$$

Regarding the PI regulator design, the previous conclusions could also be drawn, for small unbalances. If large unbalances are present, the use of the moving average filter provides good dynamic behaviour and precise tracking capability at the same time.

4) Line Input Voltages:

Since the functions ($\boldsymbol{u}_{\perp}$), synthesized by the PLL, are mathematically imposed to be sinusoidal and balanced, they always sum up to zero ($u_{a\perp}+u_{b\perp}+u_{c\perp}=0$). Thus, it is possible to rearrange (2) in order to obtain the same dot product using only two-measured line voltages (17), while reducing the number of input voltage sensors for practical applications:

$$\overline{\boldsymbol{v}\cdot\boldsymbol{u}_{\perp}} = v_{ab}\cdot u_{a\perp} + v_{cb}\cdot u_{c\perp} = 0. \quad (17)$$

In addition to the comments about the input voltage conditions, it is very important to point out that such input signals should be normalized to ensure that the PLL works in a large input range. This could be done, e.g., assuming per unit values (pu).

4. Positive Sequence Detector

As previously mentioned, this paper also proposes a positive sequence detector, which is based on the described digital PLL. Shifting the PLL output angle θ by 90 degrees, we get the synchronizing angle $\phi = \theta + 90^{o}$. So it is possible to generate a set of unitary and balanced sinusoidal signals ($u_{a1}+u_{b1}+u_{c1}=0$), which are in-phase with the fundamental of the input voltages ($\boldsymbol{v}=[v_a\ \ v_b\ \ v_c]$).

$$\begin{bmatrix} u_{a1} \\ u_{b1} \\ u_{c1} \end{bmatrix} = \begin{bmatrix} sin(q+90°) \\ sin(q-120°+90°) \\ sin(q-240°+90°) \end{bmatrix}. \quad (18)$$

The inner product of the measured voltages and such in-phase unitary signals (18) yields an instantaneous variable represented by the constant value $\bar{x}$ and an oscillatory part $\tilde{x}$, as following:

$$\boldsymbol{v}\cdot\boldsymbol{u_1} = v_a.u_{a1} + v_b.u_{b1} + v_c.u_{c1} = \bar{x} + \tilde{x} \quad (19)$$

where the constant value $\bar{x}$, if correctly scaled, is the instantaneous magnitude of the positive sequence, as defined by *Fortescue* for steady conditions. Hence, the positive sequence components are defined by:

$$\begin{bmatrix} v_{a1}^{+} \\ v_{b1}^{+} \\ v_{c1}^{+} \end{bmatrix} = k.\begin{bmatrix} u_{a1} \\ u_{b1} \\ u_{c1} \end{bmatrix} = k.\begin{bmatrix} sin(q+90°) \\ sin(q-120°+90°) \\ sin(q-240°+90°) \end{bmatrix}, \quad (20)$$

with $k = \frac{2}{3}.\bar{x}$. The mean value $\bar{x}$ can be easily obtained using a moving average filter, similar to that described in section 3. Figure 4 illustrates the proposed algorithm.

Using this methodology, only the PLL and the average filter dynamics limit the dynamic response of the positive sequence detector and, as will be demonstrated, such response can be as fast as one cycle of the fundamental period.

Except for the moving average filter, the proposed technique does not need additional filtering in the measured voltages and it is immune to utility voltage's distortions, unbalances or even frequency deviations, since the PLL ensures the necessary tracking and filtering actions.

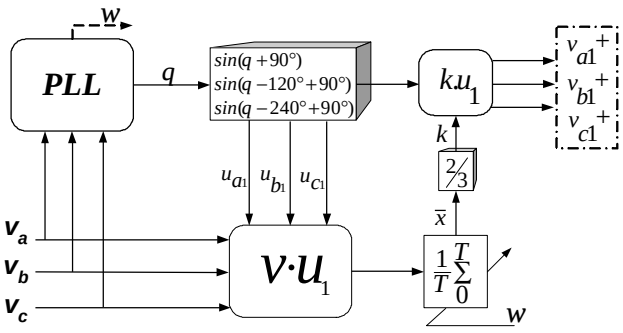


Fig. 4 – Algorithm of the Positive Sequence Detector.

A. Power Quality Indices

Several power quality indices have been proposed in order to evaluate the levels of energy deterioration or wasting in the power systems [5,7,11]. In such context, the proposed positive sequence detector could be used for example to define a symmetry index or conformity factor (21), representing the unbalance measurement of the grid voltages. This factor is also based on the vector norm $\|..\|$ concept [17].

$$fcv_1^{+} = \frac{\|\boldsymbol{v_1^{+}}\|}{\|\boldsymbol{v_1}\|} = \frac{\sqrt{\boldsymbol{v_{1a}^{+}}^{2} + \boldsymbol{v_{1b}^{+}}^{2} + \boldsymbol{v_{1c}^{+}}^{2}}}{\sqrt{\boldsymbol{v_{1a}}^{2} + \boldsymbol{v_{1b}}^{2} + \boldsymbol{v_{1c}}^{2}}}. \quad (21)$$

In balanced and sinusoidal conditions this index is unitary and decreases as the fundamental voltage unbalances increase. If the voltages are evaluated in per unit (pu) of the nominal base, then the mean value of the positive sequence index (21) is equal to the amplitude factor k defined in (20).

5. Simulation Results

Figures 5 to 7 show the performance of the single-phase digital PLL, designed with a crossover frequency (w_n=20rad/s) and ξ =0.707. In such simulation the measured input voltage presents 15% of 7th harmonic. Figure 5 illustrates the distorted input voltage (v), the digital sinusoidal function (u), which results orthogonal to the fundamental of (v) and the PLL output phase-angle (θ) in the range [0,2π]. Since the fundamental frequency was set to 60Hz, Fig. 6 shows the angular frequency convergence by the PLL (w=377rad/s) and shows the performance of the moving average filter, which is responsible for calculating the mean value of the instantaneous inner product (dp_med $\cong$ 0).

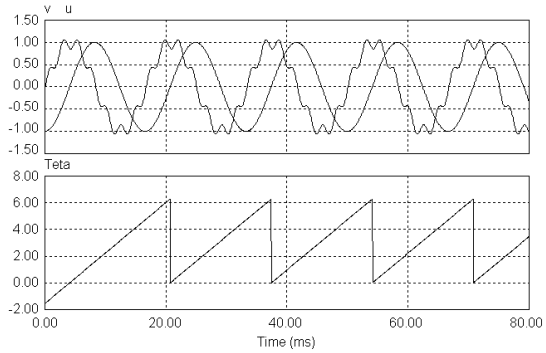


Fig. 5- Single-phase PLL: Distorted input voltage, PLL quadrature sinusoid and its argument angle θ.

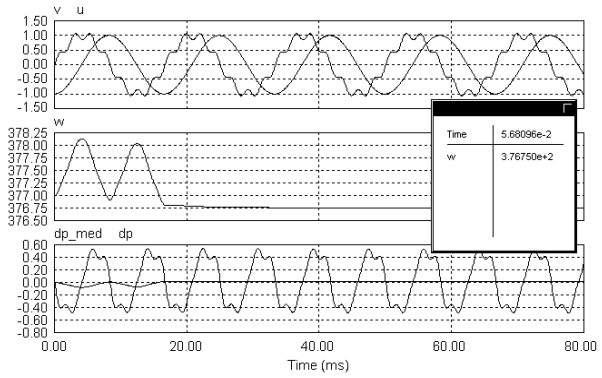


Fig. 6- Upper: input and PLL voltages. Middle: PLL frequency. Lower: input/output signals of the average filter.

Fig. 7 shows the three-phase input voltages (v_a v_b v_c) distorted by 10% with 5th, 7th, and 3rd harmonics, respectively and their fundamental amplitudes are unbalanced by 20% amplitude reduction in phase "a" and 10% increase in phase "b". Note that the PLL preserves its good performance, as long as the internal sinusoidal functions "*u*" are orthogonal to the fundamental of the input voltages "*v*", as detailed for phase "a" in the middle curves.

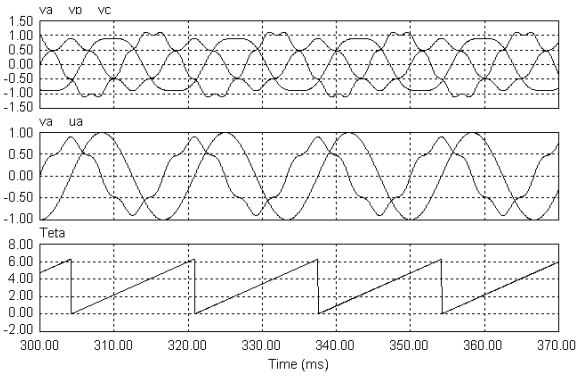


Fig. 7 - Three-phase PLL: a study case with distorted and unbalanced input voltages.

In Fig. 8, an even larger unbalance was applied to the input voltages in order to evaluate the positive sequence detector. Assuming phase "a" as the peak nominal voltage (1pu), phases "b" and "c" were set to 15% and 30% amplitude reduction, respectively.

As can be observed, in almost one cycle (16.666ms) the positive sequence scale factor converged to the expected value (in this case k = [1.0+0.85+0.7]/3 = 0.85), corresponding to amplitude of the positive sequence voltages (v_{a1}^+ v_{b1}^+ v_{c1}^+).

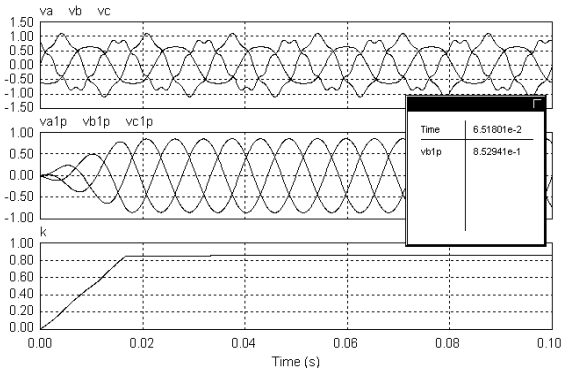


Fig. 8 – Three-phase PLL and Positive Sequence Detector: Distorted and unbalanced input voltages.

The input voltages of Fig. 9 present the same unbalance conditions of Fig. 8, but in this case without the harmonic components. After 200ms, a voltage sag of 50% was imposed. Again the PLL and the positive sequence detector converged after around one cycle.

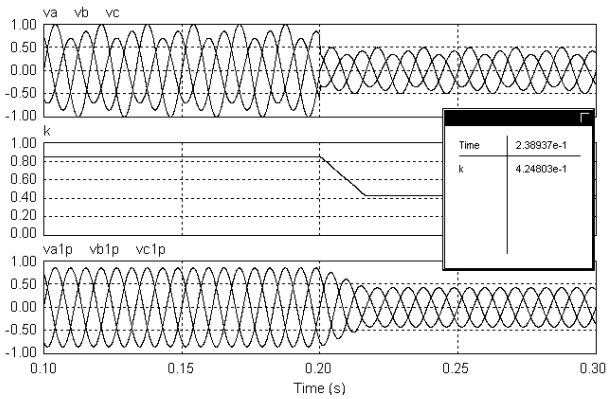


Fig. 9 – Three-phase PLL and Positive Sequence Detector during a 50% voltage sag.

6. Experimental Results

In order to validate the algorithms in practical applications, the proposed models were implemented in two different digital systems: a 16 bits fixed point DSP (ADMC401) and a prototype of Power Quality Monitoring system. The results have shown that the classical control tuning procedure (13); provides quite robust performance of the PLL for $\omega_n \cong 25$rad/s and $\xi \cong 0.7$, even with distorted and unbalanced input voltages.

Figures from 10 to 13 were obtained using the DSP system with a sampling frequency of 12kHz. Fig. 10 confirms the good performance of the PLL under sinusoidal and balanced voltage conditions, since the proposed PLL precisely tracks the power system's frequency.

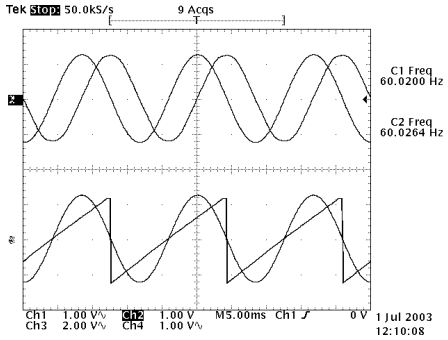


Fig. 10 – Input phase voltage, the PLL phase angle and the corresponding unitary sinusoid.

Fig. 11 shows the input voltage (lower trace) and the PLL internal sinusoid (upper trace), shifted by $+\pi/2$ in order to be in phase with the input voltage, during a frequency step (DC trace) from 50Hz to 60Hz. Note that the voltage period changes very fast from 20ms to 16.66ms (16.8ms due to the oscilloscope resolution). This test was performed using a programmable AC power source.

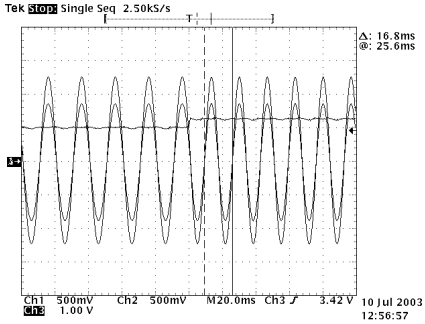
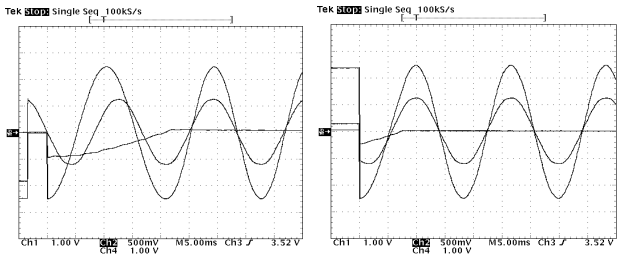


Fig. 11 – PLL action during a frequency step from 50 to 60Hz.

Figure 12 shows how the dynamic performance of the PLL is affected by the design of its PI regulator. According to the previously described method (13), as lower the crossover frequency w_n is, the better is the filtering action of the PI regulator, but in expense of the dynamic response.



(a) (b)

Fig. 12 – Input voltage, the internal in-phase sinusoid and the PI input error (a) $w_n = 23.63$ rad/s; (b) $w_n = 90$ rad/s.

In order to illustrate the PLL performance in a closed-loop power electronics application, an active power filter using selective harmonic control [20] was implemented and some results are presented in Fig. 13 (the PLL enables the necessary sampling frequency adjustment for correct action of the selective control method). The almost clean current waveform confirms that the filter tracks precisely the mains frequency.

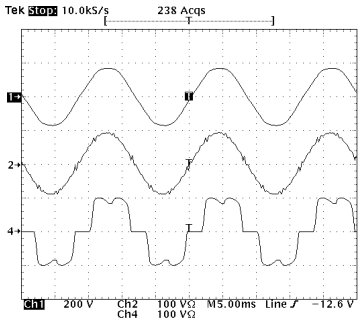


Fig. 13 – Active Filter using PLL in the selective harmonic control: line voltage, line current and load current.

Using the Power Quality Monitor (voltage mode), with a sampling frequency of 2.4kHz, figures 14 and 15 show the convergence of the positive sequence detector to unbalanced voltage sag of the input voltages without and with harmonics presence. Phases b and c were reduced abruptly from 1.0pu to 0.7pu and 0.85pu respectively. The positive sequence converged in one cycle to the expected amplitude value of k=0.85pu.

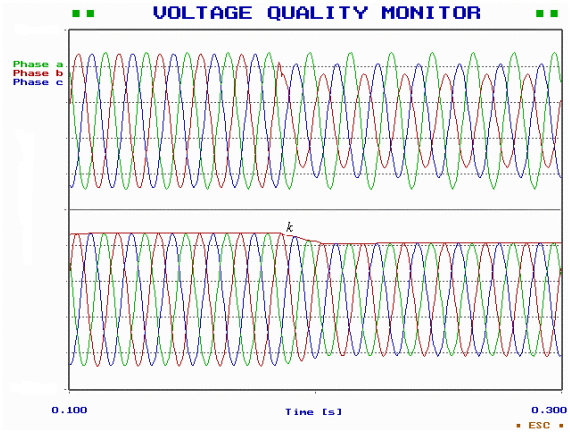


Fig. 14 –The Positive Sequence Detector during unbalanced sag - implemented in the Power Quality Monitor.

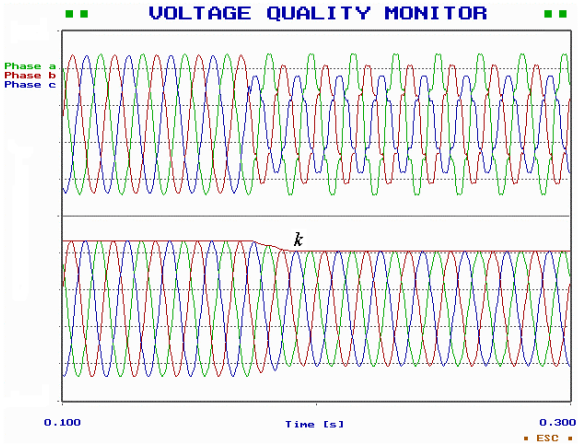


Fig. 15 – Performance of the Positive Sequence Detector, facing a unbalanced voltage sag with distortion.

7. Conclusion

This paper proposes a novel fundamental frequency and positive sequence detector, which is essentially based on a digital PLL structure, instantaneous vector algebra and moving average digital filters. The design methodology of the proposed PLL is quite simple and is valid for single and three-phase applications. The positive sequence detector is not based on the conventional *Fortescue*'s transform and thus, it is an interesting alternative to power quality analysis, due to the fast convergence and high immunity to utility distortions and unbalances. Moreover, if the PLL is used, the positive sequence detector becomes insensitive to the utility frequency deviations.

To confirm the theoretical expectations, simulation tests have shown the overall performance and the dynamic behavior of the single and three-phase PLL, along with the positive sequence detector. Experimental results, using two different digital systems were also depicted and the proposed models have shown to be very effective even in closed-loop applications, as for example, in a selective harmonic active filter, in which precise tracking of the mains frequency has been a critical issue.

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