22nd International Conference on Renewable Energies and Power Quality (ICREPQ'24)
Bilbao (Spain), 26th to 28th June 2024
Renewable Energy and Power Quality Journal (RE&PQJ)
ISSN 2172-038 X, Volume No.22, September 2024

# Measurement of half-bridge parasitic impedances using a flexible test probe

A. Llamazares[1], S. Martín-Arroyo[1] and M. García-Gracia[1]

[1] Department of Electrical Engineering
EINA, Zaragoza University
María de Luna 3 – Edificio Torres Quevedo – Campus Río Ebro – 50018 Zaragoza (Spain)

**Abstract.** The use of SiC MOSFETs in power applications allows to increase power density and efficiency because switching frequencies are higher. However, parasitic impedances are responsible for oscillations that can have negative effects.

In this paper we analyse the parasitic impedances of a half-bridge formed by a busbar PCB laminated with SiC MOSFETs. Using the distributed parameter approach, we have developed a procedure to characterize the impedance of the switching current loop responsible for the oscillations in the switching. According to the above, the conclusions obtained will be presented.

**Key words.** SiC inverter, parasitic impedance, half-bridge.

## 1. Introduction

Emerging wide bandgap (WBG) semiconductor materials, such as silicon carbide (SiC), can switch higher frequencies than silicon (Si)-based semiconductors; therefore, they allow high power densities and efficiency in inverters. Currently, there is a growing use of SiC MOSFETs for power applications. WBG semiconductors operate at higher voltages, temperatures, and switching frequencies than Si IGBTs. This allows power converters based on SiC devices to achieve higher power density, with lower heat dissipation requirements. SiC MOSFETs have lower parasitic capacities between the connections of drain, source and gate regions than their Si-based counterparts [1], which enables shorter timeframes for voltage and current switching. However, this leads to very high voltage (dv/dt) and current (di/dt) variations [2]: dv/dt reaches 88 V/ns and di/dt 4.4 A/ns for SiC MOSFETs. As a result, unwanted overvoltages and oscillations (up to 100 MHz [1]), can occur during SiC MOSFETs switching due to the excitation of the parasitic capacitance and inductance in the commutation loop. Therefore, the SiC MOSFET-based inverter design requires to minimize parasitic impedance [3]. In power switched converters like a half bridge, the commutation current loop impedance ($Z_{CCL}$) [4] depends on the parasitic impedances of the bus capacitor, SiC MOSFETs, gate drive circuits, busbars, and the tracks that interconnect these elements. Parasitic impedances are responsible for oscillations that can have negative effects limiting the designs of converters with SiC MOSFETs [5].

For an optimal converter design, it is important to have techniques to characterize parasitic impedances in the frequency domain, both in the gate circuit and in the commutation current loop, to predict oscillations and model negative effects. Parasitic impedances can be characterized experimentally or through electromagnetic simulation using different numerical methods that consider the PCB geometry and materials. For simulation estimation of parasitic impedances, there are two methods: Partial Element Equivalent Circuit (PEEC) [6],[7] and Finite Element Analysis (FEA) [4],[8]. However, these numerical methods require precise knowledge of the geometry, materials used, and their properties to obtain accurate results. Impedance in the frequency domain can be measured using an impedance analyser or a Vector Network Analyser (VNA). Both of them have been used to characterize the parasitic impedance of the switching loop in three-phase inverters [8]-[10] and parasitic impedances in low power converters. However, they require fixed test setups specifically designed for each measurement, using fixed test fixtures. This work proposes a procedure to characterize the parasitic impedances of the switching current loop $Z_{CCL}$.

## 2. Impedance measurement with VNA

### A. *Parasitic flexible test probe*

For the characterization and study of parasitic impedances in PCBs, a shielded flexible probe (Fig. 1) has been developed [11].

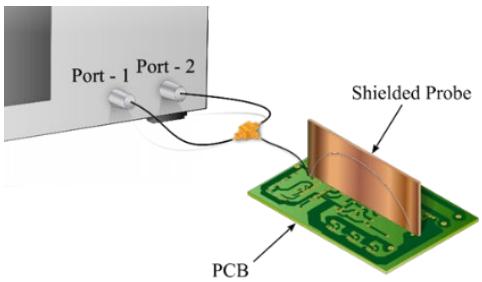


Fig. 1. Experimental setup with the flexible test probe [11].

The impedance characterization is based on a test fixture (flexible test probe) whose measuring terminals can be spaced up few cm apart. The probe consists of a pigtail coaxial cable and an RG-316/U ground coaxial that allows the return to ground of the current. The pigtail terminates in an SMA connector at one end while the other is open. The ground cable is a movable part of the probe that allows connect different points of the PCB, avoiding the need to develop a fixed test fixture for each measurement. However, the probe is located on a conductive, insulated plane perpendicular to the horizontal plane of the PCB where measurements are to be taken. The function of this conductive plane is to shield the magnetic field whose source is the current flowing during frequency scanning with the VNA. It should be noted that during calibration and measurement, both the VNA cables and the pigtail must remain in the same position to avoid unacceptable errors.

### *B. Two-port measurement with VNA*

VNA characterizes impedance in the range from hundreds of kHz to GHz, through S-parameters. The accuracy of the measurement method depends on the range of impedance measured [12]. In this work, a two-port configuration is used with the device under test (DUT) connected in shunt, allowing the characterization of low impedances (250 μΩ - 25 Ω) such as those found in PCB traces in the MHz range with a maximum error of 10%. Due to the test fixture (cables, probes, and connectors) between the VNA and measurement points, there is an error in impedance measurement which can be eliminated through a prior calibration. In this work, the SOL calibration standard has been used (short circuit (S), open circuit (O), and 50 Ω (L)).

## 3. Half bridge impedances

In the kW range, a PCB inverter uses copper planes to distribute the bus voltage in the busbar. The busbar studied in this work consists of two rectangular copper planes, parallel, with thickness *t* (35 μm), length *ℓ* (100 mm), and width *w* (50 mm) separated by the thickness of the PCB *d* (1.6 mm). This structure forms a transmission line (TL).

### *A. Busbar*

A transmission line is described by its characteristic impedance $Z_0$ and propagation constant γ

$$Z_0(\omega) = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} \tag{1}$$

$$\gamma(\omega) = \sqrt{(R' + j\omega L') \cdot (G' + j\omega C')} \tag{2}$$

where $\omega = 2\pi f$ and the parameters $R'$, $L'$, $C'$ y $G'$ are resistance, inductance, capacitance, and conductance per unit length.

The parameter $R'$ depends on the value of the skin effect frequency ($f_{sk}$) in the conductor as shown in the following relation

$$f_{sk} = \frac{1}{\sigma_{Cu} \cdot \mu_0 \cdot t^2} \tag{3}$$

$$R'(\omega) = \begin{cases} R'_{dc} & f < f_{sk} \\ R'_{ac} = R'_{dc} \cdot K_R & f \geq f_{sk} \end{cases} \tag{4}$$

where $\sigma_{Cu}$=58·10$^6$ S/m is the conductivity of copper and $\mu_0$ is the permeability of vacuum. The DC resistance $R'_{dc}$ is calculated as

$$R'_{dc} = \frac{2}{\sigma_{Cu} \cdot t \cdot w} \tag{5}$$

and $K_R$ is the AC resistance factor [13] for each conducting plane expressed as

$$K_R = \left(\frac{t}{\delta}\right) \cdot \frac{sinh\left(\frac{2t}{\delta}\right) + sin\left(\frac{2t}{\delta}\right)}{cosh\left(\frac{2t}{\delta}\right) - cos\left(\frac{2t}{\delta}\right)} \tag{6}$$

where $\delta = (2/\omega \cdot \sigma_{Cu} \cdot \mu_0)^{1/2}$ is the skin effect penetration depth.

The parameter $L'$ can be expressed as [14]

$$L'(\omega) = L'_i(\omega) + L'_e \tag{7}$$

where $L'_i$ is the internal inductance and $L'_e$ is the external one. The internal inductance $L'_i$ is due to the magnetic flux created by the current flowing through the conductor.

$$L'_i(\omega) = \frac{R'_{dc}}{\omega} \cdot K_X \tag{8}$$

where $K_X$ is the normalized reactance of each conducting plane and is expressed as

$$K_X = \left(\frac{t}{\delta}\right) \cdot \frac{sinh\left(\frac{2t}{\delta}\right) - sin\left(\frac{2t}{\delta}\right)}{cosh\left(\frac{2t}{\delta}\right) - cos\left(\frac{2t}{\delta}\right)} \tag{9}$$

the external inductance $L'_e$ originates from the surface current flowing through the conductors at very high frequencies

$$L'_e = \mu \frac{d}{w} \tag{10}$$

where $\mu$ is the permeability of the PCB equal to that of vacuum.

The inductance at sufficiently high frequencies can be approximated by $L'_e$, because $L'_i$ decreases with frequency.

The capacitance between two parallel planes $C'$ can be approximated by

$$C' = \varepsilon' \cdot \varepsilon_0 \cdot \frac{w}{d} \tag{11}$$

where $\varepsilon_0$ is the vacuum permittivity and $\varepsilon'$=4.8 is the relative permittivity of the PCB substrate.

Finally, knowing the loss tangent $tan\,\delta_e$=0.011 of the substrate, the conductance $G'$ is given by

$$G' = \omega \cdot C' \cdot tan\,\delta_e \tag{12}$$

### B. Half bridge circuit

The half-bridge circuit is shown in Fig. 2.

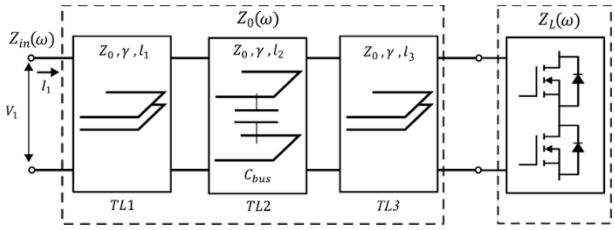


Fig. 2. The half-bridge in terms of transmission lines in cascade connection.

The busbar of the half-bridge has been divided into three cascaded transmission lines (*TL1, TL2* and *TL3*) with lengths $\ell_1$, $\ell_2$ y $\ell_3$. Section *TL1* ($\ell_1$=40 mm) connects ($V_{DC}$ to the bus capacitor $C_{bus}$. Section *TL2* ($\ell_2$=20 mm) is the busbar section in parallel to $C_{bus}$ and *TL3* ($\ell_3$=40 mm) connects $C_{bus}$ to the tracks connected to the SiC MOSFETs.

The input impedance $Z_{in}$ of a *TL* is

$$Z_{in}(\omega) = Z_0 \cdot \frac{Z_L + Z_0 \cdot tanh(\gamma\ell)}{Z_0 + Z_L \cdot tanh(\gamma\ell)} \quad (13)$$

where $Z_L$ is the equivalent load dipole and can be solved from (13) as

$$Z_L = Z_0 \cdot \frac{Z_{in} - Z_0 \cdot tanh(\gamma\ell)}{Z_0 - Z_{in} \cdot tanh(\gamma\ell)} \quad (14)$$

The switching current loop impedance $\boldsymbol{Z_{CCL}}$ is calculated as

$$Z_{CCL}(\omega) = Z_{Cbus} + Z_0 \frac{Z_L + Z_0 \cdot tanh(\gamma\ell_3)}{Z_0 + Z_L \cdot tanh(\gamma\ell_3)} \quad (15)$$

### C. Load impedance

The load dipole $Z_L$ is constituted by the elements connected to the rectangular busbar: SiC MOSFET, gate drive circuits and the tracks that interconnect them. In Fig. 3, the equivalent wye circuit of a SiC MOSFET connected with the gate circuit is shown.

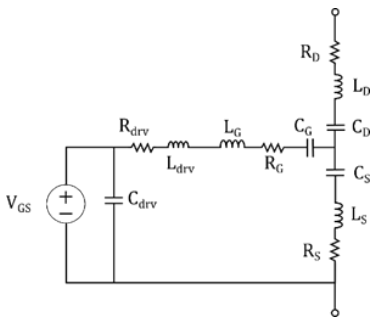


Fig. 3. SiC MOSFET circuit and gate driver assembly.

The driver impedances are: gate resistance $R_{drv}$, driver track inductance $L_{drv}$ and $C_{drv}$, the equivalent capacitance of the voltage sources $V_{GS}$. The MOSFET equivalent circuit is formed by the drain capacitances, inductances and resistances ($C_D$, $L_D$ y $R_D$), source ($C_S$, $L_S$ y $R_S$) and drives ($C_G$, $L_G$ y $R_G$). Additionally, $R_D$ and $R_S$ are of the order of mΩ and are neglected. The equivalent circuit of the SiC MOSFET and gate driver in conduction and off state are shown in Fig. 4.

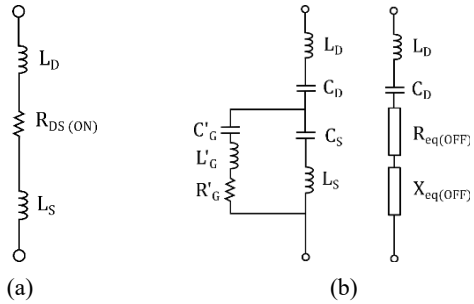


Fig. 4. Equivalent circuit of the SiC MOSFET and gate driver in conduction state (a) and off state (b).

In conduction (Fig. 4a), the conduction channel of the SiC MOSFET with resistance $R_{DS(ON)}$ is enabled, short-circuiting capacitances $C_D$ y $C_S$. The MOSFET impedance in conduction $Z_{MOS(ON)}$ is

$$Z_{MOS(ON)}(\omega) = R_{DS(ON)} + j\big(\omega(L_D + L_S)\big) \quad (16)$$

From the circuit of Fig. 4b, $R'_G$, $C'_G$ and $L'_G$ are the series equivalents between the gate terminal of the SiC MOSFET ($R_G$, $C_G$ and $L_G$) and the driver circuit ($R_{drv}$, $C_{drv}$ and $L_{drv}$). Also, the parallel impedance between the series RLC branch formed by ($C'_G$, $L'_G$ and $R'_G$) and the series RL branch formed by ($C_S$ and $L_S$) is given by $R_{eq(OFF)}$ and $X_{eq(OFF)}$. Then the equivalent series impedance of the SiC MOSFET transistor when in off state is

$$Z_{MOS(OFF)} = R_{eq(OFF)} + j\big(X_D + X_{eq(OFF)}\big) \quad (17)$$

where $X_D$ is the drain reactance formed by $C_D$ and $L_D$.

During a switching with the upper transistor (H) in conduction and the lower transistor (L) in off state (state HL=01), the resulting circuit for $Z_L$ is shown in Fig. 5. The equivalent partial inductance ($L_{CCL\_p}$)) and resistance ($R_{CCL\_p}$) of the tracks that connect to the SiC MOSFET are calculated as

$$L_{CCL\_p} = L_1 - \left(\frac{Im\{Z_{MOS(OFF)} + Z_{MOS(ON)}\}}{\omega}\right) \quad (18)$$

$$R_{CCL\_p} = R_1 - Re\{Z_{MOS(OFF)} + Z_{MOS(ON)}\} \quad (19)$$

where $L_1$and $R_1$ are the series RLC circuit inductance and resistance representing $Z_L$ and are calculated with (13) from $Z_{in}$ measurement.

## 4. Half-bridge characterization

The elements that make up the $Z_{CCL}$ switching current loop are the SiC MOSFET, $C_{bus}$, the gate driver PCB, and the half-bridge PCB. To obtain $Z_{CCL}$, SiC MOSFET, $C_{bus}$, and gate driver are characterized separately with the half-bridge unmounted. Once, SiC MOSFET and gate driver are mounted on the half-bridge PCB, but not $C_{bus}$. $Z_L$ is calculated using the measurement of $Z_{in}$ according to (14). After that, the equivalent impedances $R_{CCL\_p}$ and $L_{CCL\_p}$ are calculated form (20) and (21).

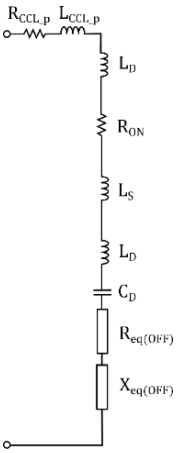


Fig. 5. Equivalent circuit of the load dipole $Z_L$ with discret elements in the HL=10 state.

### A. $C_{bus}$, SiC MOSFET and driver

$C_{bus}$ is considered to be an RLC series circuit, where ESR is the equivalent series resistance, ESL is the equivalent series inductance, and $C_{bus}$ the capacitor capacity. The impedance is obtained by using VNA.

$C_{bus}$ is measured at low frequency 5 kHz where the capacitor predominates in the impedance and a value of 29.22 µF is found. The ESL inductance (31.17 nH) is calculated at the resonance frequency ($f_s$ =166.77 kHz). The ESR is 10 mΩ and considered constant.

According to the datasheet of the used SiC MOSFET (SCTW100N65G2AG), $R_{DS(ON)}$=20 mΩ. SiC MOSFET parasitic impedances of the Table I have been characterized using a specific test setup according to the method developed in [15].

Table I. – Parasitic impedances of the SiC MOSFET

| Symbol | Description | Value | Units |
|---|---|---|---|
| $L_D$ | Drain Inductance | 1,06 | nH |
| $L_G$ | Gate Inductance | 6,76 | nH |
| $L_S$ | Source Inductance | 4,25 | nH |
| $C_D$ | Drain capacitor | 8,14 | nF |
| $C_G$ | Gate capacitor | 7,57 | nF |
| $C_S$ | Source capacitor | 2,54 | nF |
| $R_G$ | Gate resistor | 0,85 | Ω |

Gate driver characterization is done using the shunt-thru two-port method and shielded flexible probes [11]. For this, the half-bridge PCB (without mounting the $C_{bus}$ or the SiC MOSFET) is connected to a gate driver board.

After that, the shielded flexible probe is connected to the plated holes where SiC MOSFET gate (G) and source (S) terminals should be mounted as shown in Fig. 6. Measurements are done in off state.

The measured gate driver door resistance is $R_{drv}$=10.2 Ω, the power supply capacity $C_{drv}$=534 nF and $L_{drv}$=34,9 nH, which are in agreement with the designed ones.

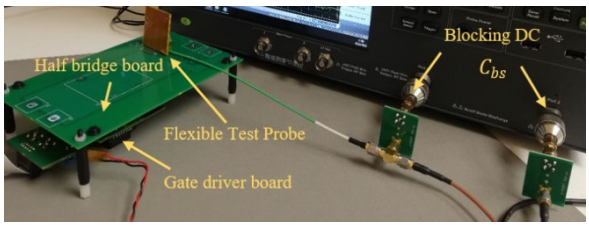


Fig. 6. Experimental setup to measure gate driver cicircuit.

### B. Characterization of the load dipole

From the measurement of $Z_{in}$ (Fig. 2), $R_1$, $L_1$, $C_1$, and $R_{CCL\_p}$ and $L_{CCL\_p}$ can be calculated. $Z_{in}$ is measured at the connection terminals with $V_{DC}$ of the half-bridge. Measurement are carried out with the shielded flexible probe. To determine the shielded flexible probe accuracy, an SMA is included as a reference. The measurement setup is shown in Fig. 7.

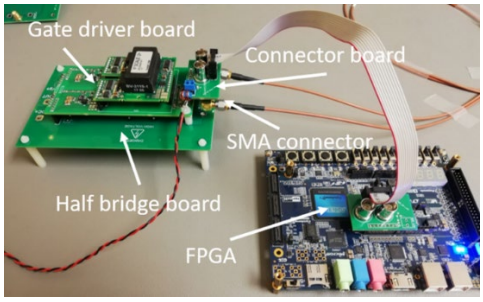


Fig. 7. Test setup for experimental characterization of the half bridge.

Fig. 8 shows the measured impedance $Z_{in}$ and Fig. 9 shows the calculated impedance $Z_L$. The measurement was made using a coaxial SMA connector, with a sweep frequency from 100 kHz to 100 MHz for the different conduction states of the half-bridge transistors (HL=00, HL=01, HL=10 and HL=11), controlled by a Cyclone V GX FPGA.

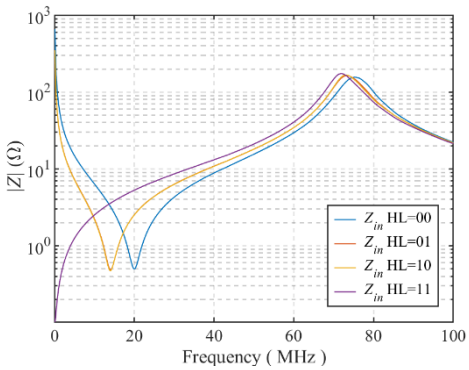


Fig. 8. Impedance $Z_{in}$ measured using a sweep frequency from 100 kHz to 100 MHz.

From the measurement of $Z_L$ and the resonance frequency $f_s$ and $C_1$; $L_1$ and $R_1$ are calculated taking into account they are the components of the series RLC circuit $Z_L$. Next, $R_{CCL\_p}$ and $L_{CCL\_p}$ are obtained using (20) and (21) at the resonance frequency $f_s$. Results obtained are shown in Table II.

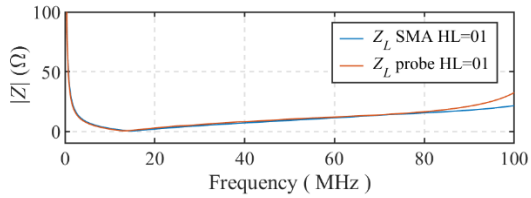


Fig. 9. Impedance $Z_L$ calculated from 100 kHz to 100 MHz.

Table II. – Measured values of the load dipole circuit (HL=01) components

| | $f_s$ (MHz) | $R_1$ (Ω) | $L_1$ (nH) | $C_1$ (nF) | $R_{CCL\_p}$ (Ω) | $L_{CCL\_p}$ (nH) |
|---|---|---|---|---|---|---|
| Probe | 13,19 | 0,514 | 32,477 | 4,483 | 0.496 | 23.094 |
| SMA | 14,76 | 0,459 | 27.903 | 4,167 | 0.453 | 18.521 |

The switching current loop impedance ($Z_{CCL}$) is calculated using (15) and results are shown in Fig. 11. The inductance $L_{CCL,SMA}$ calculated using the SMA connector is 55.02 nH while with the flexible probe the value obtained $L_{CCL,probe}$ is 59.36 nH. Therefore, the error with respect to $L_{CCL,SMA}$ is 7.89%.

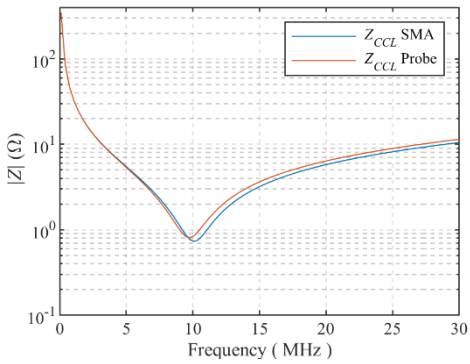


Fig. 10. Impedance measured with SMA and with flexible test probe.

## 5. Conclusions

A procedure for characterizing parasitic impedances of PCB SiC inverter is proposed. The analysis of a laminated PCB busbar (two parallel planes) is considered as a transmission line terminated at the load dipole $Z_L$. The switching current loop impedance ($Z_{CCL}$) calculated from the previous parasitic impedances is compared with those measured using a fixed probe based on SMA connector.

The proposed methodology error (7.89%) is acceptable and the technique can be considered as a valid alternative for determining the parasitic impedances.

## Acknowledgements

The authors would like to thank the technical support from the Research Group on Renewable Energy Integration (GENER) of the University of Zaragoza (accredited and funded by the Government of Aragon).

This research has received funding from the Spanish Government MCIN/AEI/10.13039/501100011033 under grant agreement No CPP2021-008848 and from the European Union NextGenerationEU/PRTR.

## References

[1] B. Zhang and S. Wang, "A Survey of EMI Research in Power Electronics Systems with Wide-Bandgap Semiconductor Devices," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 626–643, March 2020.

[2] V. Nguyen, L. Kerachev, P. Lefranc and J. Crebier, "Characterization and Analysis of an Innovative Gate Driver and Power Supplies Architecture for HF Power Devices with High dv/dt," in IEEE Transactions on Power Electronics, vol. 32, no. 8, pp. 6079–6090, Aug. 2017.

[3] T. Liu, R. Ning, T. T. Y. Wong and Z. J. Shen, "Modeling and Analysis of SiC MOSFET Switching Oscillations," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 747–756, Sept. 2016.

[4] R. S. Krishna Moorthy *et al.*, "Estimation, Minimization, and Validation of Commutation Loop Inductance for a 135-kW SiC EV Traction Inverter," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 286-297, March 2020, doi: 10.1109/JESTPE.2019.2952884.

[5] S. Li, L. M. Tolbert, F. Wang and F. Z. Peng, "Stray Inductance Reduction of Commutation Loop in the P-cell and N-cell-Based IGBT Phase Leg Module," in IEEE Transactions on Power Electronics, vol. 29, no. 7, pp. 3616–3624, July 2014, doi: 10.1109/TPEL.2013.2279258.

[6] A. Ruehli, C. Paul and J. Garrett, "Inductance calculations using partial inductances and macromodels,"*Proceedings of International Symposium on Electromagnetic Compatibility*, Atlanta, GA, USA, 1995, pp. 23–28.

[7] A. Domurat-Linde and E. Hoene, "Investigation and PEEC based simulation of radiated emissions produced by power electronic converters," *2010 6th International Conference on Integrated Power Electronics Systems*, Nuremberg, 2010, pp. 1–6.

[8] Z. Yuan et al., "Design and Evaluation of Laminated Busbar for Three-Level T-Type NPC Power Electronics Building Block with Enhanced Dynamic Current Sharing," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 395–406, Mar 2020, doi: 10.1109/JESTPE.2019.2947488.

[9] Z. Wang, Y. Wu, M. Mahmud, Z. Yuan, Y. Zhao and H. A. Mantooth, "Busbar Design and Optimization for Voltage Overshoot Mitigation of a Silicon Carbide High-Power Three- Phase T-Type Inverter," in *IEEE Transactions on Power Electronics*, doi: 10.1109/TPEL.2020.2998465.

[10] E. Shelton, N. Hari, X. Zhang, T. Zhang, J. Zhang and P. Palmer, "Design and measurement considerations for WBG switching circuits," *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Warsaw, 2017, pp. P.1–P.10, doi: 10.23919/EPE17ECCEEurope.2017.8099377.

[11] A. Llamazares, M. García-Gracia and S. Martín-Arroyo, "Characterization of Parasitic Impedance in PCB Using a

Flexible Test Probe Based on a Curve-Fitting Method," in *IEEE Access*, vol. 9, pp. 40695-40705, 2021, doi: 10.1109/ACCESS.2021.3064190.

[12] Keysight Technologies, Appl. Note 5990-7033, LF-RF Network Analyzer with Option 005 Impedance Analysis Function, pp. 7–12, 2018.

[13] M. K. Kazimierczuk, *High-frequency magnetic components*, 2nd ed., John Wiley & Sons, 2014.

[14] S. P. Hall and H. L. Heck, “Nonideal Conductor Models,” in *Advanced Signal Integrity for High-Speed Digital Systems*, 1st ed., John Wiley & Sons; 2009, doi: 10.1002/9780470423899.

[15] T. Liu, T. T. Y. Wong and Z. J. Shen, "A New Characterization Technique for Extracting Parasitic Inductances of SiC Power MOSFETs in Discrete and Module Packages Based on Two-Port S-Parameters Measurement," in *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9819–9833, Nov. 2018, doi: 10.1109/TPEL.2017.2789240.