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DC-link MPPF Capacitors Online Condition Monitoring System for AC/DC power converters integrated in Converter Control System

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Abstract. In the realm of power electronic converters, the reliability and lifespan of DC-link capacitors play a crucial role in determining the overall system performance.

This study contributes to the advancement of knowledge in the field of lifetime management and estimation for DC-link capacitors. It introduces an online estimation algorithm implemented in a 120kW PV inverter demonstrator, utilizing TDK Electronics' ultra-low inductance series B2563* capacitors.

The paper demonstrates the implementation of the monitoring algorithm without the need of additional or dedicated voltage and/or current sensors during converter operation. All calculations are based on existing variables or estimates of capacitor variables.

The impact of factors such as ambient temperature, managed power, and DC-Link voltage is analysed and tested in the prototype.

Key words. DC-link capacitor degradation, Predictive maintenance, Smart inverters.

1. Introduction

Generally, three different capacitor technologies are used in DC-Link applications: aluminium electrolytic capacitors (Al-Caps), metalized polypropylene film capacitors (MPPF-Caps) and multilayer ceramic capacitors [1]. Depending on the capacitor technology, the failure modes and mechanisms, as well as the main factors that cause failures, are different. These are deeply analysed in [1]. However, the dominant failure mode of the three types of capacitors is degradation, which causes the deterioration of the capacitor's performance.

Although the three types of capacitors share degradation as the dominant failure mode, the effect of degradation on the different types of components varies. As it is introduced on [2] for the different types of capacitors, the failure criteria considered for considering a capacitor as degraded is different. For example, in Al-Caps, a 20% of reduction in the capacitance is considered as failure; but in a MPPF-Cap is considered a 5%.

In the capacitor, the characteristic impedance does not only consist of a single capacitance, but due to the construction of the component, an ESR (equivalent series resistance) and an ESL (equivalent series inductance) are also present with the capacitance. Thus, for aluminium electrolytic capacitors, the degradation affects both capacitance and ESR. However, for film and ceramic capacitors, the ESR is not so affected, with only the capacitance being reduced when the component degrades.

Therefore, while both capacitance and ESR estimation could be used to estimate the degradation of electrolytic capacitors, this could only be done by estimating capacitance for film capacitors.

Works like [3] show typical capacitor degradation curves, based on which condition-monitoring is performed. Based on the initial capacitance or ESR, capacitance and/or ESR will be monitored throughout the use of the device. When the parameter to be monitored reaches the limit of the failure criterion (ESR increase or C reduction), it is considered that the device has achieved his useful lifetime and, therefore, it is degraded.

For the estimation of capacitor lifetime, several lifetime models exist in the literature, that evaluate the impact of different operating variables on the converter lifetime. The main factors affecting capacitor degradation are voltage, current and temperature. The latter two are highly correlated with each other, since the effect of ESR losses caused by current through the converter is to increase the temperature of the component.

This is why the models for calculating capacitor life usually depend on both the voltage applied to the capacitor, V, and the hot-spot temperature T_{HS}, following the lifetime model presented in (1), where a and b are the model parameters, and L_0 is the life at voltage V_N at the temperature $T_{HS\,N}$.

$$L = L_0 \left(\frac{V_N}{V}\right)^a e^{\frac{T_{HS} - T_{HS\,N}}{b}} \quad (1)$$

With this expression, it is possible to estimate the service life at certain stress and temperature conditions from the known life for the stress and temperature provided by the life model. In addition, in the literature is possible to see models like (1) but considering also other factors, such as for example relative humidity [2].

Particularly for polypropylene film capacitors (MPPF), the most appropriate method for monitoring their degradation is the estimation of the capacitor capacitance. The capacitor capacitance is determined from the current through the capacitor and its voltage ripple according to:

$$C = \frac{\int i_C dt}{\Delta v} \quad (2)$$

In order to use this expression for the online condition monitoring of the capacitor, the main difficulty lies in the estimation of the current through the capacitor itself, since it is usually a high frequency current that is difficult to sample in real time. For this purpose, different and varied techniques have been presented in the literature, in which the sensing of different variables necessary for the estimation and/or the injection of harmonics at different frequencies is considered. Likewise, proposals for monitoring algorithms based on the use of neural networks and/or artificial intelligence for the estimation of capacity loss in the DC-Link have also been presented [4]. Finally, it has also been proposed the estimation of the capacitance during the DC-Link precharge or discharge, monitoring how the capacitor voltage evolves and using least-mean-square algorithm [6], although this cannot be done during converter operation.

2. Converter used as case study

The converter employed as case study is a PV inverter developed by IKERLAN, and its power core is shown in Fig. 1.

The PV converter is composed by three CAS325M12HM12 semiconductor modules (1200V Silicon Carbide devices from Wolfspeed). As for the capacitor bank, it consists of 5 B25632E1117K film capacitors from TDK (Fig. 2), rated at 1000V and 110uF per capacitor. This capacitor model is part of the B2563* Series offered by TDK with ESL<13nH optimized for high frequencies, as is the case of the converter under study, based on SiC modules with extra-low parasitic inductance.

The main characteristics of this capacitor series are:

- Voltage range from 600 to 2000 V DC.
- Rated capacitance from 20 to 270 μF.
- Available with male and female terminals.
- Temperature up to 85 °C hotspot.

The whole capacitance in the DC-link is composed of three capacitors in parallel, and a fourth branch in which two capacitors are arranged in series, as can be seen in Fig. 3. Thus, the total capacitance of the capacitor DC-link is 385 uF.

Regarding the converter control, this has been performed on a sbRIO-9607 from National Instruments. The control algorithm implements a power control regulating, in d-q axes, the current delivered to the grid. To perform this current control, the converter incorporates the sensors presented in Fig. 3: sensing of the DC-Link voltage and two phases of the grid, and sensing of the three grid currents.

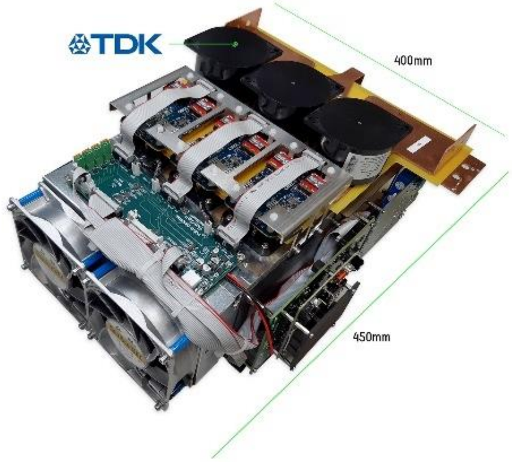

Fig. 1. 120kW inverter used as case study.

Fig. 2. MKP DC ultra-low inductance series B2563*E by TDK.

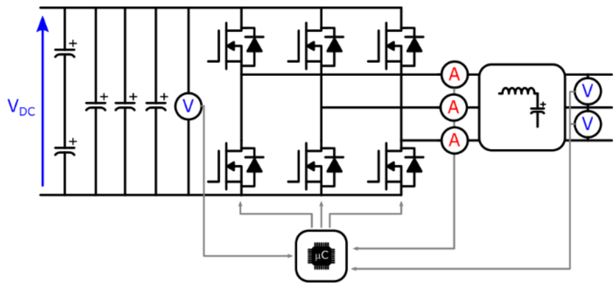

Fig. 3. PV converter electrical diagram

The characteristics of the PV converter are presented in Table 1.

Table 1. PV converter specifications

Power [kVA]	120
DC Voltage range [V]	650-1000
Switching frequency [kHz]	20
Control Unit	SbRIO
Grid voltage [V RMS]	400

The goal of this work is to integrate the monitoring algorithm into the control of the solar converter itself, to be able to make online estimation of the remaining useful life of the capacitor. This enables the preschedule of maintenance works when the component is close to deterioration.

To avoid adding complexity to the system or adding extra costs, the algorithm uses the variables and measurements already available for the control of the converter itself, without adding extra sensors. The hidden variables required to estimate the lifetime consumption of the capacitor can be estimated through the existing sensors or variables required for the converter regulation.

3. Monitoring algorithm proposal

A diagram of the DC-link capacitor monitoring algorithm is presented in Fig. 4.

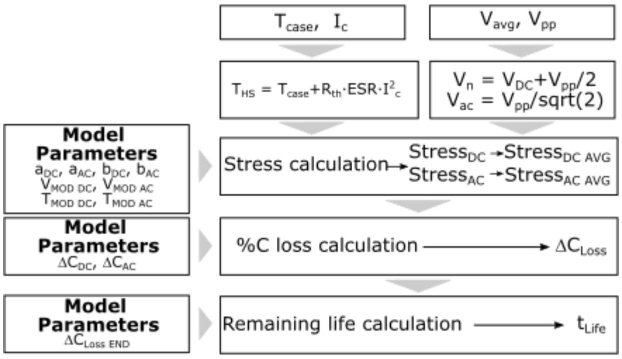

Fig. 4. Monitoring algorithm proposal

The variables needed by the algorithm, and the calculation proposal is presented hereafter.

Firstly, the measurement of the RMS current through the capacitor (I_C), and the temperature of the capacitor's case (T_{case}) are used to calculate the hot-spot temperature (T_{HS}) of the capacitor.

Then, based on the DC bus voltage measurement (V_{DC}), the average voltage (V_{avg}) and voltage ripple (V_{pp}) of each capacitor is calculated.

The three calculated parameters (T_{HS}, V_{avg} and V_{pp}) are used to determine the stress on the monitored capacitor, both DC and AC, from the component life model. The stress determines the ratio of life consumed with respect to the conditions under which the model was obtained in each period. Thus, for example, conditions resulting in a stress of 2 imply that the capacitor will take half the time of the life test to degrade, while with a stress of 0.5 the life-time will be twice as long.

To perform this estimation, it is necessary to know in detail the conditions in which the lifetime model of the device has been performed, as well as the parameters extracted from it. Life model characterization tests are usually obtained by applying controlled test conditions, either DC or AC. However, it is required to consider that in a real application a device is subjected to both AC and DC stress. Therefore, it is necessary to determine the effects of degradation in AC and DC independently, and subsequently sum their effects.

In the lifetime tests, the components are tested under certain conditions of stress: a voltage V_{MOD}, and a temperature T_{MOD}, equal to or above the nominal ones. The stress reached under this condition is $Stress_{MOD}$ =1, and the hours reached are defined as t_{MOD}. As result of the test, the capacitor losses a percentage of its capacitance ΔC_{MOD} corresponding to the end-of-life criterion (usually between 3 and 5%). In order to characterize both DC and AC stress, the lifetime tests must be done in both conditions. Therefore, the resulting model parameters are different. The parameters for these capacitor series are listed in Table 2.

Table 2. Stress parameters model example

AC Stress parameters		DC Stress parameters	
$V_{MOD\ AC}$	150V	$V_{MOD\ DC}$	1300V
$T_{MOD\ AC}$	80ºC	$T_{MOD\ DC}$	80ºC
$t_{MOD\ AC}$	1000h	$t_{MOD\ DC}$	1000h
$\Delta C_{MOD\ AC}$	3%	$\Delta C_{MOD\ DC}$	3%

These parameters are provided by TDK (capacitor manufacturer), for the B25632E1117K capacitor used in the prototype converter. Parameters a_{AC}, b_{AC}, a_{DC}, and b_{DC}, are confidential. Therefore, they are not revealed in this paper. However, they have been considered in the development.

DC and AC stress expressions are defined by (3) and (4).

$$Stress_{DC} = \left(\frac{V_{MOD\ DC}}{V_N}\right)^{a_{DC}} \times e^{\frac{T_{HS}-T_{MOD\ DC}}{b_{DC}}} \qquad (3)$$

$$Stress_{AC} = \left(\frac{V_{MOD\ AC}}{V_{AC}}\right)^{a_{AC}} \times e^{\frac{T_{HS}-T_{MOD\ AC}}{b_{AC}}} \qquad (4)$$

Once the AC and DC stresses are determined, an averaging of the stress over a time period is recommended, to avoid high fluctuations in the remaining useful lifetime calculations, due to the logarithmic relations of the variables.

Based on the AC and DC stress, and from the lifetime criterion used in determining the parameters of the life model, the cumulative percentage of consumed capacitance ΔC_{Loss} caused by DC and AC stress is calculated according to (5).

$$\Delta C_{Loss} = \sum \frac{\Delta t}{1000} (\Delta C_{MOD\ DC} \times Stress_{DC\ AVG} + \Delta C_{MOD\ AC} \times Stress_{AC\ AVG}) \qquad (5)$$

Finally, knowing the cumulative lost capacitance and both AC and DC stress averaged, it is possible to estimate the remaining useful lifetime of the device, defined as t_{life}.

$$t_{LIFE} = \frac{\Delta C_{Loss\ END} - \Delta C_{Loss}}{\frac{\Delta C_{MOD\ DC}\ Stress_{DC\ AVG}}{1000} + \frac{\Delta C_{MOD\ AC}\ Stress_{AC\ AVG}}{1000}} \qquad (6)$$

A. Capacitor's current estimation

As indicated before, it is required to implement a method for the estimation of the current through the capacitor to then estimate the capacitor losses and thus the internal temperature of the hot spot. This current has an average value of zero, and high-order frequency component, so its precise measurement is complex.

To estimate it, the analytical formula for calculating the RMS current through the whole DC-Link capacitor bank has been proposed in [5], considering that the converter is working under a 3-phase balance system:

$$I_{c,tot} = I_{ph}\sqrt{2m\left(\frac{\sqrt{3}}{4\pi} + cos^2\,\phi\left(\frac{\sqrt{3}}{\pi} - \frac{9m}{16}\right)\right)} \qquad (7)$$

As can be seen, this expression depends on the relationship between the DC input and AC output voltages through the modulation index $m = 2V_{ph}/V_{DC}$, the power factor $cos\phi$ and the RMS phase current I_{ph}.

This calculation can be performed on the converter control platform, that already has all the information for regulation purpose. It is proposed to calculate the modulation index m with which the converter operates, without being directly associated to a specific phase, based on the values of v_d and v_q (d-q axis voltages) available in the converter control according to:

$$m = 2\frac{\sqrt{v_d^2 + v_q^2}}{V_{DC}} \quad (8)$$

Similarly, from the d-q axis currents, it is possible to calculate the RMS phase current I_{ph} used for converter control according to:

$$I_{ph} = \sqrt{\frac{i_d^2 + i_q^2}{2}} \quad (9)$$

Also, from the currents in d-q synchronous reference frame, the power factor $cos\phi$ can be calculated according to:

$$cos\,\phi = \cos\left(atan\left(\frac{i_q}{i_d}\right)\right) \quad (10)$$

B. Hot-spot temperature estimation

To perform the calculation of the hot-spot temperature more accurately, it is proposed to perform the calculation by estimating the losses of the capacitor P_{loss} using the ESR, the current I_C and the thermal jump ΔT from the losses and the R_{th}, according to:

$$T_{HS} = T_{case} + \Delta T = T_{case} + P_{loss} \times R_{th} = \\ = T_{case} + I_c^2 \times ESR \times R_{th} \quad (11)$$

For this calculation, it must be considered that the current I_C per capacitor is not the same as the $I_{C,\ tot}$ calculated according to (7) of the converter capacitor bank. Since the capacitor bank is composed of five capacitors, three of them in parallel and with another branch in parallel with two in series, the calculated current will be distributed according to the impedance distribution. For each of the branches in parallel with a capacitor will circulate the current calculated in (7) multiplied by 2/7, while the branch that has two capacitors in series will circulate the current calculated in (7) multiplied by 1/7. This is depicted in Fig. 5.

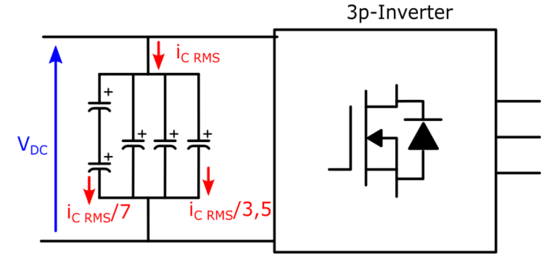

Fig. 5. Current distribution through the capacitor bank

As for ESR and R_{th}, both parameters are typically available in the component datasheet. However, ESR has a value that is usually frequency dependent. According to the supplier, TDK, the expression relating ESR to frequency is given in (12). This expression is presented in Fig. 6. Since expression (7) determines a single value of the RMS current, without specifying its frequency spectrum, it has been considered the ESR at twice the switching frequency, which is the dominant harmonic, i.e. 40 kHz. In this case, the result is 0.9382 mΩ per capacitor. Regarding the thermal resistance, its value is R_{th}=6.8 ºC/W.

$$ESR[m\Omega] = 0.9 + \frac{318.31}{f} + \left(\frac{f}{2.3E5}\right)^2, \\ \forall f \in [50Hz\,, 400\,kHz] \quad (12)$$

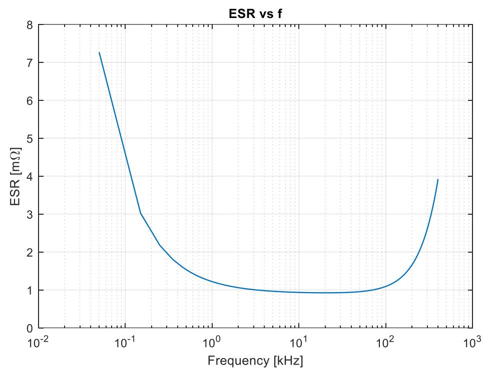

Fig. 6. Curve of ESR values as a function of frequency for capacitor B25632E1117K

Regarding the capacitor's case temperature measurement, it is common in high-power converters to incorporate different temperature sensors to avoid overheating situations of the different elements. It is possible to use one of these for monitoring the temperature of a capacitor package. This temperature sensor should be placed on the side of the package, at 1/3 of the height near the base where the terminals are located. Fig. 7 shows the arrangement of the temperature sensor in the capacitor.

Fig. 7. Capacitor case temperature sensor arrangement

C. Voltage ripple estimation (AC stress)

In the case of the voltage ripple, the voltage at the DC bus is measured by the PV converter controller, as it has been depicted previously on Fig. 3. Therefore, the peak-to-peak voltage (V_{pp}) is totally known by the controller.

With this, the model approximates the AC stress as a sinusoidal waveform with:

$$V_{ac} = \frac{V_{pp}}{2\sqrt{2}} \tag{13}$$

However, this voltage ripple in the DC-Link could also be analytically estimated based on the calculations proposed in [7].

4. Influence of the variables

In this section, it has been evaluated the influence of each variable in the consumed capacitance ΔC, considering 1 hour of operation under different operating conditions. Considering the nominal power of 120kW, with an ambient temperature of 40, 50 and 60ºC, the ΔC *[%]* per year as function of the DC voltage is presented in Fig. 8.

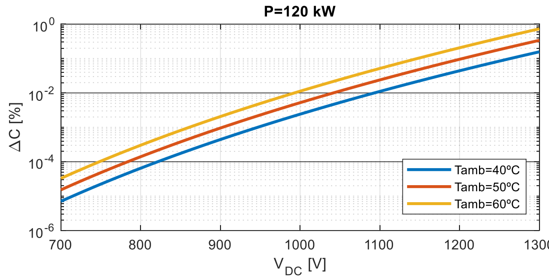

Fig. 8. ΔC *[%]* per year as function of the DC voltage.

Considering, secondly, an ambient temperature of 40ºC and a DC bus voltage of 850, 1000 and 1300V, the ΔC *[%]* per year as function of the operating power is presented in Fig. 9.

And finally, considering the nominal power of 120kW and a DC bus voltage of 850, 1000 and 1300V, the ΔC *[%]* per year as function of the ambient temperature is presented in Fig. 10.

It can be observed that, in the converter under study, the variation of voltage in the DC-Link has the greatest influence on the degradation of the converter, where working at 700V, or at 1000V, is around 330 times different.

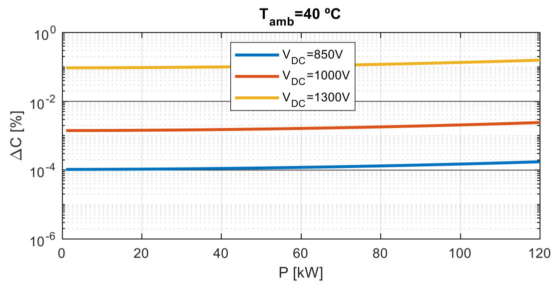

Fig. 9. ΔC *[%]* per year as function of operating power.

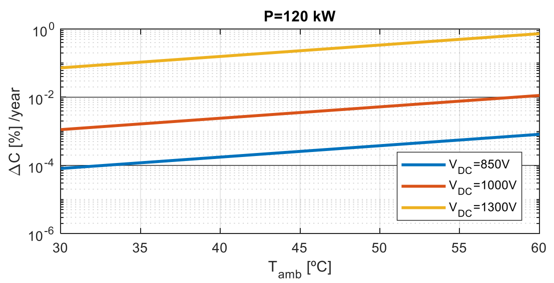

Fig. 10. *ΔC [%] per year as function of ambient temperature.*

In contrary, the influence of the ambient temperature or the power is lower in this prototype. This is because the power handled by the converter has a very low influence (1.5 times more degradation at 1kW than at 100kW), as the thermal jump in the capacitor at constant ambient temperature is very low, less than 5ºC at maximum power. Therefore, the generated thermal jump does not have a notable influence. Note that this comparative analysis may results in different conclusions for other power converters.

5. Experimental Results

In the PV converter used as case study, first, the capacitor current estimation is tested. Previously, it has been introduced that the RMS current of the capacitor (I_C) is calculated using the control variables with the expression (7). The measurement of the capacitor's current in the prototype is presented in Fig. 11, working under nominal 100kW power, with a DC bus voltage of V_{DC}=800V.

In the figure, an oscillation at 107kHz in the current is highlighted. This oscillation is due the resonances between the five DC-link capacitors that are placed on the busbar. This harmonic component is not considered in (7), because for this expression a pure sinusoidal output current and a pure DC input current are considered.

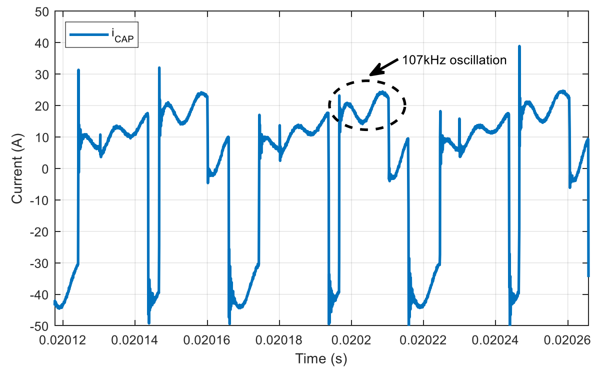

Fig. 11. Current capacitor measurement. The 107kHz oscillation is highlighted.

To quantify the error caused due to that, in Fig. 12 a comparison between the real measurements and theoretical calculations is presented. In blue, the results according to the theoretical expression (7) are plotted. And in yellow and orange, it is possible to see the values calculated with the converter control device, LabView, and the oscilloscope measurement, with an external Rogowski coil, respectively.

The results show that despite of not considering the high-frequency harmonics, the relative error (%) obtained is lower than 3% with an operating power higher than 40kW, that results in a low error on the hot-spot temperature calculations, with neglectable impact on the life calculations.

At the same time, the result of the monitoring algorithm under 30 minutes test is presented in Fig. 13. The evolution of ΔC*[%]* and t_{life} calculation is presented under different DC voltage (V_{DC}) operation conditions. The first 10min, V_{DC}=650V, then during 15 min a voltage of V_{DC}=1000V has been set, and the last 5 min, V_{DC}=800V. During all the test, 100kW power has been delivered by the converter, with an ambient temperature of 26ºC.

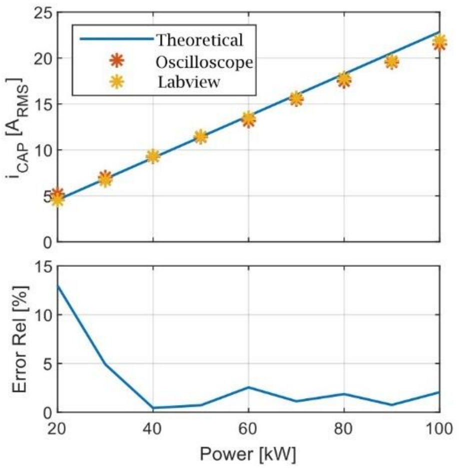

Fig. 12. Capacitor's current estimation. Top:In blue, the results according to (9). In yellow, the values calculated with the converter control device based on the converter on-line measurements. In orange, an oscilloscope measurement with an external Rogowski coil. Bottom: in blue, the relative error of the measurement used in the algorithm ("Labview").

The results show the correct behaviour of the algorithm, with a big impact of the 1000V condition, that results in an expected life of 71 years under this condition. The change of this voltage, to 800V increases the life to 2741 years.

4. Conclusion

A DC-Link condition monitoring algorithm for MPPF capacitors is presented in this work.

This algorithm uses the current and voltage sensors already available in the converter for its current/voltage control and estimates the working conditions of the DC-link capacitors to make an online estimation the accumulated capacitance degradation and expected life. Therefore, it is not required to alter the regular operation of the converter to perform the condition monitoring of the devices.

The proposed algorithm has been tested in a real 120kW SiC-based PV power converter with TDK ultra-low inductance capacitors, using the degradation models provided by TDK.

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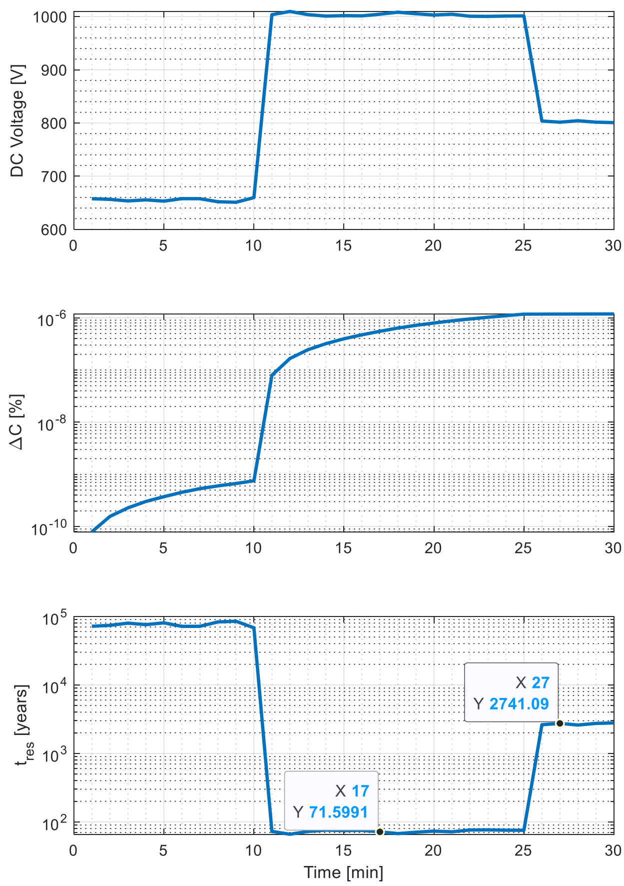

Fig. 13. Time evolution of the monitoring system algorithm, under steps on the DC voltage.

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