Power Quality and Energy Conservation Enhancement Using a Unified Filter-Capacitor Compensator

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Abstract. The paper presents a low cost pulse-width modulated Unified Power Filter/Capacitive Compensation (UPFCC) scheme. The unified filter-action combined with capacitive compensation result in increased power quality and energy conservation for a wide class of temporal, inrush-type, switch mode power supply and other nonlinear loads.

Key words

Power quality, energy conservation, harmonic reduction, nonlinear loads.

1. Introduction

The mushrooming use of nonlinear-type loads are causing severe problems for electric utility suppliers, consumers and manufacturers of electrical equipment. The electric utility industry and consumers of electrical energy are facing new challenges for cutting the electric energy cost, improving energy utilization, enhancing electric energy efficiency & demand-side management, improving supply waveform power quality, reducing safety hazards to personnel and protecting electronic sensitive computer and automatic data processing networks. All nonlinear electric loads fall in either one of two general categories, namely the arc (inrush/saturation) type and converter switching type power electronic switching.

The proposed filter/switched capacitor scheme can be used for single phase or 3 phase-4 wires "Y" connected low voltage utilization computerized network in the range of (1KVA – 150 KVA). The reduction in quasi-steady harmonics and supply waveform power quality improvement has the added safety benefit of securing the computerized network against damage, data-loss and other personnel-shock safety related issues related to hot neutrals and ground potential rise (GPR) and loop-circulating neutral ground return currents. The growing use of nonlinear type electric loads causes a real challange to power quality and harmonic mitigation issues for Electric Utilities around the world, especially in the existing era of unregulated electricity market where: competition, supply quality, security and reliability are key issues for any economic survival. Grid network pollution is characterized by the nonlinear electric load ability to distort/modify and change the voltage and current waveforms due to its inherent nonlinearity. These nonlinear-type loads include fluorescent lighting, computers, adjustable speed drives, heating and lighting controls, industrial rectifiers, UPS (uninterruptible power supplies), arc-furnaces and other process industry loads [1]-[8]. Harmonics, waveform distortion and power quality problems generally also translate into inefficient electric power system operation, electric fire and personnel safety hazards, Telecom-noise-interference and malfunction of solid-state relaying and protection systems as well as serious ground potential rise GPR/Tingle voltage/hot neutral phenomena, causing havoc with telecommunications, computer and data networks as well as posing live-stock and farm safety risk and Milk Farm production decline.Harmonics and power quality PQ problems [9]-[13] are also usual by- products of solid-state converters, industrial-rectifiers.

This paper presents the novel low-cost UPFCC filter/compensation scheme using an on-line dynamic-control strategy for combined power quality (PQ) enhancement, harmonic reduction and energy conservation. The scheme is a member of a family of low-cost switched/modulated power filters and electrical energy economizers (misers) and compensators developed by the First Author.

2. Digital simulation Models

Figure 1 depicts the single line diagram (SLD) of the utilization (single-phase) or (three-phase- 4-wire) feeder and the connection of the Unified power filter & capacitor Compensator (UPFCC) to the nonlinear SMPS-

computer network load or any nonlinear inrush or temporal type load.

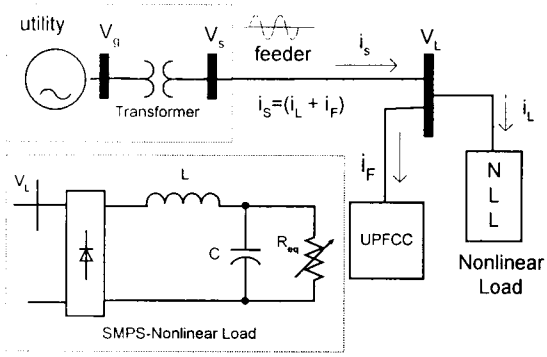

Fig. 1. SLD of the Utilization Feeder with the (UPFCC) Compensator at the nonlinear load bus

Figure 2 shows the proposed low cost Unified (UPFCC) compensator scheme. The UPFCC is a switched/ modulated capacitor bank using the pulse-width-modulated (PWM) strategy. The switching device uses either solid state switch (IGBT or GTO). Figure 3 shows the proposed dual-loop dynamic tracking controller to ensure that both objectives of (energy/power) saving as well as power quality enhancement of the supply system current and load bus voltaje can be achieved.

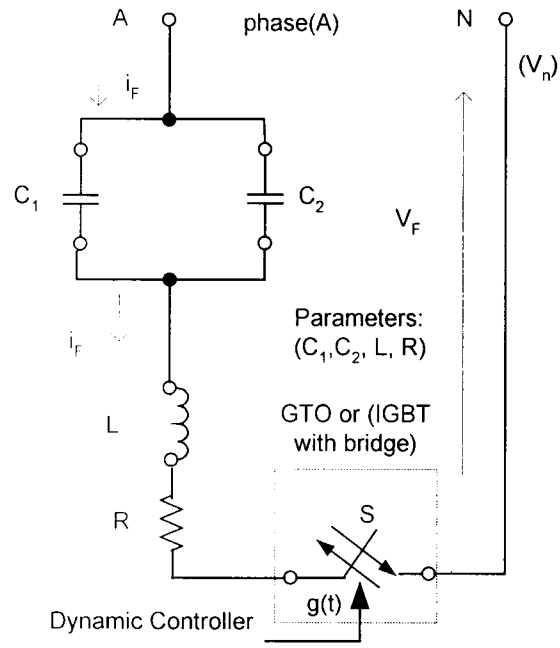

Fig. 2. Low-Voltage Switched/Modulated (TAF)/Filter Compensator

Figure 3 shows the proposed dual-loop dynamic tracking controller to ensure the objectives of (energy/power) saving as well as power quality enhancement of the supply system current and load bus voltage. Figure 4 depicts the equivalent circuit of the switch mode power supply nonlinear load model used. The SMPS, in one form or another, is the most common nonlinear device causing a great deal of power quality problems due to their massive numbers and proliferation. This type of nonlinear load draw nonsinusoidal current in short pulses rather than the smooth sine waveform. In order to deliver the same amount of power in short pulses; the current peaks are much higher. This puts more stress on the system wiring in the circuit breakers, and even the generation and distribution equipment provided by the electric utilities.

3. Matlab/Simulink Results

The unified power filter and capacitor compensator scheme (UPFCC) was validated on a simple radial utilization-low voltage feeder. The system, compensator and controller parameters are given in the Appendix.

The validation results using the MATLAB/Simulink/ Power System Blockset (PSB) indicated the effectiveness and simplicity of this low cost (UPFCC) solution to harmonic reduction. Total voltage and current distortions $(THD)_V$, $(THD)_i$ indices were utilized to select the (UPFCC) compensator parameters using an off-line performance criterion "J" based on (THD) magnitude of offending harmonic and RMS value of source current:

$$J_{min} = \text{Min}\{\alpha_1 (THD)_i + \alpha_2 (THD)_V + \alpha_3 (I_{S\,old} / I_{S\,new}) + \alpha_4 |I_n| \quad (1)$$

Where all α are specified design weighting factors and $|I_n|$ is any offending dominant low order (triplen or odd) harmonic intensified by any near-parallel resonance condition on the utilization grid network.

The unified compensator (UPFCC) scheme was validated for the combined effectiveness in reducing feeder power P_S and source current harmonics, saving energy as well as improving the waveform power quality for the supply current (i_s) and load voltage V_L by reducing the harmonic content, flickering, inter-harmonics or any low order frequencies introduced by the combined nonlinear load temporal, inrush and switching type nonlinearities as encountered in lighting control, computer-SMPS network, ventilation and air-conditioning motorized load. The feeder system was checked for the two cases (i) without UPFCC compensator and (ii) with UPFCC compensator for a switch-mode type nonlinear load.

Figures 5 to 14 show the MATLAB/Simulink digital simulation results of the system dynamic response for the two-cases of: (i) without (UPFCC) filter/compensator and (ii) with (UPFCC) filter/compensator. Figures 8 and 13 show the (FFT) harmonic current spectra, and total harmonic distortion levels Figure 12 show the switching-pattern of the solid state switch (g1) controlling the unified switching action introduced by the capacitive

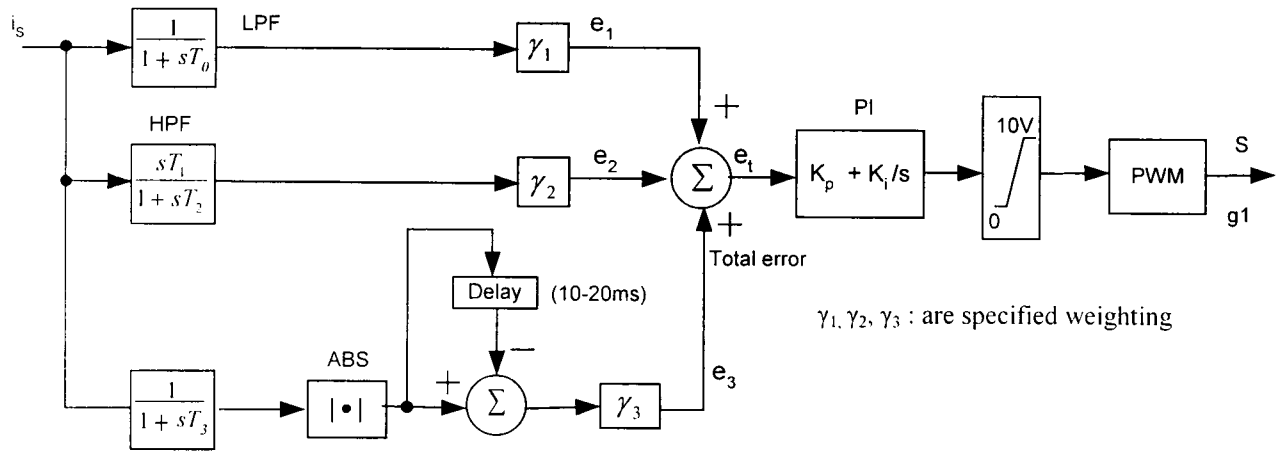

Fig. 3. Tri-Loop Dynamic Current and Harmonic Ripple Tracking Controller

compensation and modulated tuned-arm power filter admittance. Figures 7 and 11 show the power factor, source effective current RMS value and instantaneous power variations without and with the novel low-cost (UPFCC) device. The above ten figures confirm the capacitive compensating effectiveness as well as the harmonic filtering of the unified power filter and capacitive compensating scheme. The novel control objectives are the combined power quality enhancement, harmonic reduction and power/energy savings using a multi-loop dynamic controller for PWM-switching action and UPFCC topology variation between tuned-arm switch filter and a simple time-switched capacitor compensation.

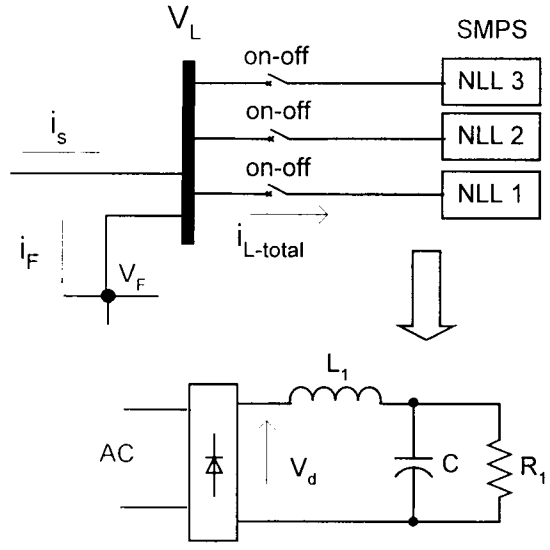

Fig. 4. Equivalent Circuit of SMPS Nonlinear Load

4. Conclusion

The paper presents a low cost novel PWM switched unified power filter and capacitor compensator scheme for either single or 3-phase 4-wire utilization (residential/commercial) loads including Buildings, Malls and Small-Industrial loads. These loads are usually of nonlinear nature. The proposed low cost (UPFCC) scheme ensures both power quality (PQ) enhancement, RMS/power current level reduction, efficient power /Energy utilization and effective demand side management. A THD reduction in source current (is) was calculated and the source current (THD) was reduced from 94% to 8%. The effective fundamental current value was increased, as the source current harmonic content was extensively reduced by the dynamic controller power quality enhancement. The reduction in THD of source current translates into improved power factor and energy saving despite the slight-increase in the fundamental source current component. The power factor PF was calculated as a function of the distortion factor (DF) and the value is improved from 0.72 to 0.99, this means enhanced utilization and energy savings.

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Appendix

System parameters:
120VAC, 60Hz, Single-phase
Nonlinear Load: SMPS
UPFCC-Compensator
C1=25uF; C2=25uF; L=15mH; R=1 Ohm
Controller PID Type (refer to figure 3)
K_p=10; K_i=0.2; γ_1= γ_2= γ_3=1
T_0=60ms; T_1=20ms; T_2=60ms; T_3=60ms;
PWM Switching
$\alpha_D = t_{on} / T_{S/W}$ (duty-cycle-ratio)
$0 < \alpha_D < 1.0$; $T_{S/W} = 1 / f_{S/W}$; $f_{S/W}$ =1000Hz
Total Harmonic Distortion
$(THD)_{is}$ without the USCS=94%, with the USCS=8%
$(THD)_{VL}$ without the USCS=3%, with the USCS=3%

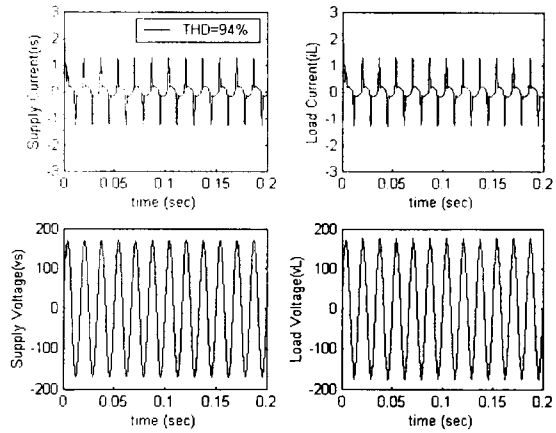

Figure 5: Voltage and current waveforms (source, load) without the UPFCC

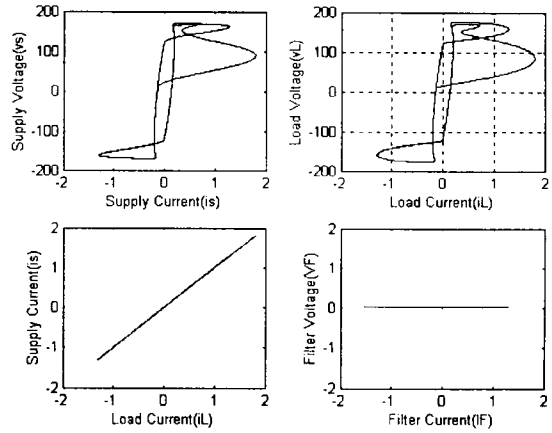

Figure 6: Volt-Ampere Phase Portraits without the UPFCC

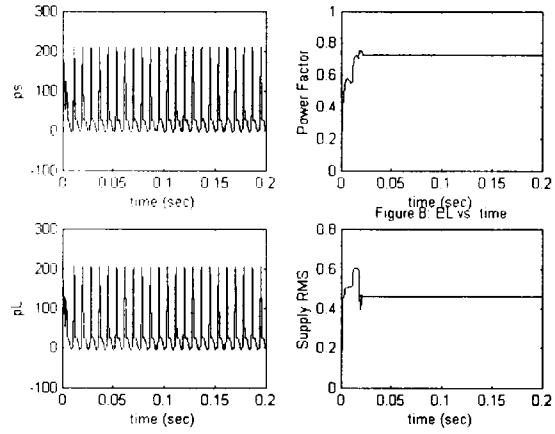

Figure 7: Power waveforms (source, load) and Power Factor and Supply Current RMS without the UPFCC

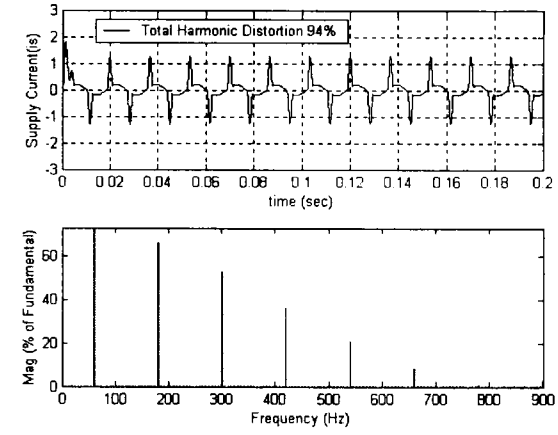

Figure 8: Frequency-Spectra of Supply Current (i_S) without the USCS

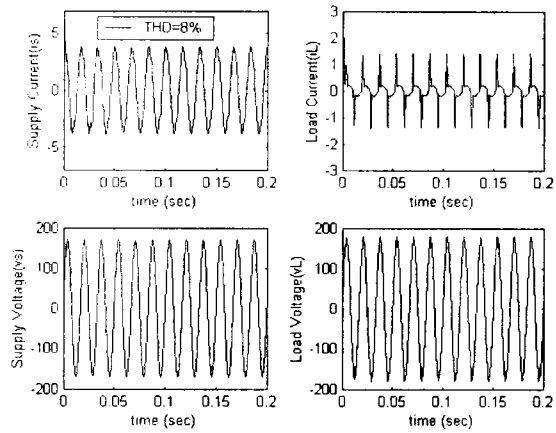

Figure 9: Voltage and current waveforms (source, load) with the UPFCC

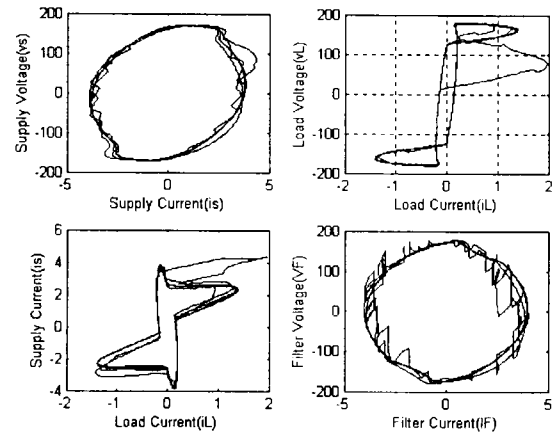

Figure 10: Volt-Ampere Phase Portraits with the UPFCC

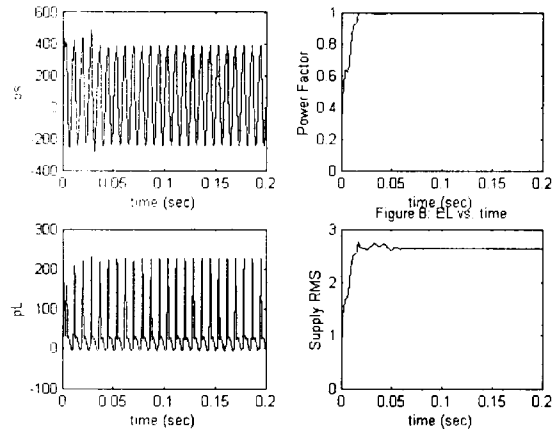

Figure 11: Power waveforms (source, load) and Power Factor and Supply Current RMS with the UPFCC

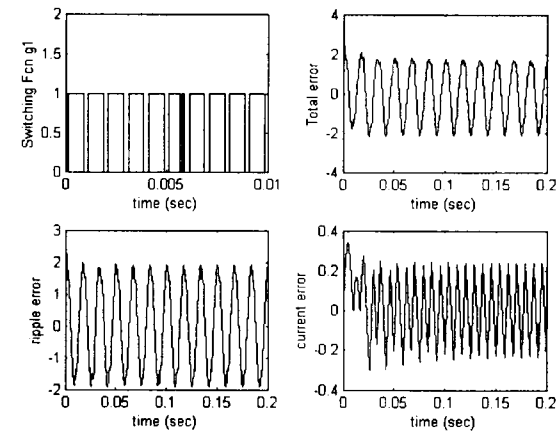

Figure 12: Switching Pattern of S(g1) and PID Input with the UPFCC

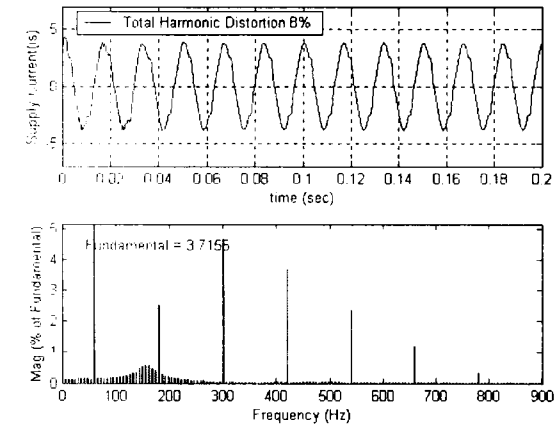

Figure 13: Frequency-Spectra of Supply Current (i_S) with the UPFCC

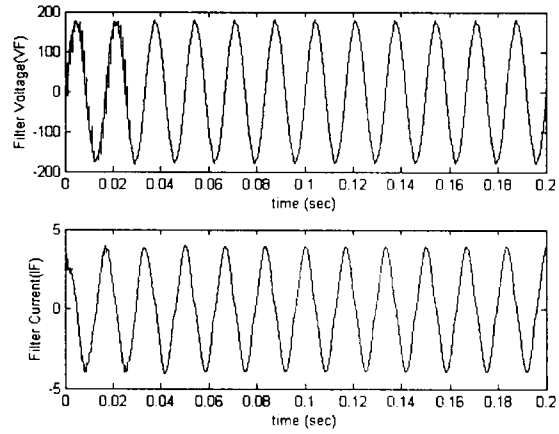

Figure 14: UPFCC Filter/Compensator Voltage and Current