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Adaptive Dead Time Compensation for Cross-Period Single Phase Shift Control of Dual Active Bridge Converters

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Abstract. Nowadays, the need for isolated bidirectional DC-to-DC converters is increasing, as electric energy storage is gaining more popularity. For high power applications, the dual active bridge (DAB) DC-to-DC converters are widely used. Various control methods were proposed throughout the years, but the conventional ones are not practical to use with low frequency and low leakage transformers. In this paper an adaptive dead time compensation method is presented for cross-period single phase shift control, which is specifically designed for these applications and has outstanding transient response characteristics. The behaviour is analysed and compared to uncompensated control thorough hardware-in-the-loop simulation.

Key words. DAB converter, 400Hz transformer, isolated converter, power conversion.

1. Introduction

In power electronics extensive equipment testing is a crucial part of the design process. As electric powertrains are gaining more popularity, the need for high power test laboratories is increasing. In response to this demand an advanced high power electric propulsion drivetrain test laboratory is being built at Budapest University of Technology and Economics, which includes a $360kW$ nominal power Dual Active Bridge (DAB) DC-to-DC converter.

The DAB topology was first proposed and patented in 1991 as an efficient high power bidirectional solution for DC power conversion [1], [2]. The main circuit is built up by two independent full-bridge inverters connected together through a transformer, as shown on Fig. 1. The main energy transfer element is the leakage inductance between the primary and secondary side, this parameter greatly influences the converter behavior [3].

Latest publications on DAB converter switching device selection and algorithms are focusing on enhancing efficiency [4]–[6] and increasing the switching frequency to reduce physical size [7]. For transformers, with low switching frequency and low leakage inductance, the authors proposed the cross-period single phase shift (CP-SPS) control method, which allows outstanding load regulation properties (e.g. in sudden load drop conditions) [8].

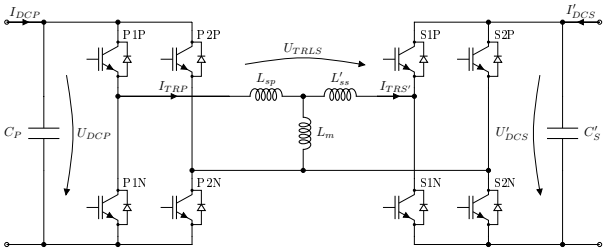


Fig. 1. Power circuit schematic diagram of the DAB converter

Switching devices together with the gate driver circuits have a specific turn-on and turn-off time. The on signal must be delayed from the off signal to prevent short circuit of the DC bus, which would result in excessive heating of the switching device. The time delay between the signals, which is called dead time, could cause voltage distortion on the half-bridge output, depending on the direction and magnitude of the half-bridge output current. This phenomena is well known, however rarely considered in DAB converter applications [9]. In the recent years various publications were written on the topic of dead time effects on SPS [9], DPS [10] control and even for three-phase [11] and ZVS [12], [13] DAB converters.

The turn-on and turn-off time of the switching devices are depending on various parameters [14] (e.g. temperature, current). In this paper an adaptive

dead time compensation method will be presented, to mitigate issues with changing switching delay time in CP-SPS control applications.

In Section 2. the case study converter is introduced, the dead time and switch delay effects on CP-SPS control is analysed in Section 3. The proposed adaptive dead time compensation is presented in Section 4. and validated through hardware-in-the-loop simulation in Section 5.

2. Power circuit

A real application is used as a case study, to analyse the effect of dead time and to present the adaptive compensation method. The analysed equipment is a $360kW$ nominal power DAB converter. Creating a high frequency capable ferrite core for the transformer would be much more expensive than from regular laminated steel core. To keep the equipment cost low, a $400Hz$ laminated steel core transformer was chosen for the DAB converter.

The transformer has multiple primary and secondary windings, which allows various turns ratios between the two sides selected by contactors. Leakage and magnetizing inductance changes depending on the actual turns ratio (Table I). The magnetizing inductance is kept reasonably low to allow measurement of the magnetizing current based on primary and secondary current. The primary side voltage varies between $600 - 800VDC$.

Both DC bus voltage is measured by the controller board. Hall-effect based, fast current sensors are used on both sides of the transformer (I_{TRP}, I'_{TRS}) and on both DC buses (I_{DCP}, I'_{DCS}), as shown on Fig. 1. The full-bridge inverters are built up from $1000A/1700V$ IGBT half-bridge modules.

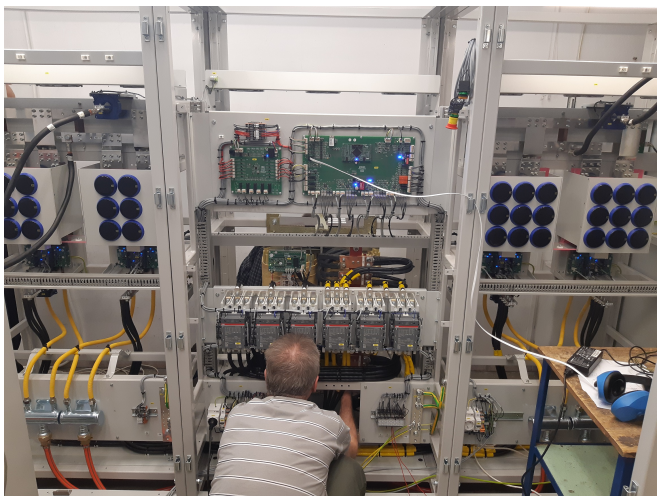


Fig. 3. The real hardware: primary busbar, IGBT modules and gate drivers on the left; transformer, control modules and contactors in the middle; secondary busbar, IGBT modules and gate drivers on the right.

Table I - Transformer parameters

Turns ratio	L_{sp}	L_{ss}	L_m
1.5 and 0.75	$17.0\mu H$	$17.0\mu H$	$5.0mH$
1.2 and 0.6	$25.3\mu H$	$25.3\mu H$	$7.9mH$
1.0 and 0.5	$28.2\mu H$	$28.2\mu H$	$11.1mH$

3. Dead-Time effects on CP-SPS control

The CP-SPS possible switching waveforms are shown on Fig. 2, the basic idea is to change the transformer pass through current ($I_{AVG} = \frac{I_{TRP}+I'_{TRS}}{2}$), while keeping the magnetizing current on the original trajectory. One switching period is divided into six phases (PH1 to PH6). By changing the secondary

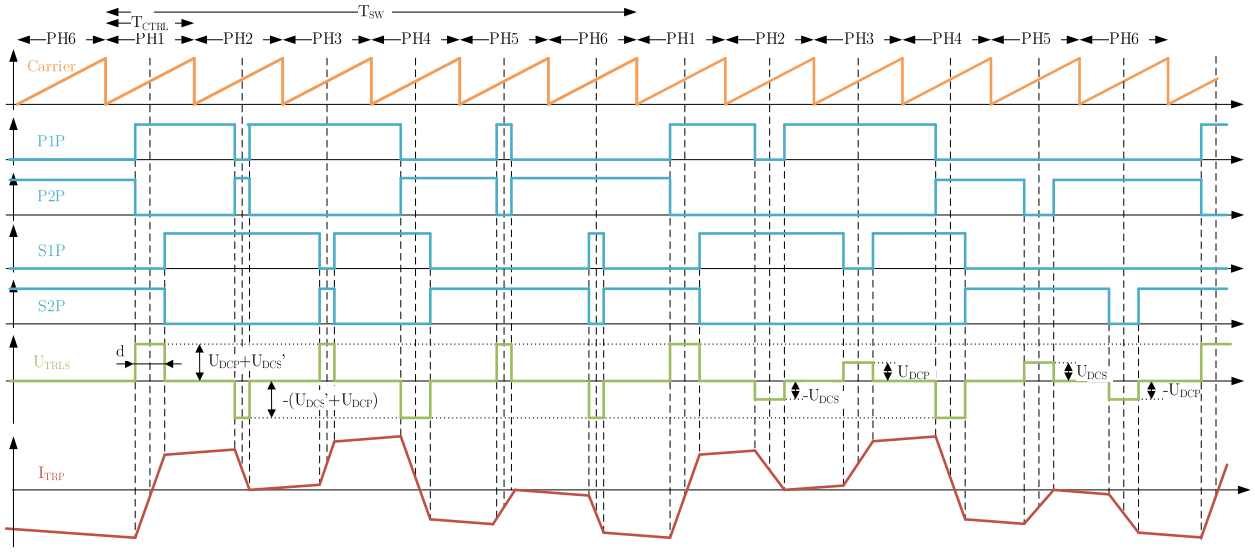


Fig. 2. CP-SPS control resulting waveforms illustrating possible in-period transformer current modifications.

or primary side voltage, the transformer current can be modified six times in one switching period. This is three times more than what is achievable with traditional SPS control [8]. A short circuit can be created either on the primary side (Primary Short, PS) or the secondary side (Secondary Short, SS). Inverting the voltage also possible either on the primary side (Primary Invert, PI) or on the secondary side (Secondary Invert, SI).

The dead time hugely effects the CP-SPS control in PH1 and PH4. Fig. 4 shows the relevant signals during PH1 switching. t_{off} is the falling edge delay, t_{on} is the rising edge delay, t_d is the applied dead time. The time for changing the transformer current (requested by the controller) is d_{orig}. The delays are considered equal on each side as usually the die temperature, applied voltage and current are the same on one side.

In continuous current conduction mode (CCCM) the effective d is not equal to d_{orig} if the falling edge delays are different on primary and secondary:

$$d_{CCCM} = d_{orig} + t_{off}^{S} - t_{off}^{P} \tag{1}$$

If the transformer current reaches zero meanwhile all the primary switches are turned off, the current can not rise further as the body diodes of P1N and P2P were conducting the current. This operation is called discontinuous current conduction mode (DCCM), which distorts the transformer current and results with an effective d of

$$d_{DCCMP} = d_{orig} + t_{off}^{S} - t_d - t_{on}^{P} - (L_{sp} + L'_{ss}) \frac{|I_{TRP}|}{U_{DCP} + U'_{DCS}} \tag{2}$$

where I_{TRP} is the transformer current before the switching action. The voltage-time area of the leakage inductance is reduced, hence the transformer current will reach a lower value then the controller intended.

If the transformer current is negative and all the secondary side switches are turned off, the current is conducted by S2P and S1N diodes until it reaches zero. The effective d can be calculated as

$$d_{DCCMS} = (L_{sp} + L'_{ss}) \frac{|I_{TRP}|}{U_{DCP} + U'_{DCS}} \tag{3}$$

where I_{TRP} is the transformer current before the switching action.

These equations are true for PH4 as well. It can be clearly seen that the switch delays and dead time changes the effective voltage-time area on the leakage inductance, which results with an error in the CP-SPS control.

The applied control loop is shown on Fig. 5. A PI voltage controller is responsible for keeping the primary and secondary side voltage at the nominal level defined by the transformer turns ratio. The secondary side DC current (the load current) is fed forward, thus the controller I_{ctrl} output is near zero in steady state operation. The sum of I_{ctrl} and the load current is the reference for the current controller,

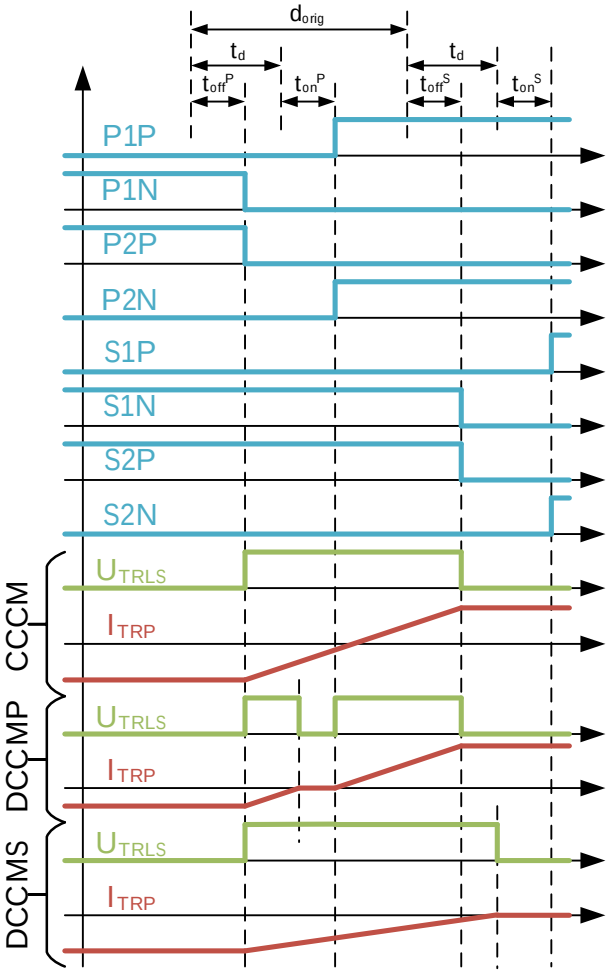


Fig. 4. Dead time effects on transformer current in CCCM and DCCM operations. Magnetizing current is ignored.

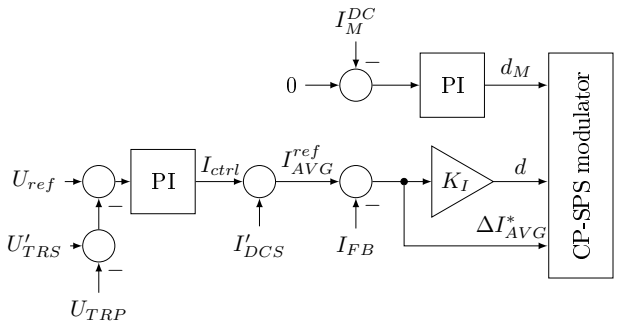


Fig. 5. Control diagram for the Cross-Period Single Phase Shift algorithm

Fig. 6. Control phase dependent parameters

	PH2	PH3	PH5	PH6
U_{PHi} for PS	$-U_{DCS}$	$-U_{DCS}$	U_{DCS}	U_{DCS}
U_{PHi} for SS	U_{DCP}	U_{DCP}	$-U_{DCP}$	$-U_{DCP}$
I_{FB}	I_{AVG}	I_{AVG}	$-I_{AVG}$	$-I_{AVG}$

which K_I and I_{FB} parameters are different for the six control phases [8]. The CP-SPS modulator will decide the switching actions needed in PH2, PH3, PH5 and PH6 based on ΔI^*_{AVG} value [8].

The dead time and switch delays results with lower effective d value, the voltage will drop on the secondary. The voltage controller will detect this error and change its I_{ctrl} output, which results with a non-zero ΔI^*_{AVG} value in PH2, PH3, PH5 and PH6, thus the modulator will create unwanted switching actions. This will result with more distorted current waveform and increased heat in the IGBTs.

4. Adaptive compensation

As t_{off} and t_{on} changes together with the IGBT voltage, current and temperature, the transformer current thresholds for the CCCM or DCCM operation changes. Moreover, the transformer magnetizing current modifies the effects of dead time and switch delay. A solution to this problem would be to calculate how much voltage-time area is missing and compensate for that by increasing or decreasing d. This requires known t_{off} and t_{on} delays, which is not trivial as they change during operation.

A different approach would be to get a feedback about the current change and compensate d based on this information. The main idea of current control in PH1 and PH4 is to calculate d based on the needed change in I_{AVG}:

$$d_{PH1} = \frac{L_{sp} + L'_{ss}}{U_{DCP} + U'_{DCS}} \cdot \frac{1}{T_{CTRL}} \cdot (I^{ref}_{AVG} - I_{AVG})$$

$$d_{PH4} = \frac{L_{sp} + L'_{ss}}{U_{DCP} + U'_{DCS}} \cdot \frac{1}{T_{CTRL}} \cdot (I^{ref}_{AVG} + I_{AVG})$$

For this I_{TRP} and I_{TRS} must be sampled before the switching action to be able to calculate I_{AVG}, the sampling points are shown as ① and ③ on Fig. 8. If these values are sampled again after the switching actions, at ② and ④, ΔI_{AVG} can be calculated to give a feedback for d_{PH1} and d_{PH4} calculation.

The modified control diagram is shown on Fig. 9, it is only applicable for PH1 and PH4. The measured ΔI_{AVG} is compared to the previous ΔI^*_{AVG} required current change, the difference is fed into an integrator,

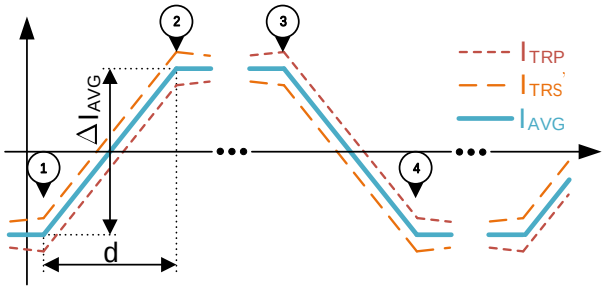


Fig. 8. Transformer current waveforms during PH1 and PH4 switching operations.

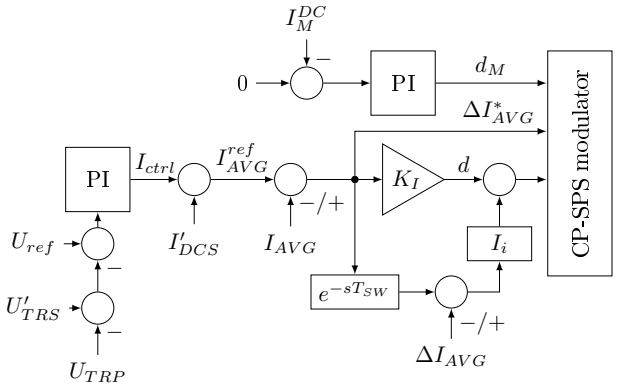


Fig. 9. Control diagram for the Cross-Period Single Phase Shift algorithm with adaptive dead time compensation

which output is added to the calculated d value as a compensation. The integrator is separate for PH1 and PH4, this way the control works correctly even if the delays are different in the two phases.

5. Validation

The adaptive dead time compensation algorithm was tested with hardware-in-the-loop (HIL) simulation method. The power circuit model (Fig. 7) was created in MATLAB simulink and then compiled to a Zynq-7000 SoC powered development board. The control algorithm was implemented in C language and run by

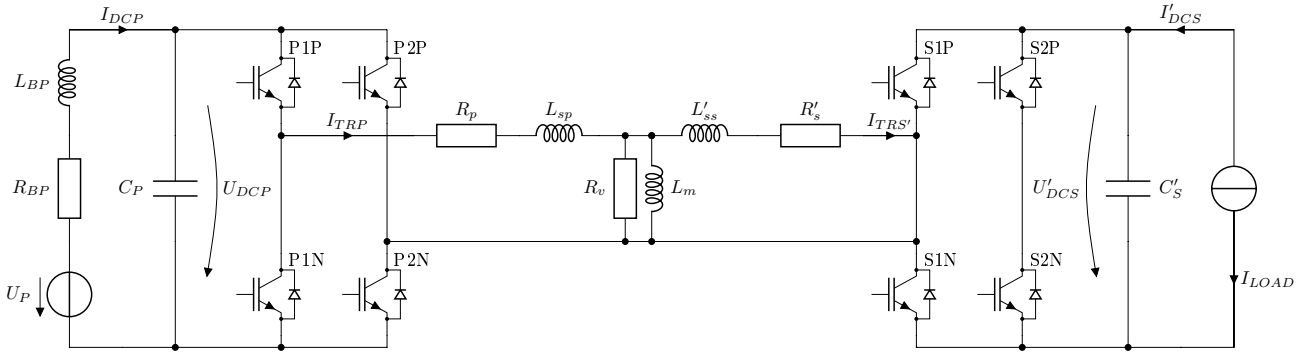
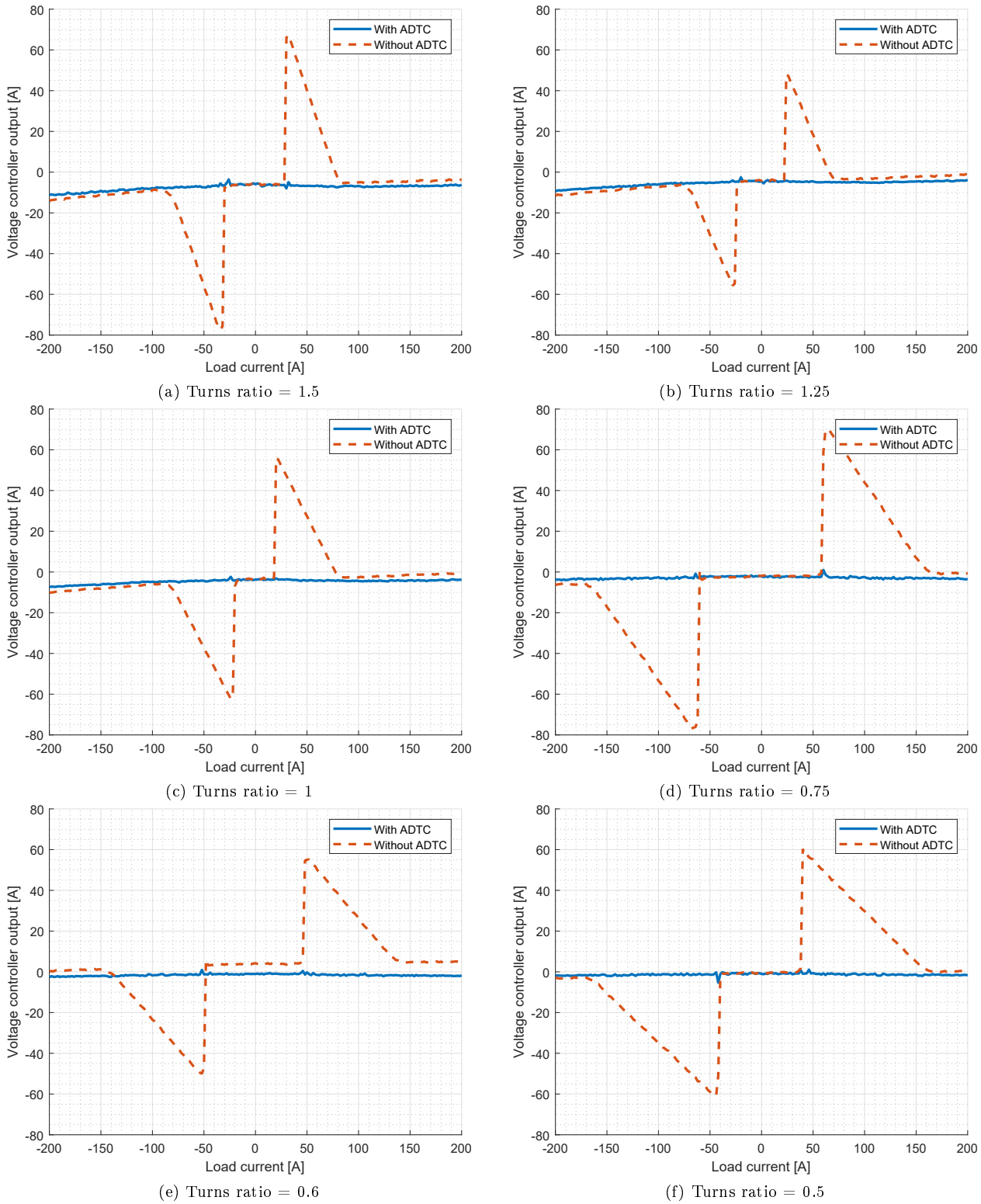


Fig. 7. Power circuit schematic diagram used in the HIL simulation.



(a) Turns ratio = 1.5

(b) Turns ratio = 1.25

(c) Turns ratio = 1

(d) Turns ratio = 0.75

(e) Turns ratio = 0.6

(f) Turns ratio = 0.5

Fig. 10. Comparison of HIL simulation results for different transformer states with and without adaptive deadtime compensation (ADTC).

the TMS320F28075 DSP board, which is used in the real hardware as well.

The simulation results ware captured when the primary DC voltage was set to $800V$. The load current (I_{LOAD}) was changed between $-200A$ and $+200A$ in $2A$ steps. After each current setting a $5s$ wait time was used to allow controllers to settle. Then 128 samples was collected from the voltage controller output and finally the average was calculated. This was done for all 6 possible transformer turns ratio settings. The results can be seen on Fig. 10.

Without ADTC the controller output has high values because of the uncompensated dead time. Peak value and load current thresholds vary with the transformer turns ratio as the transformers inductive parameters change as shown in Tab. I.

Turning on ADTC results with minimal steady state voltage controller output value. On Fig. 10e an advantageous side effect of ADTC can be observed. With 0.6 turns ratio settings, without ADTC and outside dead time effect load current zone, the voltage controller output has non-zero value. This could be due to incorrect K_I parameter settings in the control loop. The ADTC algorithm corrects this error, which means that the controller can adapt to various parameter change (e.g. transformer leakage inductance, delay, temperature).

6. Conclusion

In this paper the switch delay and dead time effects of DAB converters were analysed and was shown how the CP-SPS control is affected by it.

An adaptive dead time compensation method was presented, which effectively solves the issues with low computational power. The solution not only compensates for switch delay, but for other parameter change as well, resulting with a robust control loop.

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