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Design of a PFC rectifier with fast start up response and low input current distortion

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Abstract. For a PFC rectifier, normally designing of the PI compensator is based on the frequency domain model which is derived from the dynamic model of the rectifier, so it cannot guarantee a fast start up response. As the high input current quality and fast start up response are conflicting objectives and with improving one of them, another is degraded, for designing a PI controller which can provide both of them, a Multi-Objective optimization approach can be implemented. In this paper, for the first time, Strength Pareto Evolutionary Algorithm which is based on Pareto Optimality concept is used to gain a fast start up response as well as low input current distortion. In order to validate the proposed PI controller, simulation results are presented.

Key words. Power Factor Correction Rectifier, Boost Converter, Start-up response, Total Harmonic Distortion, Multi-Objective Optimization

1. Introduction

Single-phase diode bridge rectifiers with output capacitor filter are gradually being replaced by pulse-width modulation (PWM) rectifiers to maintain a sinusoidal input current at near unity power factor and to satisfy the necessary harmonic regulations [1]. Power Factor Correction (PFC) Rectifiers with one active element are one of the cheapest topologies which used for providing this goal [2]. Features of this type of converters have received considerable attention in the recent two decades. There are several topologies for these types of rectifiers that Boost based PFC rectifiers are of the most popular ones [3]. For obtaining a low input current THD and high power factor, a high bandwidth current control loop and a low bandwidth voltage control loop in the control circuit of these rectifiers are considered. The bandwidth of voltage control loop is designed low to avoid of entering the voltage ripple to the reference current of the current control loop [4]. This designing is based on the dynamic model or frequency domain model of the rectifier so it cannot provide a good large signal response. In the last years, several techniques have been proposed to improve the dynamic response of these rectifiers by implementing a digital filter [4], ripple estimators [5]-[6], different bandwidths of voltage control loop for steady state and transient [7], or feedforward controller [8]-[9], but the start up response of them has not been studied carefully.

There are several control methods for PFC rectifiers [2], such as, average current control, hysteresis control, Non-linear career control and Indirect current control, which because of needless to measure the input voltage and load current in Indirect current control [8], In this paper this method is considered as the basic control scheme for obtaining the optimized PI compensator coefficients.

In this paper a new method of designing the PI compensator is presented which does not need to any linear or approximate model of the system rather it utilizes the Simulink model of the PFC rectifier. In this proposed method a Multi-Objective Optimization approach is implemented to gain a low input current distortion as well as fast start up response.

2. Evolutionary Algorithm

For solving a Multi-Objective optimization problem, usually the objectives are combined and made a scalar function, and then it is solved by using a common scalar optimization approach. As there is no straightforward method for combining the objective functions which they vary constantly, Game theory concept was considered, that in its original status doesn't need to any modification or combining the objectives. This method of solving the optimization problems requires an evolutionary method to reach globally optimum results. One of the most successful evolutionary methods is Strength Pareto Evolutionary Algorithm [10].

Generally, a multi-objective optimization problem can be represented as:
Minimize:

$$y = f(x) = (f_1(x),... f_i(x),... f_k(x) \quad (1)$$

Subjected to:

$$x = (x_1, x_2,...x_n) \in X \;\; \& \;\; y = (y_1, y_2,..., y_k) \in Y$$

Definition: The vector a in the search space dominates vector b if:

$$\forall_i \in \{1,2,...,k\}: f_i(a) \geq f_i(b) \quad (2)$$

$$\exists_j \in \{1,2,...,k\}: f_j(a) > f_j(b)$$

If at least one vector dominates b, then b is considered dominated vector otherwise it is called non-dominated. Each non-dominated solution is regarded optimal in the sense of Pareto or called Pareto Optimal. The set of all non-dominated solutions is called Pareto Optimal Set and the set of the corresponding values of the objective functions is called Pareto Optimal Front.

A. Strength Pareto Evolutionary Algorithm (SPEA)

The SPEA includes the flowing major steps.

1) *Generate an initial population P and create the empty external non-dominated set P'.*
2) *Paste non-dominated members of P into P'*
3) *Remove all the solutions within P' which are covered by any other members of P'.*
4) *If the number of externally stored non-dominated solutions exceeds a given maximum N', prune P' by means of clustering.*
5) *Calculate the fitness of all individuals in P and P'.*
6) *Use binary tournament selection with replacement and select individuals from P and P' until the mating pool is filled.*
7) *Apply crossover and mutation operators as usual.*
8) *If the maximum number of generations is reached, then stop, else go to step 2.*

Fitness evaluation is also performed in two steps. First, the individuals in the external non-dominated set P' are ranked. Then, the individuals in the population P are evaluated [11].

3. Conventional PFC rectifier system

The AC/DC converter under study is a Boost based PFC Rectifier that converts a 110 volt input supply (AC) to 230 volt at output (DC), this rectifier with Indirect current control scheme is shown in Fig. 1.

The specifications of the PFC rectifier are as follows: i) output power P_O=300 W, ii) peak input voltage: V_{gm}=156 V, iii) line frequency: 50Hz, iv) rated output voltage: V_O=230 V, v) maximum peak-to-peak ripple in the output voltage: $\Delta V_{O(MAX)} = 0.04*V_O$, vi) maximum peak-to-peak ripple in the input current: $\Delta I_{g(MAX)} = 0.2*I_{gm}$, vii) switching frequency: F_{sw}= 70kHz, viii) voltage sensor gain: K_v=0.005, ix) current sensing gain: R_s=0.2Ω, output capacitor: C_O=440 μF, Boost inductor: L_b= 2mH.

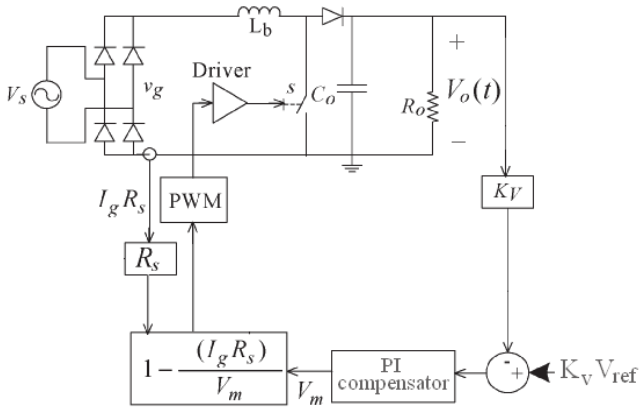

Fig. 1. Boost based PFC Rectifier under study with indirect current control

In the conventional methods of designing the controller for PFC rectifiers, is used from the frequency domain model which is derived from the dynamic model of the rectifier. Fig. 2 shows this frequency domain model of the voltage loop. Equation (3) demonstrates the transfer function of the system.

$$G(s) = \frac{G_V}{1 + sT_V} \quad (3)$$

Where the Tv and Gv can be calculated by help of equations (4) and (5) respectively.

$$T_v = \frac{R_o C_o}{1 + M_g^2 \, R_o/R_e} \quad (4)$$

$$G_V = \frac{0.5 M_g^2 \, R_o/R_s}{1 + M_g^2 \, R_o/R_e} \quad (5)$$

In the above equations the Mg is the ratio of the output DC voltage to the maximum of input voltage. PI compensator can be considered as the equation (6), Value of TPI has been selected to compensate the pole of the system, so it is almost equal to Tv. For the input current THD to be low, usually the corner frequency of the PI compensator is set around 10 Hz.

$$H(s) = \frac{K_{PI}(1 + sT_{PI})}{sT_{PI}} \quad (6)$$

$$K_{PI} = \frac{2\pi f_{BW} T_V}{G_V K_V} \quad (7)$$

By using the equations (4) and (7) the corresponding values TPI and KPI can be calculated as 26ms and 4.8 respectively. Figure 3 shows the steady state input current and start up response of this converter with PI gains which have been designed based on the frequency domain model of this rectifier.

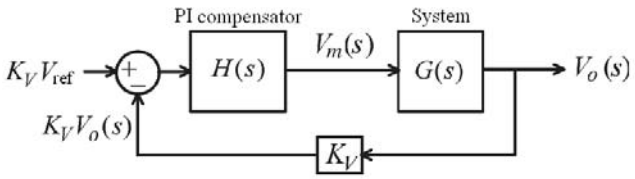

Fig. 2. frequency domain model of the voltage control loop

4. Proposed compensator gains

For obtaining the optimized gains of PI controller in the Indirect current controller of PFC Rectifier, the program is conducted by m-file in MATLAB, while the objective functions have been calculated in SIMULINK using the details of the system. The input current THD and time of start-up response were considered as the objective functions.

Optimal gains (Pareto Optimal Set) and optimal results (Pareto Optimal Front) of running this program are given in Table I and shown in Fig. 4 and Fig. 5. These results are obtained through running the program for 20 generations and each generation includes 25 members. Also the crossover fraction is selected to be 70%.

Start up response and steady state input current for some points selected from Pareto Front are shown in Fig. 6. All of these results are optimum but according to the some other technical priorities, any of them can be chosen. As seen in the Fig. 5, all the black points in the Pareto Front dominate the conventional point. When still less input current THD is needed, gray points can be selected.

5. Conclusion

For a PFC rectifier, Input current THD and start-up response are conflicting features, so a Multi-Objective optimization method such as Strength Pareto algorithm can be useful in improving them simultaneously. In this paper, these conflicting features of Boost based PFC rectifier were defined as the objective functions and optimized while the PI coefficients in the indirect current control scheme were design variables. By the help of Pareto Set and Pareto Front which are offered in the paper, designer can easily choose any of the results based on the features which he expect of the PFC rectifier.

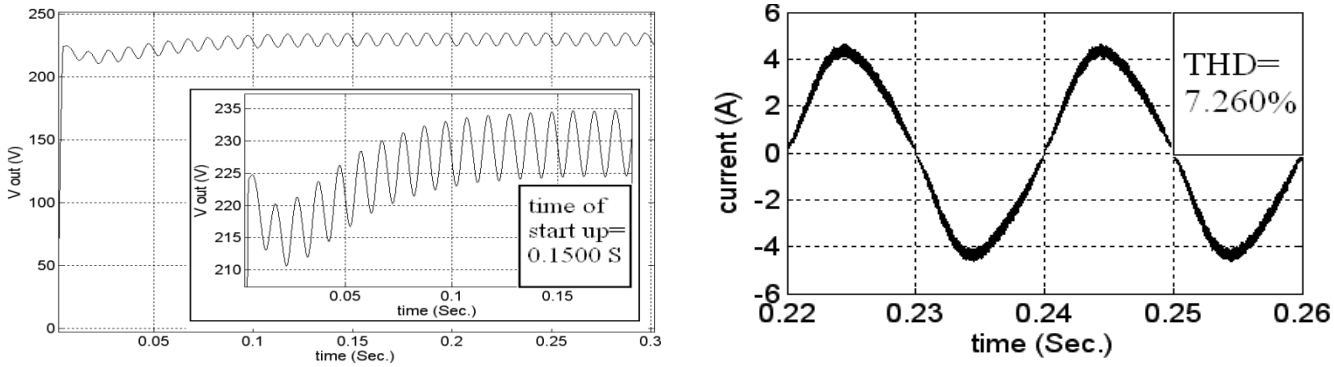

Fig. 3. Start up response and steady state input current of PFC rectifier with conventional PI gains (KPI=4.8, TPI=26ms), current THD equals 7.26% and time of startup response is 150 ms

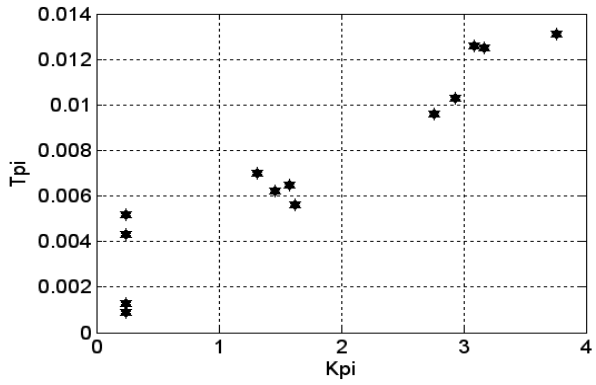

Fig. 4. Pareto Optimal Set

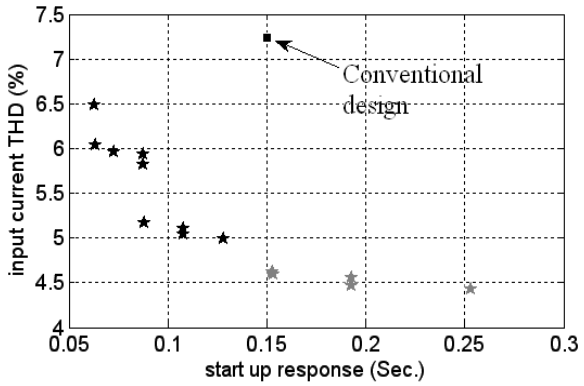

Fig. 5. Pareto Optimal Front

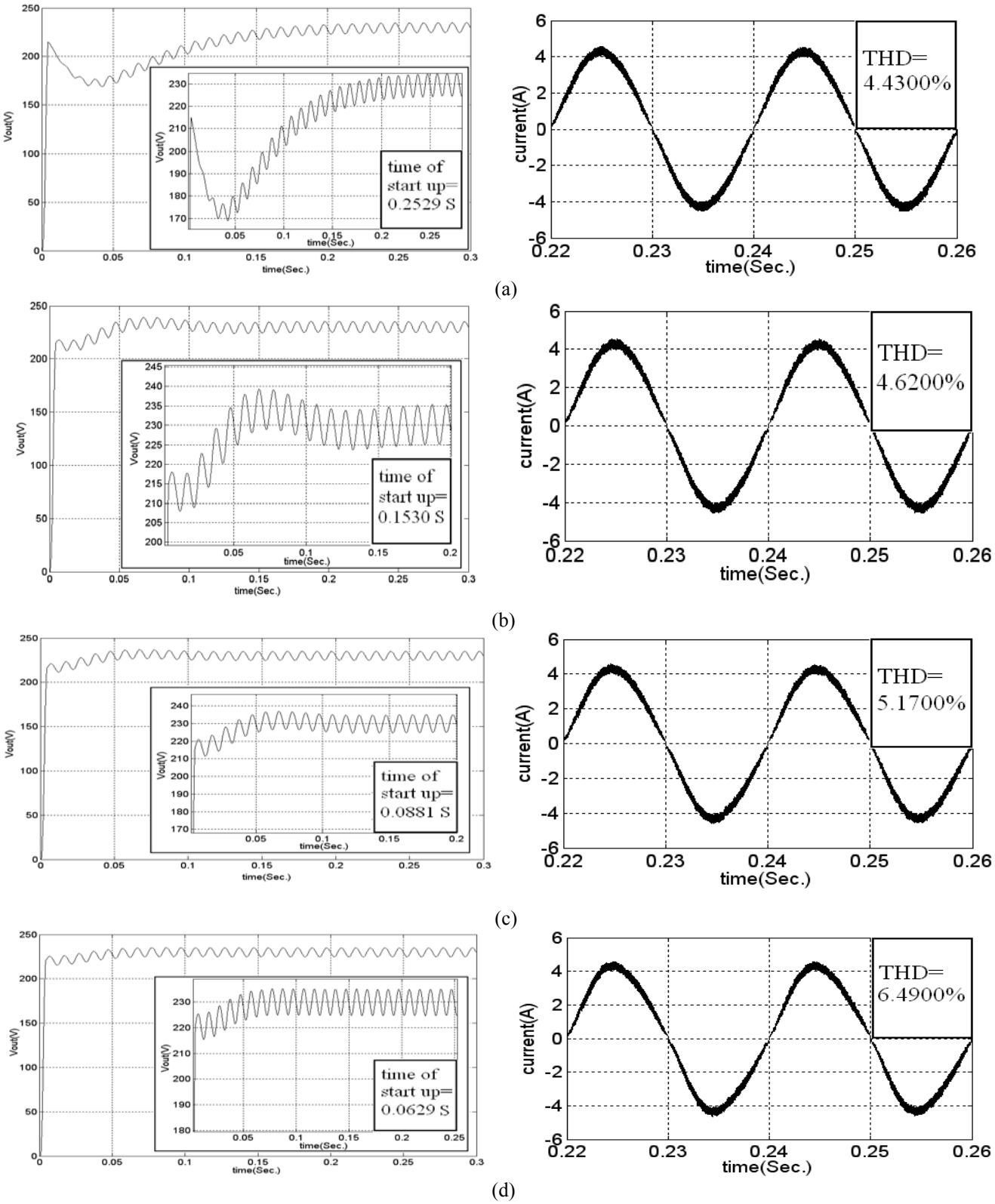

Fig. 6. Startup response and steady state input current for some points selected from Pareto Front, (a) case 14, (b) case 10, (c) case 6, (d) case 1

Table I. - Pareto Set (PI controller coefficients) and Pareto Front (input current THD and time of start-up response)

CASE	K_{PI}	T_{PI}	START UP RESPONSE (SEC.)	INPUT CURRENT THD (%)
1	3.7589	0.0131	0.0629	6.4900
2	3.1699	0.0125	0.0632	6.0400
3	3.0859	0.0126	0.0728	5.9600
4	2.9285	0.0103	0.0875	5.9300
5	2.7634	0.0096	0.0877	5.8200
6	1.6210	0.0056	0.0881	5.1700
7	1.5749	0.0065	0.1079	5.1000
8	1.4587	0.0062	0.1080	5.0400
9	1.3099	0.0070	0.1280	4.9900
10	0.2400	0.0009	0.1530	4.6200
11	0.2400	0.0009	0.1531	4.6000
12	0.2400	0.0013	0.1927	4.5500
13	0.2400	0.0043	0.1928	4.4600
14	0.2400	0.0052	0.2529	4.4300

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