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Evaluation of custom-designed lateral power transistors in a silicon-on-insulator process in a synchronous buck converter

Sinan Okumus *, Lin Fan*, Yasser Nour *, Arnold Knott*
*Department for Electrical Engineering,
Technical University of Denmark,
Elektrovej, building 325,
2800 Kongens Lyngby, Denmark
Email: 120042@student.dtu.dk, linfan@elektro.dtu.dk, ynour@elektro.dtu.dk, akn@elektro.dtu.dk

***Abstract*—Most of todays power converters are based on power semiconductors, which are built in vertical power semiconductor processes. These devices result in limited packaging possibilities, which lead to physically long galvanic connections and therefore high external electromagnetic fields. These fields compromise power quality significantly. Therefore this paper examines the possibility to use lateral silicon-on-insulator power MOSFETs and uses the custom-made devices in a $48\ \mathrm{V}$ to $12\ \mathrm{V}$ synchronous buck converter in continuous conduction mode. The converter is designed based on custom made power transistors, implemented and verified by experimental results. The resulting efficiency of the $1\ \mathrm{W}$ converter is around $93\ \%$ across a wide load range and its temperature rise is less the $10\ ^{\circ}\mathrm{C}$. This leads to the conclusion, that modern lateral silicon-on-insulator power processes allow high integration of power stages and therefore promise lower emissions, leading to higher power quality.**

***Index Terms*—power semiconductors, vertical semiconductor process, lateral semiconductor process, silicon-on-insulator process, buck converter**

I. Introduction

Modern power semiconductor transistors are often constructed as vertical devices. [1]–[3] The advantage of vertical devices are very low on-resistances $R_{DS_{on}}$ in combination with low gate charges Q_g, therefore resulting in a low figure of merit FOM, where $FOM = R_{DS_{on}} \cdot Q_g$. The FOMs of several processes can be compared to each other for a given maximum device voltage, as a bigger gate area increases the width of the channel, therefore effectively reducing its $R_{DS_{on}}$, but negatively affecting the gate charge Q_g due to the increased plate areas of the gate facing the channel. These plates effectively create the input capacitance C_{iss} and represent the gate charge Q_g.

Within all other integrated circuit design areas, such as Complementary Metal Oxid Semiconductors (CMOS), such as [4]–[7], lateral devices are state-of-the-art. Figure 1 shows a simplified representation of a vertical and a lateral Metal Oxid Semiconductor Field Effect Transistor (MOSFET).

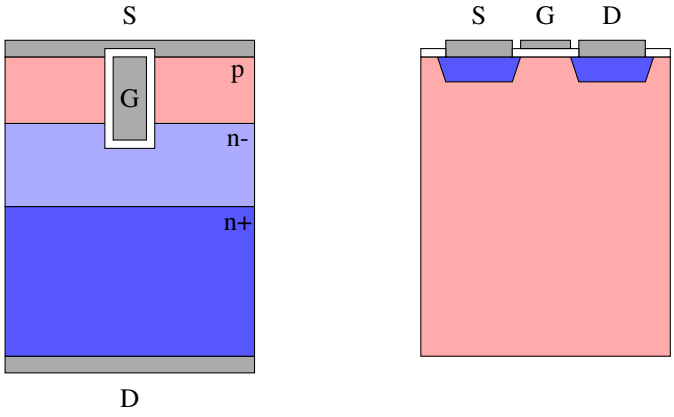

Fig. 1. Simplified example of crosssection of the die of a vertical (left side) and a lateral (right side) power n-channel MOSFET, where D is drain, G is gate and S is source. The coloring and n+, n- and p are indicating the doping of the semiconductor. The bulk connection in the lateral device is neglected.

The vertical n-channel device on the left side of Fig. 1 is using the whole die thickness and the n-doped wafer provides plenty of electrons to be flushed into the channel, when attracted by a positive potential applied between gate (G) and (S) source, hence a low resistance between drain (D) and source (S), i.e. low $R_{DS_{on}}$.

The lateral device on the right side of Fig. 1 is built on a p-doped wafer, where the number of free electrons to be attracted to the channel between drain (D) and and source (S) are rather low. However in this case, the backside of the die - called bulk (B) - has no electrical function and is typically tied to the lowest potential of the implemented circuit, which is the

source of the power MOSFET in this case.
For building a power stage, many power converter topologies, such as synchronous buck, synchronous boost, half-bridge and full-bridge, require two stacked power transistors. These stacked power transistors are the power stage inside those topologies and are called half-bridge or switching pole. Figure 2 shows such a half-bridge configuration.

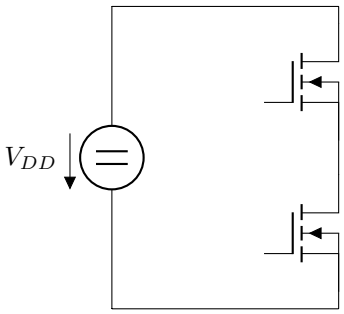

Fig. 2. Half bridge switch-mode power stage realized with two n-channel MOSFETs.

When connecting two vertical MOSFETS in such a half-bridge configuration, the top-metallization of the low-side device is connected to ground and the backside metallization of the other die is connected to the supply voltage V_{DD}. Furthermore, the backside of the die of the low-side MOSFET needs to be shorted to the topside of the high-side MOSFETs die. This node is the switch node, which is carrying a high $\frac{dI}{dt}$ and $\frac{dV}{dt}$. Figure 3 is visualizing these connections.

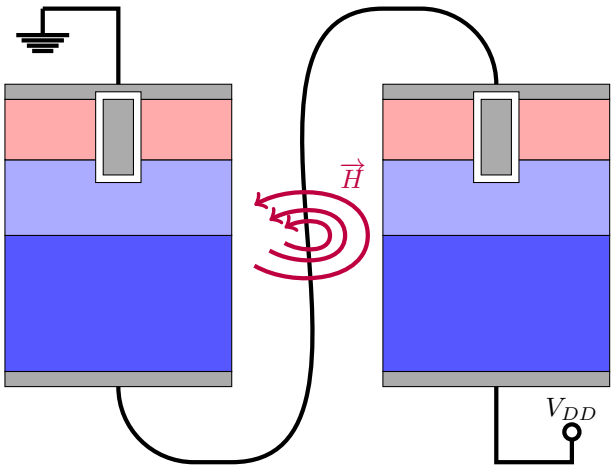

Fig. 3. Parasitics inductance and resulting magnetic field through connection of two vertical MOSFETs in a half bridge configuration

Especially the $\frac{dI}{dt}$ running in this connection generates a magnetic field $\vec{H}$, which is defined by equation 1:

$$\vec{H} = \oint \frac{dI}{dt} dl. \tag{1}$$

If the path l, which the alternating current (AC) is flowing along, is long, the area between the forward and the return path of the loop is big and therefor the integral on the right side of the equation is big.
In the case of vertically implemented MOSFETs, the physical path, where this current flows is rather large, as it consists of a number of mechanical connections:

- drain connection of die of low-side device
- package
- printed circuit board
- source pin of high-side device
- lead frame of high side device
- source bonding wire of high-side device
- routing in metal of high-side source

Therefore the resulting $\vec{H}$-field is rather big, which results in a significant contribution to radiated electromagnetic emissions, which can potentially couple into other circuits in the same system [8] or even worse getting emitted outside the mechanical enclosure of the system. This compromises the radiated electromagnetic compatibility (EMC) significantly and therefore compromises the power quality of the system.
When connecting lateral power devices in a half-bridge configuration as provided in Fig. 2, the high-side device needs to be isolated from the die-substrate, the bulk, which is accomplished by modern silicon-on-insulator processes (SOI). Such an arrangement is visualized in figure 4.

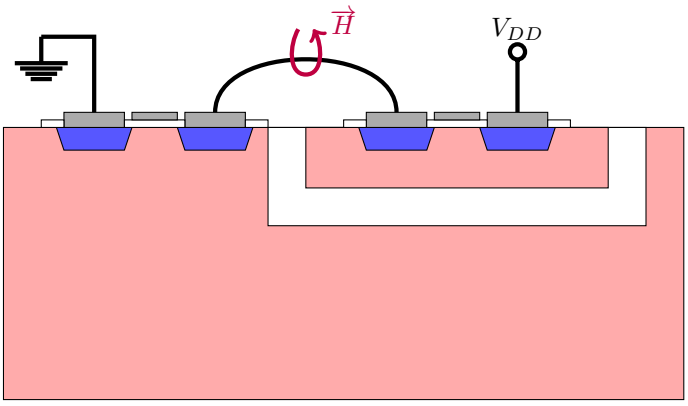

Fig. 4. Parasitics inductance and resulting magnetic field through connection of two lateral MOSFETs in a half bridge configuration

Compared to the routing of the switch-node in vertical devices, the alternating current in the lateral configuration only needs to be routed inside the metallization layers on top of the active silicon and does neither leave the package nor the die. Therefore the forward and the return path of the loop, penetrated by the alternating current is rather short, resulting in a significantly reduced $\vec{H}$-field.
As initially mentioned, the increased on-resistance of the vertical devices compared to the vertical counterparts, is their largest drawback. Therefore this paper focuses on the usability of lateral devices in power converters with respect to achievable efficiency. Section II introduces the custom made lateral SOI devices used in section III in a synchronous buck

converter design. Section IV shows the achieved experimental results and section V concludes the paper.

II. Custom Made Lateral Power Devices in Silicon-On-Insulator Process

The design procedure and layout extracted results for the four designed lateral power MOPSFETs in a 180 nm SOI high voltage process is given in [9] and [10]. The resulting on-resistances of the two bigger devices are in the 2.5 Ω-range and the two smaller devices achieve around 3 Ω. Figure 5 provides the top-view of the designed devices, revealing their aspect ratio and their relative sizes. Furthermore, the bonding diagram is included in Fig. 5.

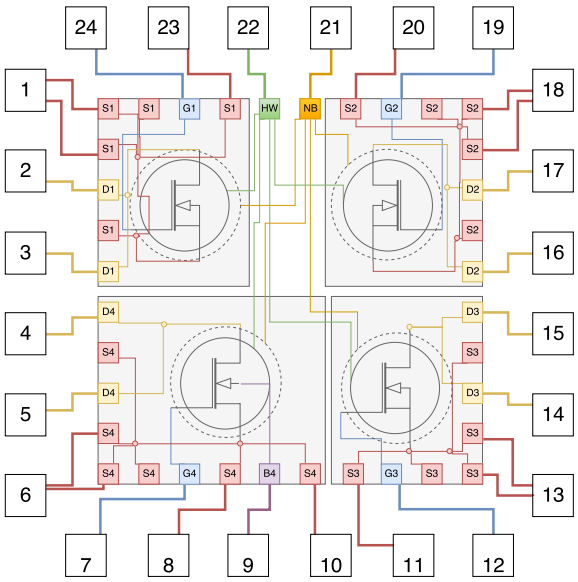

Fig. 5. Bonding diagram and top-view of the layout of the test MOSFETs

Figure 6 shows the packaged devices with open lid after soldering on a test printed circuit board (PCB). Here the aspect and size ratio of the two uper MOSFETs compared to both lower MOSFETs is even more visual, corresponding to the approximately 0.5 Ω difference in on-resistance between the respective drain and source connections, when the gate-source voltage is above the devices threshold voltage.

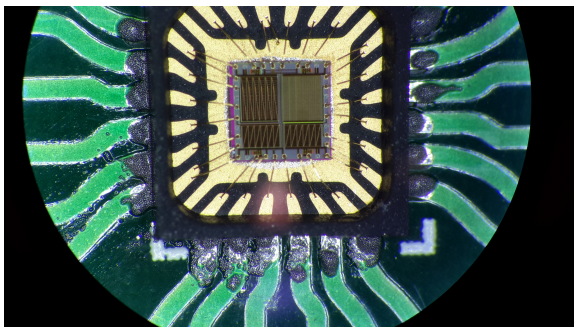

Fig. 6. Die photograph, when mounted on a printed circuit board (PCB).

III. Design of Synchronous Buck Converter

The synchronous buck converter is designed to fullfil the specifications given in table I.

TABLE I
Specifications for Synchronous Buck-Converter Based on the SOI MOSFETs

Parameters	Value
Input Voltage V_{in}	48 V
Output Voltage V_{out}	12 V
Maximum output power $P_{out_{max}}$	$\geq$ 1 W
Switching frequency f_{sw}	100 kHz
Output voltage ripple ΔV_{out}	$\leq$ 500 mV
Operation mode	continuous at $P_{out_{max}}$

These specifications result in an output current I_{out} of

$$I_{out_{max}} = \frac{P_{out_{max}}}{V_{out}} = 83 \text{ mA}, \tag{2}$$

which results in an equivalent load resistance R_{load} of

$$R_{load_{min}} = \frac{V_{out}}{I_{out_{max}}} = 144 \ \Omega. \tag{3}$$

To keep the converter in continuous conduction mode [11] at the maximum power level $P_{out_{max}}$, the output inductor L_{out} must fullfil

$$L_{out} \geq \frac{(1-d)R_{load_{min}}}{2 \cdot f_{sw}} = 540 \ \mu\text{H}, \tag{4}$$

where d is the duty cycle of the buck converter in continuous conduction mode, derived as $d = \frac{V_{out}}{V_{in}} = 0.25$. The 820 µH inductor MSS1278-824KL with ±10 % tolerance and a maximum series resistance of 1.296 Ω from Coilcraft satisfies the design criteria. The contribution of the inductors DC resistance to the losses in the converter is therefore limited to 9 mW and an inductor ripple current $\Delta I_{L_{out}}$ of

$$\Delta I_{L_{out}} = \frac{(1-d)V_{out}}{f_{sw} \cdot L_{out}} = 110 \text{ mA}. \tag{5}$$

The contribution of the switching losses of the inductor are estimated in the approximate same range to 10 mW.
To keep the output ripple within the requirement an output capacitor C_{out} of

$$C_{out} \geq \frac{\Delta I_{L_{out}}}{4 \cdot f_{sw} \cdot \Delta V_{out}} = 550 \text{ nF} \tag{6}$$

is needed, where the design choice for C_{out} is a 590 nF ceramic X7R capacitor with 50 V rating. The losses in the equivalent series resistance of the output capacitor are negligible.
The half-bridge needs a gate driver. Here the design choice is an L5113 with a maximum power dissipation of 15 mW.
The completed design results in full schematic in Fig. 7 including all decoupling capacitors and the inputs to the gate driver.

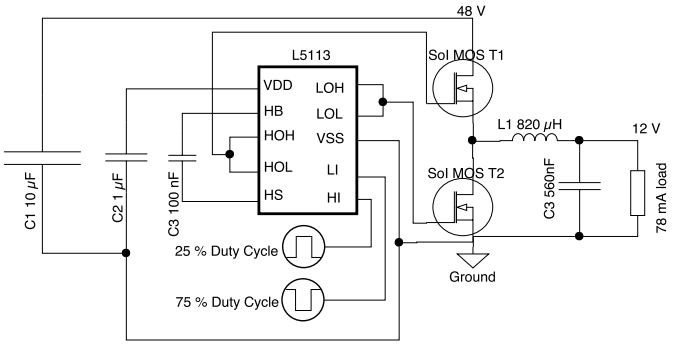

Fig. 7. Total schematic of the implemented synchronous buck converter.

Figure 8 shows a picture of the implemented prototype.

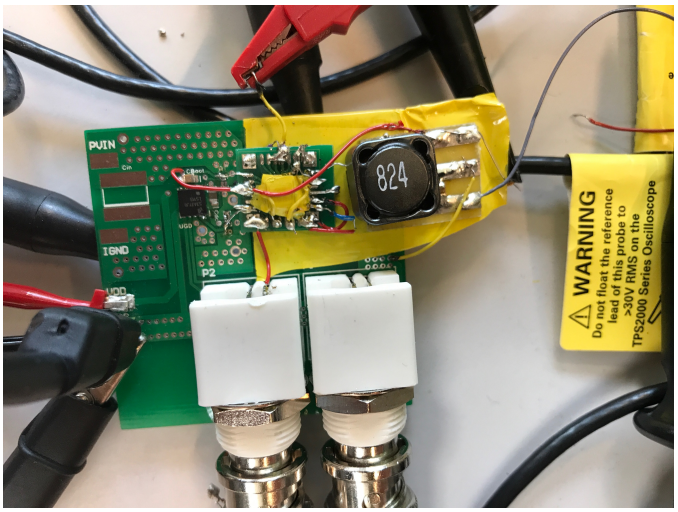

Fig. 8. Photograph of the implemented synchronous buck prototype with the test chip under yellow isolation take, the gate drive signals fed through the white BNC connectors at the bottom and the output inductor on the right side.

IV. Experimental Results

The block diagram of the experimental verification setup is provided in Fig. 9.

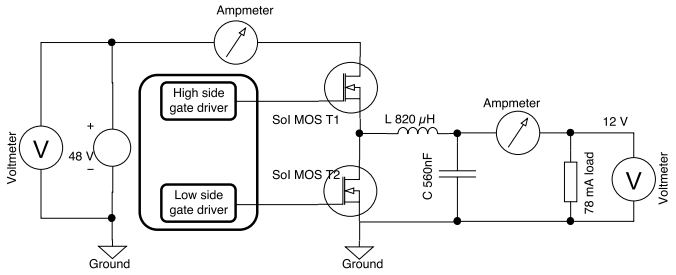

Fig. 9. Block diagram of setup to verify the usability of lateral SOI-based MOSFETs in the designed synchronous buck converter.

Figure 10 shows the laboratory setup, where the function generator Rigol DG4062 provides the gate signals and the active load ELA250 from Zentro Elektrik functions as the load resistor.

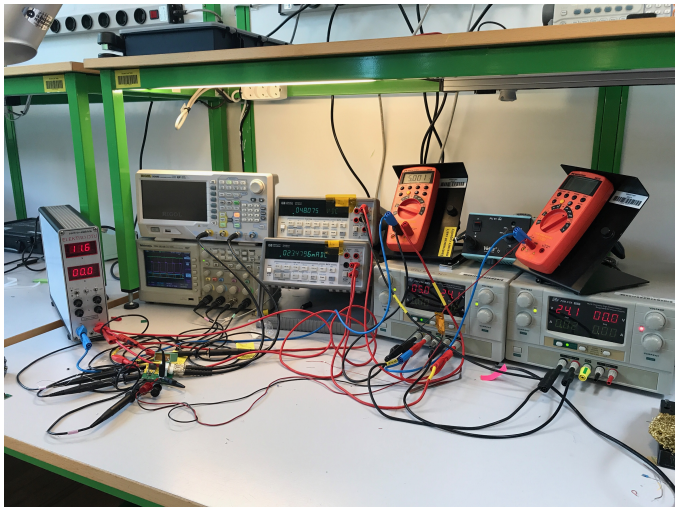

Fig. 10. Photograph of laboratory setup including - from left to right - the active load, the prototype, the function generator, the multimeters and the supplies for the input voltage as well as the auxiliary supply for the gate driver.

The correct operation of the buck converter is confirmed by measuring the switch node, e.g. the connection of the low-side MOSFETs drain to the high-side MOSFETs source, while monitoring the output voltage. Fig. 11 shows a screenshot of the oscilloscope measurement. The output voltage V_{out} is 12.0 V, the average voltage of the switching node is 12.5 V, while the converter is operating at 100.0 kHz. The overswing on the switch-node are an artifact of the applied measurement technique, resulting from the coupling of magnetic fields into the loop of the ground clip of the oscilloscopes probe.

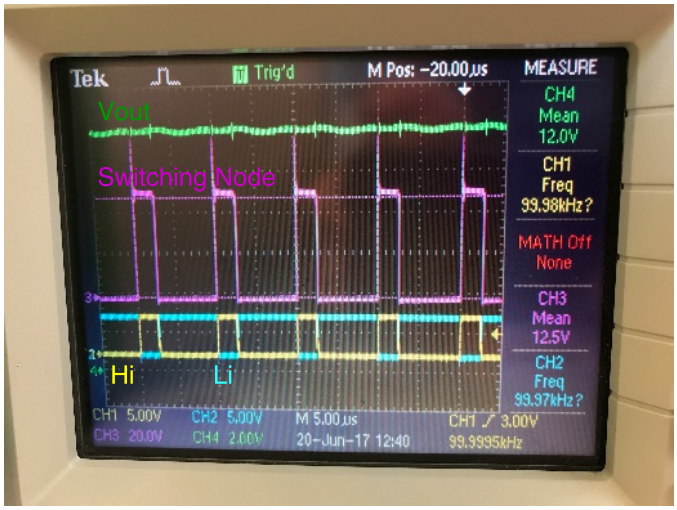

Fig. 11. Verification of the operation of the synchronous buck converter based on custom made lateral SOI power MOSFETs. From top to bottom: output voltage (green, 2 V/div), switch node (purple, 20 V/div), low-side input to the gate driver (cyan, 5 V/div) and its high-side input (yellow, 5 V/div) with a time base of 5 µs/div

The most important parameter to verify the usability of lateral power MOSFETs in switch-mode power stages to reduce the

external fields and therefore improve the overall power quality of the converter is its achievable efficiency. The losses in the passive components, i.e. the output inductor and the output capacitor, as well as the losses in the gate drive are minimized by design. This leaves the switching and conduction losses in the power devices as the determining factor of efficiency, as the parasitic capacitances of the power devices are responsible for the switching losses and the on-resistance dominates the conduction losses. Hence the definition of the FOM. Figure 12 represents the final quantitive representation of the losses in the converter.

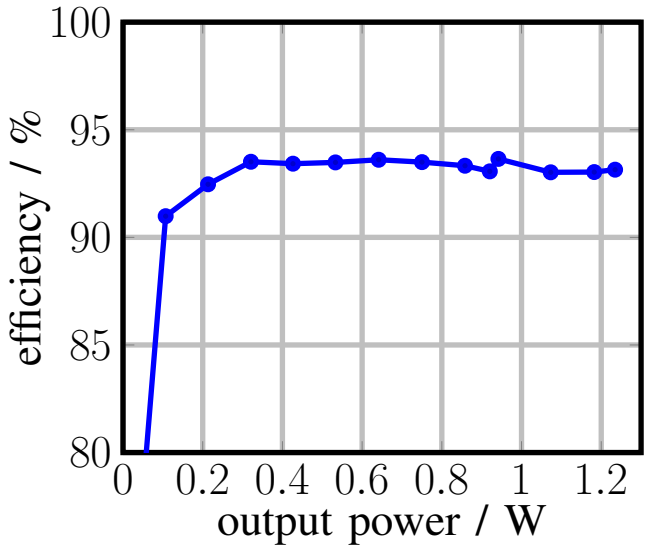

Fig. 12. Measured efficency of the implemented buck converter

Over a wide power range (from 10 % of $P_{out_{max}}$ to $P_{out_{max}}$), the converter operates above 90 % and at more than 300 mW the efficiency is around 93 %. This leaves about 70 mW to losses, of which 34 mW have been accounted for in the gate driver (15 mW) and the output inductor (19 mW) by design above. The remaining 36 mW of losses are expected in the power semiconductors.

The thermal image of the converter confirms the power semiconductors as the highest components with the highest temperature. Given their physical volume and the fact that they dissipate about half of the total losses, this is expectable. As the highest temperature of the converter in thermal equilibrium is 34.6 °C, only 8.9 °C above the ambient temperature of 25.7 °C, the overall performance of the converter is acceptable for many applications. Given a maximum operating temperature of silicon devices at 150 °C and adding a small safety margin, this design can be qualified up to an ambient temperature of 140 °C, which is enough for most consumer, industrial, automotive and space applications.

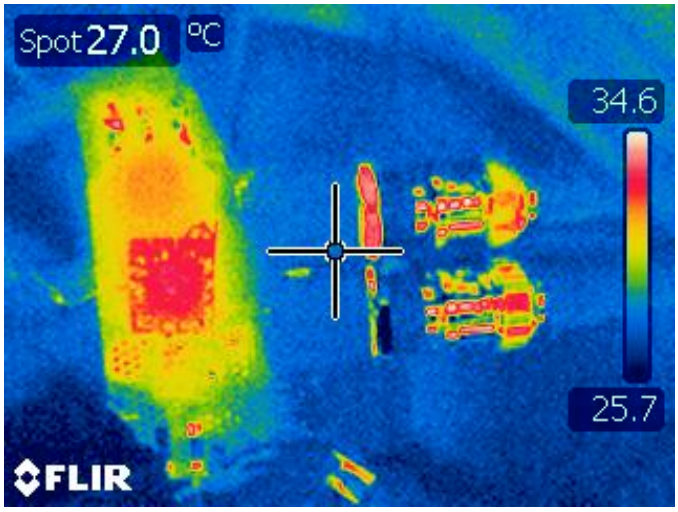

Fig. 13. Thermal image of the synchronous buck converter under operation: the highest temperature rectangle to the left of the cursor represents the tested custom made lateral SOI power MOSFETs, whereas the hot spots to the right of the cursor are the BNC connectors - which might represent a wrong temperature due to the reflective nature of their surface with respect to the infrared cameras measurement technique.

V. Conclusion

Lateral power semiconductors are proposed as a method to reduce emitted magnetic fields compared to the widely used vertical power devices. To check the feasibility of the lateral devices, their useability in power converters needs to be examined. This paper used custom made silicon-on-insulator lateral power MOSFETs to determine the applicability of the selected process in power electronics. A 48 V to 12 V, 1 W synchronous buck converter was designed and experimentally verified. The experimental results show a high efficiency (around 93 %) over a wide load range and a temperature rise of less than 10 °C, proofing that lateral silicon-on-insulator power MOSFETs are a serious alternative to vertical devices.

Acknowledgements

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References

[1] B Jayant Baliga. *Fundamentals of power semiconductor devices*. Springer Science & Business Media, 2010.

[2] B Jayant Baliga. *Advanced power MOSFET concepts*. Springer Science & Business Media, 2010.

[3] Josef Lutz, Heinrich Schlangenotto, Uwe Scheuermann, and Rik De Doncker. *Semiconductor Power Devices: Physics, Characteristics, Reliability*. Springer-Verlag Berlin Heidelberg, 2011.

[4] Yoni Yosef-Hay, Dennis Øland Larsen, Pere Llimós Muntal, and Ivan HH Jørgensen. Fully integrated, low drop-out linear voltage regulator in 180 nm cmos. *Analog Integrated Circuits and Signal Processing*, 92(3):427–436, 2017.

[5] Pere Llimós Muntal, Ivan HH Jørgensen, and Erik Bruun. A continuous-time delta-sigma adc for portable ultrasound scanners. *Analog Integrated Circuits and Signal Processing*, 92(3):393–402, 2017.

[6] Pere Llimós Muntal, Erik V Thomsen, et al. Transmitting performance evaluation of asics for cmut-based portable ultrasound scanners. In *Ultrasonics Symposium (IUS), 2017 IEEE International*, pages 1–4. IEEE, 2017.

[7] Dennis Øland Larsen, Martin Vinter, et al. Switched capacitor dc-dc converter with switch conductance modulation and pesudo-fixed frequency control. In *ESSCIRC 2017-43rd IEEE European Solid State Circuits Conference*, pages 283–286. IEEE, 2017.

[8] Elena Baikova, Stanimir Valtchev, Rui Melicio, and Vtor M Pires. Electromagnetic interference from a wireless power transfer system: Experimental results. *Renewable Energy & Power Quality Journal*, 1(14):1–5, 05 2016.

[9] Lin Fan, Arnold Knott, and Ivan Harald Holger Jorgensen. Nonlinear parasitic capacitance modelling of high voltage power mosfets in partial soi process. *Elektronika ir Elektrotechnika*, 22(3):37–43, 2016.

[10] Lin Fan, Arnold Knott, and Ivan Harald Holger Jørgensen. Layout capacitive coupling and structure impacts on integrated high voltage power mosfets. In *Ph. D. Research in Microelectronics and Electronics (PRIME), 2016 12th Conference on*, pages 1–4. IEEE, 2016.

[11] Ned Mohan. *First Course on Power Electronics*. MN Power Electronics (MNPERE), Minneapolis, 2009 edition, May 2009.