

# A 380 V High Efficiency and High Power Density Switched-Capacitor Power Converter using Wide Band Gap Semiconductors

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**Abstract.** State-of-the-art switched-capacitor DC-DC power converters mainly focus on low voltage and/or high power applications. However, at high voltage and low power levels, new designs are anticipated to emerge and a power converter that has both high efficiency and high power density is highly desirable. This paper presents such a high voltage low power switched-capacitor DC-DC converter with an input voltage up to 380 V (compatible with rectified European mains) and an output power experimentally validated up to 21.3 W. The wide band gap semiconductor devices of GaN switches and SiC diodes are combined to compose the proposed power stage. Their switching and loss characteristics are analyzed with transient waveforms and thermal images. Different isolated driving circuits are compared and a compact isolated half-bridge driving circuit is proposed. The full-load efficiencies of 98.3% and 97.6% are achieved for the power stage and the complete power converter, without heatsink or airflow. The corresponding power densities are 7.9 W/cm<sup>3</sup> and 2.7 W/cm<sup>3</sup>, based on boxed volumes, respectively.

## Key words

Switched capacitor circuits, DC-DC power converters, Gallium nitride, Silicon carbide, Wide band gap semiconductors.

## 1. Introduction

Industrial and consumer electronics keeps demanding smaller and lighter power supplies [1]. One of the principle approaches is to design power converters that consist of switches and capacitors. Research on switched-capacitor circuits has been commenced since 1930s [2]. Afterwards, switched-capacitor converters have been investigated for memory applications on IC (Integrated Circuit) in 1970s [3]. Research on state-of-the-art switched-capacitor DC-DC converters has focused on low voltage and/or high power applications, majority of which are implemented on ICs [4]-[6]. For switched-capacitor power converters that have voltage and power levels above 12 V and 2 W, discrete power converters are commonly implemented by academia [8],[9] and industry [10]. Recent advances in switched-capacitor DC-DC

power converters are up to a 200 V input voltage with output powers of 30-53 W [11],[12]. Switched-capacitor DC-DC power converters at further higher input voltage and lower output power level are anticipated to emerge. This paper presents a 380 V input voltage (compatible with European 220-240 Vrms AC operation with  $\pm 10\%$  tolerance) switched-capacitor DC-DC power converter, which is intended to be used as the voltage conversion stage for LED (light-emitting diode) drivers. This paper focuses on the high efficiency and high power density design of the complete power converter (i.e. the power stage with the driving circuit included). For high voltage, low current applications, the switching loss becomes significant. The wide band gap semiconductors, i.e. GaN (Gallium Nitride) switches and SiC (Silicon Carbide) diodes are combined to properly address both conduction loss and switching loss, in order to achieve both high efficiency and high power density.

This paper presents a switched-capacitor DC-DC power converter that consists of a power stage and its driving circuit. The target is to achieve both high efficiency and high power density for the complete power converter. In section 2, the proposed power stage and its basic operation principle is introduced. The consideration of the off-state leakage is also elaborated and discussed. In section 3, different driving circuit topologies are analyzed and compared. An isolated half-bridge driving circuit is chosen to achieve high power density. In section 4, the complete power converter is implemented. The choice of the components and the PCB design considerations are illustrated. In section 5, the proposed power converter is experimentally validated. The measurement methods and results are presented. Thermal images and oscilloscope waveforms are used to analyze and compare the behavior of the wide band gap semiconductors. The measured efficiency and power density of the prototype converter are summarized. Section 6 concludes the paper.

## 2. Power Stage

The power stage is the core design of the complete power converter. The proposed power stage is shown in Fig. 1.

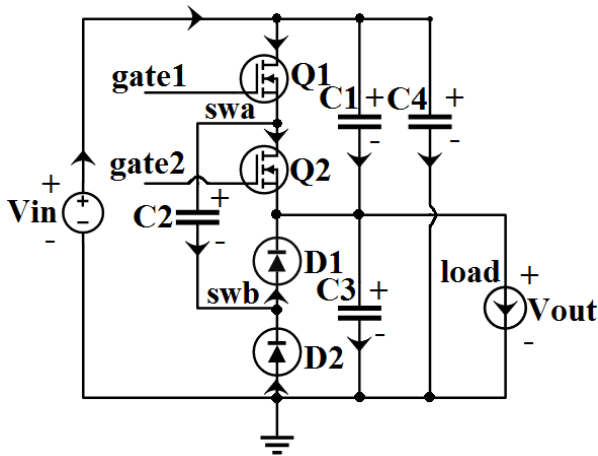


Fig. 1. Proposed power stage of switched-capacitor DC-DC converter for high voltage low power applications

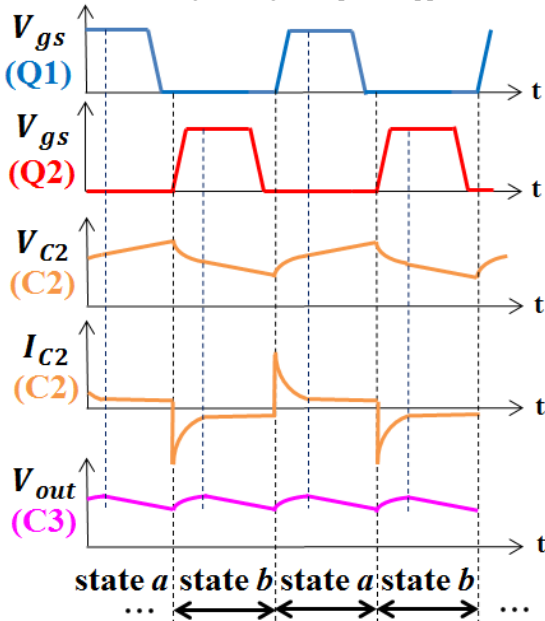


Fig. 2. Key waveforms of the proposed power stage (two main operation states are annotated with state *a* and stage *b*)

The power stage has a DC-DC voltage conversion ratio of 2:1 from the input voltage to the output voltage. It consists of two switches ( $Q1$ ,  $Q2$ ), two diodes ( $D1$ ,  $D2$ ), and four capacitors ( $C1$ - $C4$ ). The switches  $Q1$  and  $Q2$  are the main control devices. The diodes  $D1$  and  $D2$  facilitate the charge transfer to and from the capacitor  $C2$ , with  $Q1$  and  $Q2$ , respectively. The capacitors  $C1$  and  $C3$  serve as both input and output capacitors while balancing the charge transfer loops. The capacitor  $C4$  adds further decoupling capability (in addition to  $C1$  and  $C3$ ) to filter out high frequency noise of the input supply. This topology is in contrast to the conventional all-transistors switched-capacitor DC-DC converters. For high characteristic impedance (high voltage, low current) applications, by analyzing the direction of the current flow, some of the switches may suitably be implemented with diodes, which reduces switching loss and gating loss while constraining conduction loss. Therefore, high efficiency and high power density can be achieved with the proposed power stage, while the ultimate trade-off between the efficiency and the power density depends on the components used to implement the power converter and the PCB design.

The waveforms of the proposed power stage are shown in Fig. 2. The power stage operates with complementary fixed 50% duty cycle gate-source signals for the two switches  $Q1$  and  $Q2$ . There is a slight dead time between the two gate-source signals. The optimal dead time is tuned for optimizing the efficiency. The dead time cannot to be too long, to avoid the transient period when the output current is solely provided by the output capacitors ( $C1$ ,  $C3$ ), which further reduces the efficiency of the energy transfer of the power stage. A too short dead time is also not desired, to prevent shoot-through loss. An undesired shoot-through condition can also be triggered by improper dead time timing, together with the parasitic capacitances, resistances and inductances of the transistors, gate drivers, packages and PCB layout, where a switch under turning-off transients can suffer from the  $dv/dt$ -induced turn on and the  $di/dt$ -induced turn on [13].

The basic operation principle of the power stage is identified with two operating states (state *a*, state *b*). In state *a*, the pair  $Q1/D1$  is on and the pair  $Q2/D2$  is off, the energy transfer capacitor  $C2$  is charged while providing the load current. In state *b*, the pair  $Q2/D2$  is on and the pair  $Q1/D1$  is off, the energy transfer capacitor  $C2$  is discharged to supply the load current. The capacitors  $C1$  and  $C3$  always charge and discharge in opposite ways because the sum of their voltages equals to the input voltage. During each of the state *a* and the state *b*,  $C3$  charges then discharges while  $C1$  discharges then charges. Therefore, the output voltage ripple of the power stage is at the double frequency of the switching frequency of the switches  $Q1$  and  $Q2$ . Due to the charge balance of the energy transfer capacitor  $C2$  in steady state, the average current of  $C2$  equals to zero.

$$I_{C2} = \frac{1}{T_s} \int_0^{T_s} i_{C2} \cdot dt = 0 \quad (1)$$

However, the current flows through  $C2$  in opposite directions for each of the 50% duty cycles. The average of the absolute current of  $C2$  equals to the DC output current.

$$|I_{C2}|_{avg} = \frac{1}{T_s} \int_0^{T_s} |i_{C2}| \cdot dt = \frac{1}{T_s/2} \int_0^{T_s/2} |i_{C2}| \cdot dt = I_{out} \quad (2)$$

Considering the current of  $C2$  conducts through either the pair  $Q1/D1$  or the pair  $Q2/D2$  during a 50% duty cycle period, the average current of these devices is half of the output DC current.

$$I_{Q1} = I_{D1} = I_{Q2} = I_{D2} = \frac{1}{T_s} \int_0^{T_s/2} |i_{C2}| \cdot dt = I_{out} / 2 \quad (3)$$

Then the peak-to-peak voltage ripple of  $C2$  can be calculated, which is shown to be inversely proportional to the capacitance of  $C2$  and the switching frequency, and it is proportional to the output load current.

$$\Delta V_{C2} = \frac{1}{C2} \int_0^{T_s/2} |i_{C2}| \cdot dt = \frac{(I_{out} / 2) \cdot T_s}{C2} = \frac{I_{out}}{2 \cdot C2 \cdot f_s} \quad (4)$$

It may seem that if designers choose  $C1$  and  $C3$  to have an equal capacitance value, then at no load condition when all switches are off, the capacitor divider of  $C1$  and  $C3$  may automatically balance the output voltage to be half of the input voltage. However, this does not happen in practice due to the leakage of the devices (in the  $\mu A$  range).

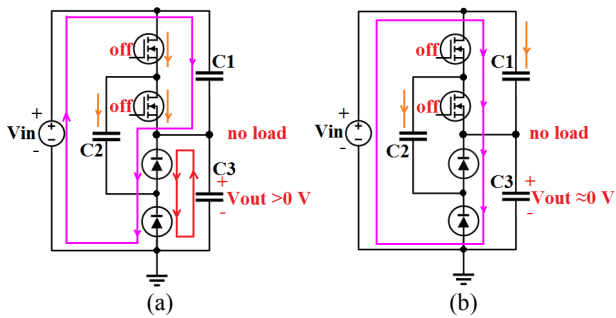


Fig. 3. Leakage current paths at no load condition when all switches are off (e.g. before start-up, or after turn-off). (a)  $C3$  is not fully discharged. (b)  $C3$  is fully discharged.

The main leakage paths are shown in Fig. 3 when an input voltage is applied to the circuit under discussion. In Fig. 3(a), there are still residual charges stored on  $C3$ , and these charges on  $C3$  are mainly discharged by the reverse current of the diodes. When  $C3$  discharges,  $C1$  is charged by the input supply, and the charge current also flows through the reverse biased diodes. The drain-source leakage current of the switches and the leakage current of  $C2$  are relatively small and may be negligible in this case. In Fig. 3(b),  $C3$  is fully discharged, and the majority of the leakage current passes through the switches and the diodes. These devices individually carry different leakage current and the bottom diode carries the highest leakage current. In either case of Fig. 3(a) and Fig. 3(b), the capacitor  $C1$  is eventually charged to the input voltage and has to withstand it. Therefore, the voltage rating of the capacitor  $C1$  (without adding extra component or circuitry) is determined by the input voltage, rather than its steady state operating voltages.

### 3. Driving Circuit

After the power stage is designed, designing its driving circuits is another challenge. The conventional bootstrap circuits are not suitable for the proposed power stage. First, the diodes  $D1$  and  $D2$  are utilized in the power stage to complete the charge transfer loops, and there are no conventional low-side switches that can be used to charge the high-side bootstrap capacitors. Second, though the load current might be used in series with the charge path of a bootstrap capacitor, the voltage of the highest bootstrap capacitor suffers most from the voltage drop of the bootstrap diodes [10], which may not ensure an adequate gate-drive voltage or even trigger an under-voltage lockout by its voltage ripple, which is in turn caused by transistor gate charge, driver supply bias current, transistor gate leakage, diode reverse leakage, and other leakage current [14].

The possible driving circuits for the proposed power stage are shown in Fig. 4. In Fig. 4(a), digital isolators are used in series with conventional low-side gate drivers [11],[15], to provide isolated high-side gate signals to the switches  $Q1$  and  $Q2$ . If each switch has its own digital isolator and gate driver, then 4 components are needed to drive 2 switches. In addition, if one pair of digital isolator and gate driver shares the same isolated supply, as shown in Fig. 4(a), then in total 6 components are required to complete the driving circuit.

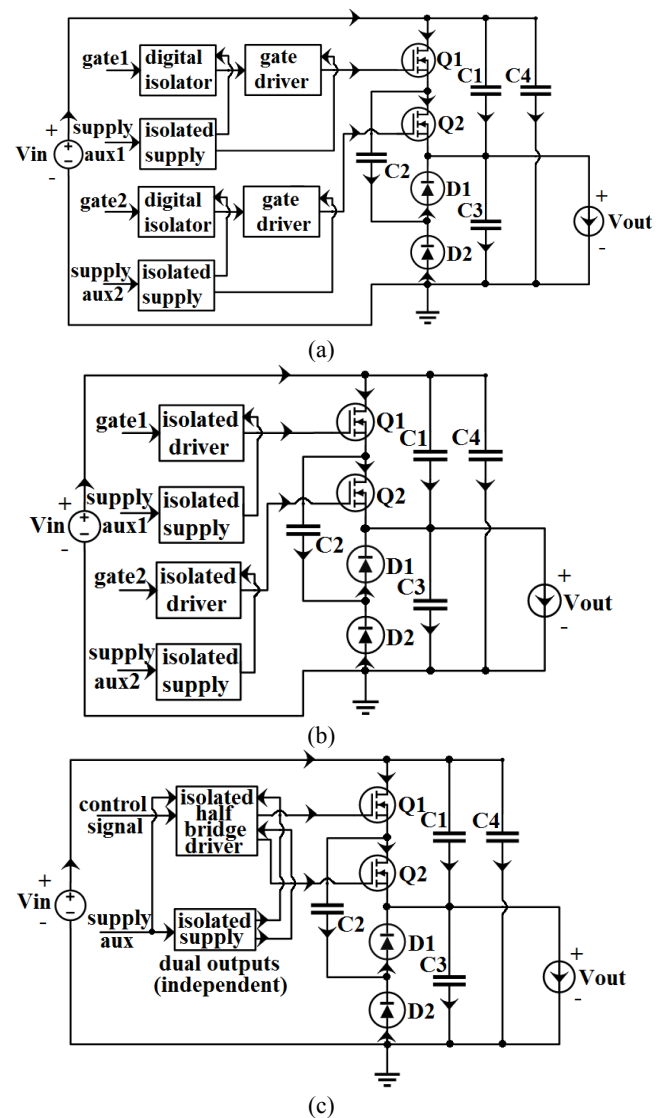


Fig. 4. Possible driving circuits for the power stage. (a) Using digital isolators with conventional low-side gate drivers. (b) Using single-channel isolated gate drivers. (c) Proposed driving circuit, using a single isolated half-bridge gate driver.

In Fig. 4(b), two single-channel isolated gate drivers are used to replace the corresponding two pairs of digital isolator and gate driver [16]. In this case, if each isolated gate driver has its own isolated supply, then in total 4 components are used to compose the driving circuit. To further improve the integration level thus the power density of the converter, the driving circuit in Fig. 4(c) is proposed. Because the switches  $Q1$  and  $Q2$  are driven complementary with fixed 50% duty cycle, as discussed in the previous section, the driving circuit for these two switches is suitable for implementation with an isolated half-bridge gate driver. Furthermore, an isolated supply with dual independent outputs is used to provide supplies for the individual outputs of the gate driver. As a result, with only 2 components the driving requirements of the power stage are fulfilled and high power density is thus achieved.

### 4. Implementation of Complete Converter

The complete power converter can now be synthesized with the power stage and the driving circuit.



Table I. Components for the prototype converter

Component	Technology	Specification
Switches <i>Q1, Q2</i>	Gallium Nitride (GaN)	EPC2012C, EPC 200 V, 5 A, 100 mΩ
Diodes <i>D1, D2</i>	Silicon Carbide (SiC)	C3D1P7060Q, CREE 600 V, 3.3 A, 4 nC
Capacitors <i>C1, C3</i>	Multi-Layer Ceramic Capacitor (MLCC)	450 Vdc, 1 μF, ±10% X7T, TDK
Capacitor <i>C2</i>	Multi-Layer Ceramic Capacitor (MLCC)	250 Vdc, 10x 1 μF, ±10% X7T, TDK
Capacitor <i>C4</i>	Multi-Layer Ceramic Capacitor (MLCC)	450 Vdc, 0.22 μF, ±20% X7T, TDK
Gate Driver	Capacitive-isolated (with dies)	SI8274GB1-IM, 4 A, 2.5 kVrms, Silicon Labs
Driver Supply	Inductive-isolated (with transformer)	R1DA-3.30505, 1 W, 1 kVdc, RECOM Power

A prototype of the switched-capacitor power converter is implemented with the key components listed in Table I. The switches *Q1* and *Q2* are GaN devices. The diodes *D1* and *D2* are SiC devices. The capacitors *C1-C4* are all ceramic capacitors. The isolated gate driver has pull-down transistors with 1.0 Ω equivalent on-resistance, and pull-up transistors with 2.7 Ω equivalent on-resistance, resulting in peak output current of 4.0 A and 1.8 A, respectively. It has a minimum CMTI (Common Mode Transient Immunity) rating of 150 V/ns, to facilitate the fast dv/dt transients of the GaN and SiC devices. The isolated power supply has dual independent outputs. Each of the outputs has a maximum output current rating of 100 mA, which is excessively over-designed for the converter and causes unnecessary low efficiencies operating at light load conditions, and the choice is due to the availability of the components.

All components are SMD (Surface-Mount Devices). The PCB of the prototype converter is designed with 2-layers (industry-standard conductor track widths, conductor spacing distances, and through hole diameters), where the components are mounted on both sides of the PCB, to minimize the charge transfer loops and the power loops. The thickness of the PCB is 1.0 mm, with trade-offs between parasitic inductance of vias, heat dissipation capability, cost and mechanical reliability. A copper thickness of 2 oz is used to trade-off conduction loss and solder joint reliability. The surface finish of ENIG (Electroless Nickel Immersion Gold) is used to improve the planarity and the fine-pitch capability of the copper pads for the LGA (Land Grid Array) devices, e.g. the isolated gate driver.

## 5. Experimental Results

The experimental setup of the test bench is shown in Fig. 5. The digital multimeters 34401A are employed for the efficiency measurements. For the highest accuracy of 34401A, the full 6½ digits resolution and the manual ranging are used. The prototype of the power converter under test is shown in Fig. 6. The default ground leads of the oscilloscope probes are not used because of the signal-ground loop inductances. Instead, local ground connections are custom-made to minimize the loops for more accurate transient measurements.

The measured efficiency of the power stage and the complete power converter is shown in Fig. 7, with a switching frequency of 1 kHz for the switches *Q1* and *Q2*. The total efficiency includes the power consumption of the driving circuit (i.e. the gate driver and the isolated supply), which is about 153-159 mW. All the efficiency measurements are made at the room ambient temperature, without any heatsink or any airflow. The full-load power stage efficiency is 98.3%, and the efficiency of the complete power converter at the full-load is 97.6%. The efficiency of the complete power converter at the 10%-100% load range is always above 90%. The efficiency is measured up to an output power of 21.3 W, which is limited by the multimeters rather than the converter itself. The reading accuracy of 34401A measuring a DC current with the 1 A range (0.1 Ω shunt resistor) is 5 times worse than with the 100 mA range (5 Ω shunt resistor) [17]. The accuracy of the measurement of the input and output power is highly demanded for the resulting maximum absolute error in the efficiency, where the losses are determined indirectly. A direct measurement of losses by means of a calorimeter [18] may be of consideration for high efficient power converters.

The measure peak temperature of the hottest spot on the PCB is also shown in Fig. 7. The efficiency increases with the output power at high temperatures. This is mainly caused by the temperature effects of the SiC diodes. SiC diodes typically have positive temperature coefficient at high current levels. However, at low current levels (as in the proposed high voltage low current power converter), the temperature coefficient of the SiC diodes becomes negative [19],[20], i.e. for a given forward current, the forward voltage becomes less at a higher temperature. This phenomenon happens for a limited low-forward-current range of the SiC diodes, and it contributes to reduce the conduction loss, which is the dominated loss at high output power levels for the proposed power converter.

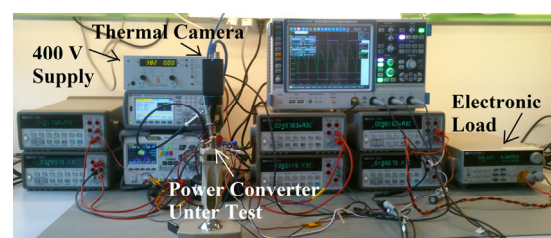


Fig. 5. Experimental setup of the test bench

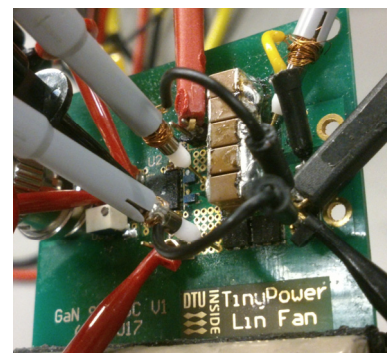


Fig. 6. Prototype converter under test (local ground connections are custom-made for oscilloscope probes)

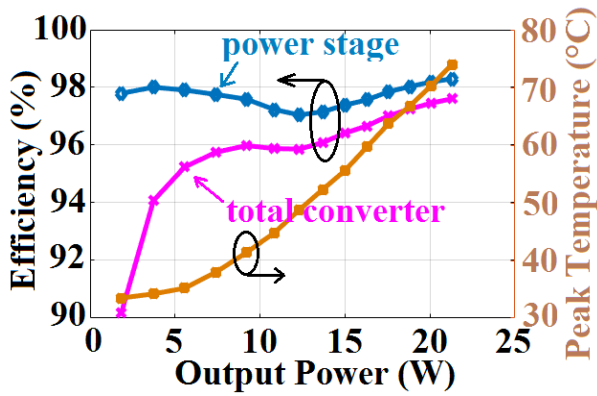


Fig. 7. Measured efficiency of the power stage and the complete power converter (including gate driver and isolated supply) vs. output power. No heatsink, no airflow, with the peak temperature of the hottest spot on the PCB.

This is further experimentally validated with thermal measurements. The thermal images of the power converter operating at 380 V input voltage and 21.3 W output power are shown in Fig. 8. In Fig. 8(a), the thermal image is measured after one hour full-power operation without any airflow. The peak temperature is 74.6 °C and the measured efficiency of the power stage is 98.3%. After adding forced airflow, the thermal image is measured again and shown in Fig. 8(b). The peak temperature is 57.5 °C, and the measured efficiency of the power stage is 97.8%. For the same constant load current of the power stage, the negative temperature coefficient of the SiC diodes increases the forward voltage drop at a low temperature, which increases the conduction loss and decreases the resulting efficiency.

The measured DC output voltage and the peak-to-peak output voltage ripple with respect to it versus the output current are shown in Fig. 9(a) and Fig. 9(b), respectively. As the output current rises, the conduction loss increases accordingly and the DC output voltage decreases for a given implementation of the power converter at a fixed switching frequency. The peak-to-peak output voltage ripple (thus the corresponding percentage with respect to the DC output voltage) rises as the output current increases, as expected, because the same amount of capacitance is loaded with more current for a fixed switching period. The waveform of the peak-to-peak output voltage ripple measured at a worst-case full-load current of 116 mA is shown in Fig. 10. The 3.3 V control signal is shown as a reference signal for the switching period. The output voltage ripple has a double frequency of the control signal frequency, as previously discussed.

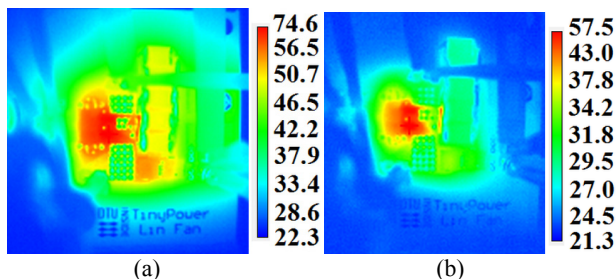


Fig. 8. Thermal images (°C) measured at 380 V input voltage, 21.3 W output power. (a) No airflow, measured after one hour full-power operation. (b) With forced airflow.

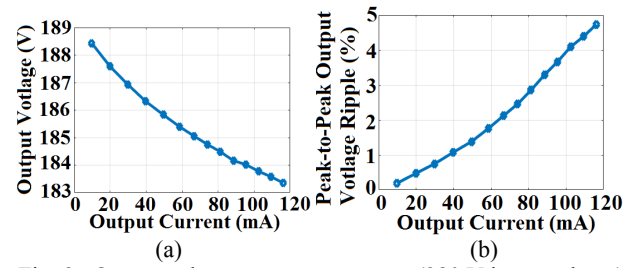


Fig. 9. Output voltage vs. output current (380 V input voltage). (a) DC output voltage. (b) Peak-to-Peak output voltage ripple.

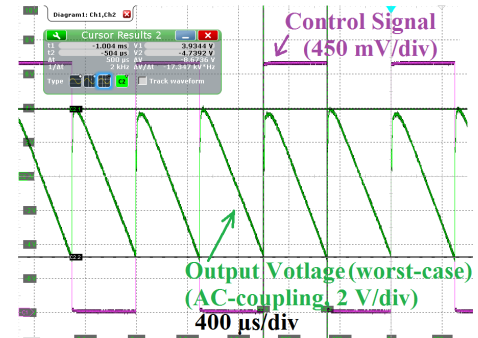


Fig. 10. Waveforms of peak-to-peak output voltage ripple (at a double frequency of the control signal)

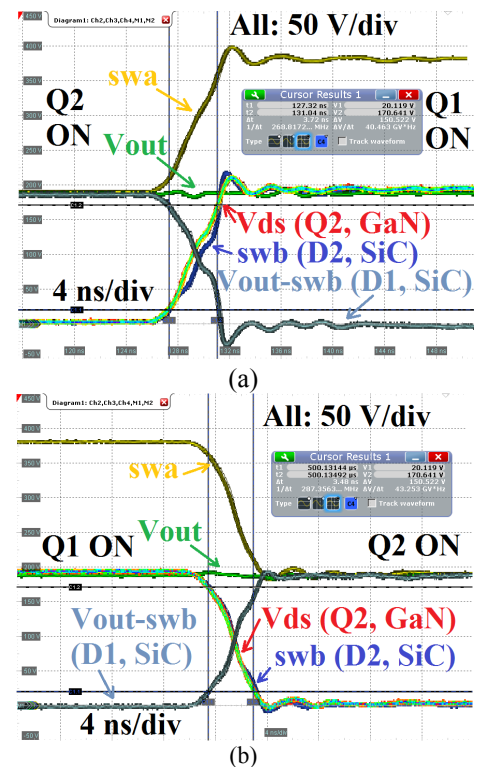


Fig. 11. Measured waveforms of switching transients, with comparisons of GaN device and SiC device. (a) Q1-on/Q2-off transient. (b) Q2-on/Q1-off transient.

Table II. Volumes and power densities of the prototype

	Power Stage	Total Power Converter
Dimension as Cuboid	14.55 mm 21.70 mm 8.50 mm	27.70 mm 21.70 mm 13.00 mm
Boxed Volume	2.68 cm <sup>3</sup>	7.81 cm <sup>3</sup>
Power Density	7.9 W/cm <sup>3</sup> (130 W/inch <sup>3</sup> )	2.7 W/cm <sup>3</sup> (45 W/inch <sup>3</sup> )

The waveforms of the switching nodes (*swa*, *swb*, as shown in Fig. 1) are measured using the probes with the custom-made local ground connections (as shown in Fig. 6). The results are summarized in Fig. 11. The average slew rate of the switching signals is about 40-43 V/ns. The GaN switch (*Q2*) is switching at a similar  $dv/dt$  rate as the SiC diode (*D2*), with slightly faster rise and fall time ( $<0.2$  ns). The GaN device and the SiC device are combined and shown to work well in the proposed power converter.

The attainable power density of the power converter depends on the PCB layout design as well as the circuit topology and the realizing components. The volumes and the power densities of the power stage and the complete power converter of the implemented prototype are summarized in Table II. The power density of the power stage achieves  $7.9 \text{ W/cm}^3$ , and the power density of the complete power convert is  $2.7 \text{ W/cm}^3$ . The boxed volume is used to calculate the power density and it is mainly limited by the height of the energy transfer capacitor *C2* for the power stage and the height of the isolated supply for the complete power converter. The boxed volume of the prototype has further improvement possibilities.

## 6. Conclusion

This paper presents a switched-capacitor DC-DC power converter with an input voltage up to 380 V and an output power experimentally validated up to 21.3 W. The wide band gap semiconductor devices of GaN switches and SiC diodes are combined to compose the proposed power stage for high voltage low power applications. Different isolated driving circuits are analyzed and compared and an isolated half-bridge driving circuit is proposed to achieve high power density. Switching and loss characteristics of the wide band gap semiconductors are analyzed with transient waveforms and thermal images. The full-load efficiency of the complete power converter (including driver and supply) is 97.6%, without heatsink or airflow, and the power densities of the power stage and the complete power converter are  $7.9 \text{ W/cm}^3$  and  $2.7 \text{ W/cm}^3$ , respectively.

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