Voltage Disturbances and Inrush Current of DC Power Supplies

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Abstract. The potential damaging effects of high inrush currents occurring after power quality disturbances on switch-mode dc power supplies (SMPS') have been reported, but have not been studied in detail. This paper presents a new analytical model for the accurate representation and calculation of inrush currents of low-power SMPS devices. This model is verified against previously developed circuit-based simulation model and compared with the only other analytical model available in existing literature. The developed analytical model is also used to investigate device protection co-ordination, in order to demonstrate two important effects of high-inrush current: nuisance tripping of protection and damage of internal SMPS components.

Key words. Inrush current, load modelling, analytical representation, switch-mode dc power supply (SMPS), power quality disturbance, short interruption, voltage sag.

1. Introduction

The potential damaging effects of inrush currents occurring after power quality disturbances (typically voltage sags and short interruptions) on dc power supplies have been reported and investigated in [1, 2]. The same effects were also reported in [3], where several personal computers (PCs) and monitors were permanently damaged when repetitive voltage sags and short interruptions were applied during the testing of equipment sag sensitivity.

While there is a general awareness of high inrush currents due to re-energising of equipment during the voltage recovery following a sag or interruption (commonly known as "hot restart" of equipment), there is no full analytical description and characterisation of this phenomenon, particularly regarding the influence of relevant factors on inrush current and expected range of inrush current values. Accordingly, the analysis presented in this paper provides an analytical model and corresponding relations for the full characterisation and calculation of inrush currents in case of dc power supplies.

This paper is a continuation of the previous work from [4], where accurate circuit-based simulation models of dc power supplies are developed, showing that inrush current may be substantially greater than nominal current. It was also shown in [4] that highest inrush currents will occur when the point-on-wave (POW) of ending of voltage reduction event is close to 90° or 270° of the instantaneous supply voltage, i.e. when supply voltage recovers at the maximum of its sinusoidal waveform.

Section 2 of this paper presents a general background for the analysis of inrush currents in dc power supplies. An analytical model, based on the previously developed full circuit model and equivalent circuit model from [4], is proposed in Section 3, and discussed in more detail in Section 4. The analytical model is then used in Section 5 to determine the influence of some relevant factors (circuit components, system impedance and loading conditions) on the magnitude of inrush current. Finally, the results from the developed analytical model are compared against the only previously published results in Section 6. An example of protection co-ordination is given in Section 7, in order to highlight two possible negative effects of inrush current: nuisance protection tripping and damage of internal SMPS components.

2. Background

A. SMPS

Electronic loads (e.g. TV's, PC's, audio and video equipment, etc.) are responsible for about 25% of the total UK residential power demand [5]. As modern electronic loads are sensitive to voltage variations, they require a regulated dc power supply, commonly referred to as a switch-mode dc power supply (SMPS). A generic SMPS block diagram is shown in Fig. 1.
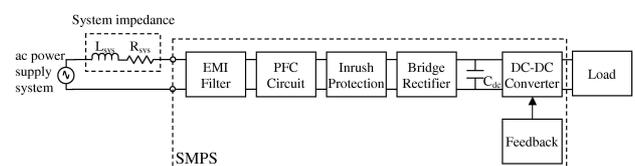
Fig. 1. Generic SMPS block diagram.

The nature of operation of SMPS results in a non-linear current waveform being drawn from the power supply system. This is due to the charging/discharging of the dc link capacitor (C_{dc}), which is used to reduce (i.e. "smooth") the variations of the bridge rectifier dc voltage output. As a consequence, equipment with SMPS will draw high inrush current at the end of voltage reduction event, as the discharged dc link capacitor will recharge upon the voltage recovery. This increased current may cause activation of internal SMPS overcurrent protection, or damage of some of the SMPS circuit components.

Externally, i.e. outside the sealed SMPS casing, the inrush current may cause nuisance tripping of dedicated protection system/component, such as miniature circuit breakers or fuses. The effect of high inrush current on the internal SMPS circuit components is generally more severe, as it may result in permanent damage [1, 2, 3, 4].

Inrush current at the voltage recovery will flow from the ac supply system through all components to the left of C_{dc} in Fig. 1. In the most general case, this includes: diodes, inductors, capacitors, resistors and printed circuit board (PCB) connections and joints. As the flow of high inrush current may result in permanent damage of these components (they usually have low I^2T thermal stress limits, [1]), it is important to consider maximum (i.e. peak) inrush current conditions during the design of SMPS. Typical inrush current protection consists of a negative temperature coefficient (NTC) resistor, which is only able to offer protection when SMPS is initially connected to the supply (i.e. for "cold-start" equipment conditions). The NTC represents a fixed resistance during the steady-state equipment operation (further details can be found in [4]).

B. SMPS Classification

It is possible to divide loads with SMPS' into two general categories, based on their rated active powers and existing harmonic legislation ([6]). Harmonic legislation in [6] stipulates that electronic loads with rated active power less than or equal to 75 W do not need to satisfy any of the prescribed harmonic emission limits. Accordingly, SMPS-based electronic equipment is divided into low-power (≤75 W) and high-power (>75 W) SMPS load.

The general structure (i.e. circuit topology) of low- and high-power SMPS' are similar, except that low-power SMPS' will usually not have the power factor correction (PFC) circuit (Fig. 1), as they do not have to adhere to prescribed harmonic limits. Although this paper focuses on low-power electronic loads (utilising SMPS' with rated powers ≤75 W, such as small television sets, desktop monitors, DVD players, etc.), the presented analysis can be easily extended to high-power SMPS devices.

3. Development of Analytical Model

Previous work in [4] showed that an equivalent model (Fig. 2) was able to accurately describe the inrush current conditions of SMPS-based electronic loads. The general principles of the operation of SMPS circuit form the basis of the analytical model proposed in this paper, and are described below.

When the magnitude of the rectified system voltage (v_{rect}) is greater than the magnitude of capacitor voltage (v_{dc}), capacitor C_{dc} charges, and current is drawn from the supply. Voltage v_{dc} will increase as C_{dc} charges, until it is greater than v_{rect}.

When v_{dc} is greater than v_{rect}, C_{dc} will discharge through the equivalent load, and v_{dc} will decrease, as the energy supplied to the load is taken from the capacitor C_{dc}. During the discharging stage, no current is drawn from the supply. Any inductance/resistance in the system-load conduction path will influence the charge/discharge rate of C_{dc} and the shape of the input current pulses. All inductances and resistances present at the front-end of the SMPS circuit can be grouped in one inductance (L_{SMPS}) and one resistance (R_{SMPS}) in front of the bridge rectifier without any loss of accuracy.
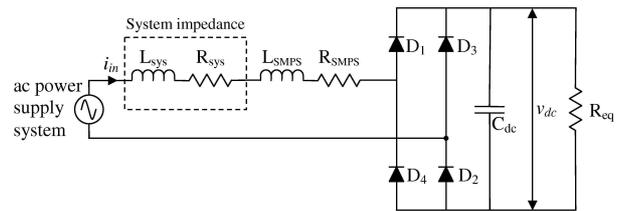
Fig. 2. Equivalent SMPS circuit.

In Fig. 2, L_{sys} and R_{sys} represent the system impedance (Z_{sys}), R_{SMPS} represents the sum of all resistances in the SMPS circuit, L_{SMPS} represents the sum of all inductances in the SMPS circuit and R_{eq} is the equivalent load resistance, defined according to [4] as:

$$R_{eq} = \frac{V_{dc}^2}{P_{rated}} \qquad (1)$$

Using this general circuit description, it is possible to define two general modes of operation of SMPS, determined by the state of charge of C_{dc}. These two modes can be represented by two simple circuits: one for charging state, and one for discharging state. The charging state is represented by an RLC circuit supplied by the rectified system voltage, while the discharging state is represented by an RC discharge circuit, Fig. 3.
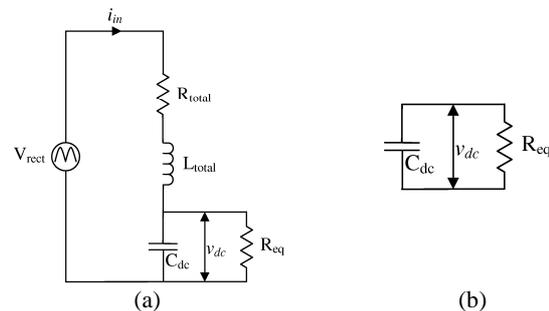
Fig. 3. Equivalent SMPS model:
a) charging state, b) discharging state.

In Fig. 3, R_{total} represents the sum of all resistances in the system-load conduction path ($R_{sys} + R_{SMPS}$); L_{total} represents the sum of all inductances in the system-load conduction path ($L_{sys} + L_{SMPS}$); input voltage (v_{rect}) is rectified system voltage (i.e. positive half-waves after the diode bridge rectifier).

Analytically, the equivalent charge/discharge circuit may be represented by equations (2), (3) and (4).

$$\begin{bmatrix} \dfrac{di_{in}}{dt} \\ \dfrac{dv_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} -\dfrac{R}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C_{dc}} & -\dfrac{1}{C_{dc}.R_{eq}} \end{bmatrix} \begin{bmatrix} i_{in} \\ v_{dc} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} v_{rect} \quad (2)$$

where: R is previously used R_{total} and L is previously used L_{total}

$$i_{in} = 0 \quad (3)$$

$$v_{dc} = v_{start} e^{\dfrac{-t}{R_{eq}C_{dc}}} \quad (4)$$

where: v_{start} is capacitor voltage at the start of discharge period.

After solving differential equations (2), recurrence relations (5) and (6) are obtained for i_{in} and v_{dc} (the device input current and dc link voltage, respectively) during the charging period.

$$i_{in}(n+1) = \frac{1}{\alpha}\left(4C_{dc}i_{in}(n)LR_{eq} + \Delta t^2(-i_{in}(n)(R+R_{eq})+V_s(n)) + 2\Delta t(i_{in}(n)(L-C_{dc}RR_{eq})+C_{dc}R_{eq}(-2V_{dc}(n)+V_s(n+1)+V_s(n)))\right) \quad (5)$$

$$V_{dc}(n+1) = \frac{1}{\alpha}\left(4C_{dc}LR_{eq}V_dc(n) + 2\Delta t(2i_{in}(n)LR_{eq}-LV_{dc}(n)+C_{dc}RR_{eq}V_{dc}(n)) + \Delta t^2(-RV_{dc}(n)+R_{eq}(-V_{dc}(n)+V_s(n+1)+V_s(n)))\right) \quad (6)$$

where: $\alpha = 4C_{dc}LR_{eq}+\Delta t^2(R+R_{eq})+2\Delta t(L+C_{dc}RR_{eq})$, Δt - time step, V_s - instantaneous supply voltage, n and n+1 denote two subsequent calculation steps with values of $i_{in}(n+1)$ and $v_{dc}(n+1)$ calculated from the corresponding (n) step values.

The analytical expressions (5) and (6) can be used instead of the circuit-based simulation model, which will significantly reduce calculation times, without compromising the accuracy of the solution. Furthermore, the proposed analytical model can be easily implemented, exchanged and adapted.

4. Conditions of Peak Inrush Current

During a short supply voltage interruption, the capacitor energy is discharged and supplied to the load, and dc link voltage decreases. If the duration of voltage interruption exceeds the full discharge time of the RC circuit in Fig.3b, the capacitor will fully discharge on the connected equivalent load and the dc link voltage will fall to zero, Fig. 4.

Upon the voltage recovery, the discharged capacitor will start to charge, and current drawn by a capacitor will be proportional to the difference between pre-recovery dc link voltage and supply voltage at the recovery. The maximum inrush current occurs for fully discharged capacitor and recovery at the peak of supply voltage. Figure 4 illustrates that the inrush current and dc link voltage are much greater for recovery at 90°, than for recovery at 0°. The proposed analytical model in Fig. 4 is compared with the equivalent model, which is in [7] fully validated using experimental measurement results.

5. Parameter Variation

To better understand the occurrence of inrush current, two of the most dominant parameters are varied: size of C_{dc} and system impedance. All results are obtained using the analytical model of a typical low-power SMPS with: R=1.31Ω, L=0.73mH, C_{dc}=117µF, P_{rated}=75W (see [4]), POW of initiation of voltage interruption 0° and supply voltage of 50Hz, 230V_{rms} unless stated otherwise.

A. C_{dc}

Fig. 4. Influence of POW of voltage recovery after an interruption on inrush current and dc link voltage: a) POW at 0° b) POW at 90°.
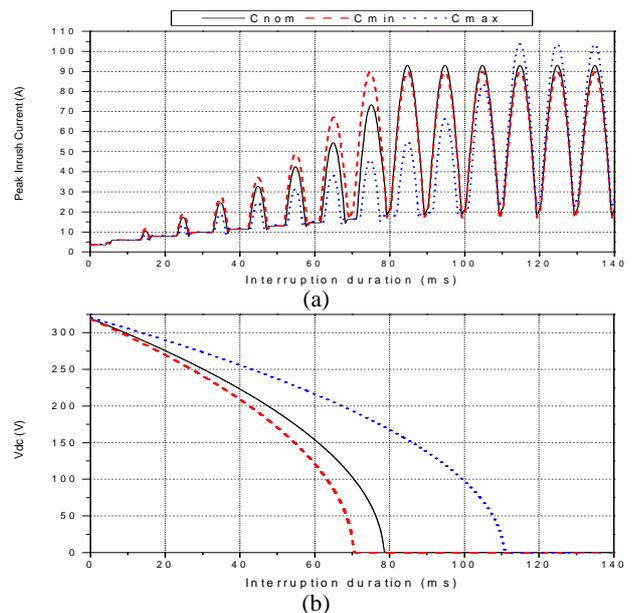
Fig. 5. Influence of size of C_{dc} (nominal 117µF, -10% and +40%) on inrush current for nominal system impedance and full load: a) peak inrush current b) dc link voltage.

The size of C_{dc} will have significant influence on inrush current magnitude. Although it has been shown in [7] that C_{dc} is generally a function of the SMPS' rated power, capacitor manufacturers usually state a -10%/+40% tolerance range for their products. Accordingly, Fig. 5 illustrates that the largest capacitor will have the longest discharge time and will draw the highest inrush current after being fully discharged.

An envelope of peak inrush current within each half-cycle (10ms at 50Hz frequency) is visible in Fig. 5. This envelope is the result of the difference in POW of interruption ending values within the half-cycle. The peak inrush current occurs at 90°/270° POW of interruption ending and the inrush current envelope is constant after C_{dc} is fully discharged.

B. System Impedance

As the value of supply system impedance will vary depending on the connection point of the equipment, it is useful to determine the influence of system impedance on inrush current.

The values of system impedance are added in series to the model as described in Section 3, Fig. 3.

Table I: System impedance values, [8]

Value	System Impedance (Ω)	Rsys (Ω)	Lsys (mH)
Min_Zsys	Z = 0.12+j0.11	0.12	0.35
Nom_Zsys	Z = 0.25+j0.23	0.25	0.73
Max_Zsys	Z= 0.46+j0.45	0.46	1.43

It is evident that system impedance will strongly influence the peak value of inrush current. Lower values of system impedance result in higher values of inrush current, and vice versa. For low power devices, the increased series resistance in case of higher system impedance will significantly reduce the inrush current magnitude (for about 40%-50%).

C. Loading Conditions

The SMPS load is not constant, and it is unlikely that the SMPS will constantly operate at rated power. Figure 7 shows inrush current results for SMPS loaded at half rated power.

Fig. 6. Influence of system impedance and capacitor size on inrush current for full load: a) nominal capacitance b) minimum capacitance c) maximum capacitance.
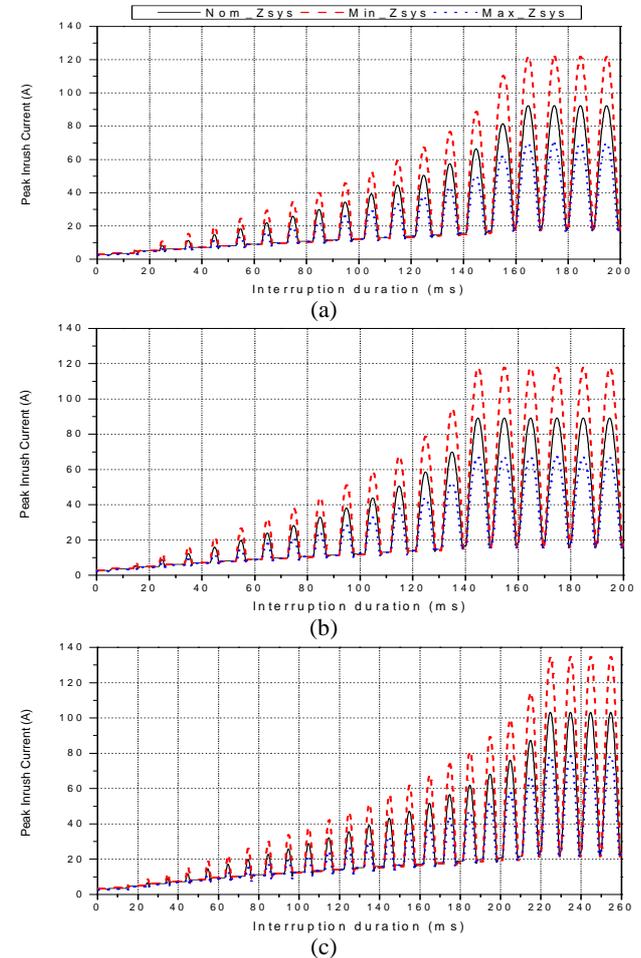
Fig. 7. Influence of system impedance and capacitor size on inrush current for half load: a) nominal capacitance b) minimum capacitance c) maximum capacitance.

The values of typical UK domestic low-voltage system impedance are taken from [8], which specifies typical nominal and maximum values. As no value of minimum system impedance is given, an estimate is made based on the specified values, Table I. The corresponding results for inrush current are shown in Fig. 6.

Comparing Fig. 6 and Fig. 7, it is clear that the SMPS load will influence the peak inrush current. The SMPS will draw the same inrush current when the capacitor is fully discharged, as this is determined by the size of the capacitor and input system/circuit components which remain constant. However, the discharging stage will take twice the time when the SMPS is half loaded, when the equivalent resistance will be doubled.

D. Real SMPS Operation

Modern SMPS' contain sophisticated integrated circuit (IC) control chips, offering a range of features, including: reduced standby power, higher efficiency at reduced load and internal thermal protection.

The control chip is supplied from the dc link voltage and requires a certain minimum dc voltage to function properly. If the dc link voltage is reduced (e.g. due to sag, or short interruption), the controller will act to disconnect the load and maintain some energy in the capacitor after the dc voltage approaches some prescribed minimum value. Therefore, in real SMPS devices, the capacitor may not actually fully discharge, and inrush current may not be as high as predicted by the equivalent circuit.

Figure 8 shows the performance of a typical low-power SMPS with undervoltage control chip. It can be clearly seen in Fig. 8a that nominal load voltage of 24V reduces to zero as load is disconnected in order to preserve minimum dc link voltage. A comparison between inrush current magnitudes of this controlled SMPS with the uncontrolled SMPS is shown in Fig. 8b, together with the results of detailed full circuit model from [4].

Figure 8b shows that the analytical model can accurately match the values of inrush current for controlled SMPS. There is a slight difference for interruption duration between 50-80ms, when discharging rate of capacitor increases and more inrush current is drawn to recharge the capacitor, which is a consequence of the increased complexity of the full circuit model.

(a)

(b)
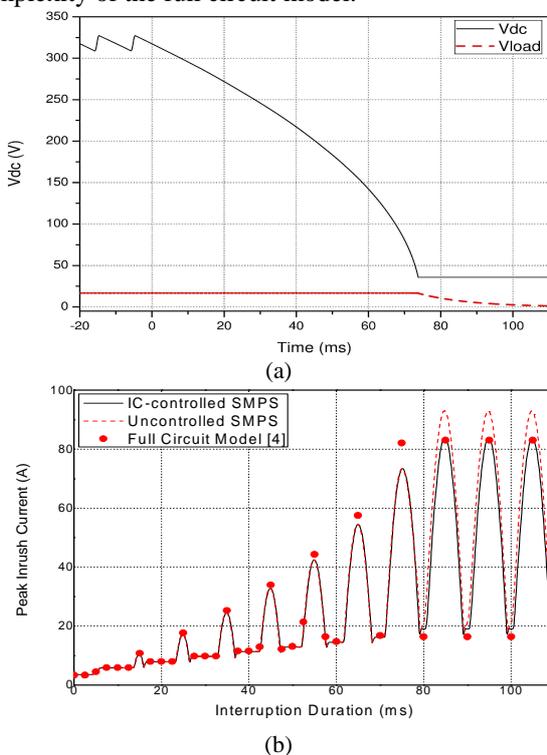
Fig. 8. Inrush current of IC-controlled SMPS (interruption initiation at 0ms): a) full circuit model dc link voltage and load voltage b) inrush current magnitude comparison with uncontrolled SMPS

6. Comparison with Published Results

A simple analytical relation, (7) and (8), for the calculation of peak inrush current is proposed in [1] and further used in [2]. The expressions are given for POW of interruption ending of 90°/270° only, i.e. the worst case. This work also assumed that POW of interruption initiation is 90°. As the pre-disturbance charging state of dc link capacitor is at the maximum for POW of initiation at 90°, this assumption may result in the calculation of lower peak inrush currents for shorter interruptions (i.e. when capacitor is not fully discharged). The worst POW of initiation case is obtained when the capacitor is at the minimum of its normal steady state charge, i.e. just before it would normally start to charge if there is no short voltage interruption/reduction .

$$\Delta V = \frac{I_{load} T_{60}}{2 C_{dc}} \qquad (7)$$

$$I_P = \frac{\left(2N - \frac{1}{2}\right) \Delta V}{\sqrt{\frac{L_S}{C_{dc}}}} \qquad (8)$$

where: I_{load} - load current, T_{60} – period of 60Hz supply system (1/f), N - duration of sag/interruption in cycles, L_s - system inductance; ΔV – half-cycle capacitor voltage decay and I_P – peak inrush current.

The results obtained using (8) are compared with the full circuit simulation results ([4]) and the results from the proposed analytical expression (5) in Fig. 9. The circuit parameters used to verify the expression are taken from [1]: I_{load}=5A, L_s=35µH, C_{dc}=2mF. (*Note:* Although these parameters do not relate to low-power SMPS devices, they are used here to validate (8) from [1] and provide a fair test.)

(a)

(b)
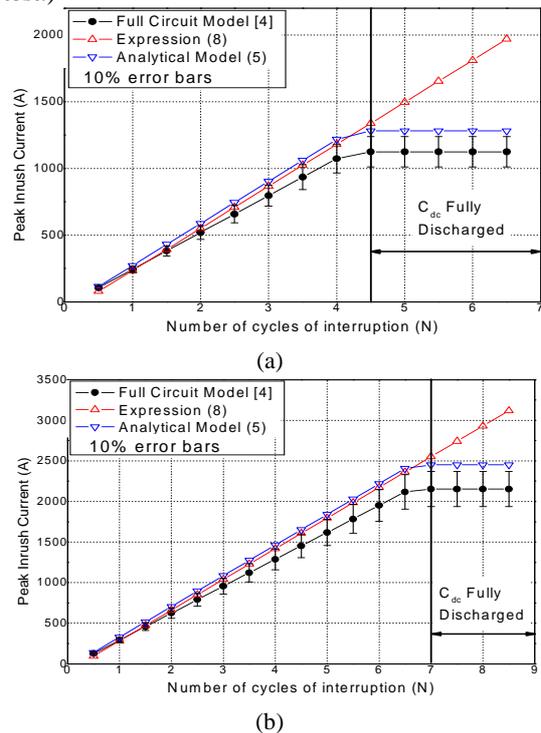
Fig. 9. Comparison of results obtained from [1], [4] and using proposed analytical model (I_{load} = 5A, L_s = 35µH, C_{dc} = 2mF): a) V_{rms}=120V, f=60Hz b) V_{rms}=230V, f=50Hz.

It was found that the expression (8) can match the results for peak inrush current obtained using circuit model [4] and proposed analytical model (5) for both 50Hz and 60Hz supply frequency, assuming that R_{total} is set to zero. As this clearly does not reflect the realistic system-load supply conditions, the corresponding results are

compared again for an actual power supply and SMPS characteristics in Fig. 10.

Expression (8) describes a linear relationship between interruption duration and inrush current, and cannot account for fully discharged capacitor condition, which can be clearly seen in Fig. 9. As mentioned, expression (8) does not account for any resistance in the conduction path, which will influence the shape of input current pulses, essentially reducing the magnitude/value of the inrush current. Therefore, (8) gives overestimated values for inrush currents due to longer sags and interruptions.

For the accurate calculation of inrush current, resistance must be included, as considered SMPS devices will contain a fixed ohmic resistance from the NTC inrush current protection circuit, system impedance and other series resistances present in the conduction path.

The developed analytical model (5) is compared with circuit-based simulation model from [4] and expression (8) for an actual low-power SMPS in Fig. 10, using the circuit parameters stated at the beginning of Section 5.
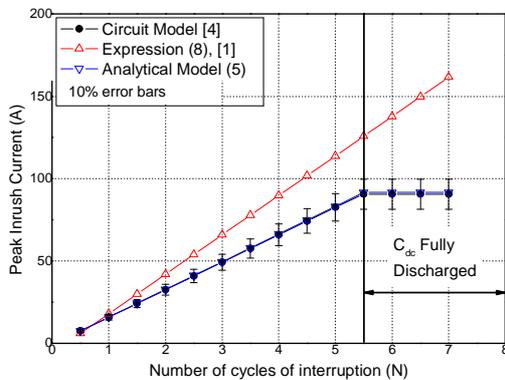
Fig. 10. Comparison of results based on [1], [4] and using proposed analytical model (5), R_{in}=1.31Ω, L_s=0.73mH, C_{dc}=117μF, V_{rms}=230V, f=50Hz.

As expected, the resistance acts to reduce the peak inrush current and expression (8) is now not able to accurately predict the value of peak inrush current. However, very good matching is shown between the proposed analytical model (5) and circuit model from [4]. This is simply a consequence of the correct representation of all relevant components and parameters of modelled SMPS circuit and supply system in both full circuit model from [4] and the proposed analytical model.

7. Protection Co-ordination

The power system is designed to provide protection against excessive currents (e.g. due to short circuit faults). At low-voltage, this is typically achieved by fuse co-ordination. The considered low-voltage supply system and SMPS load is shown in Fig. 11, while the corresponding protection equipment is discussed in the subsequent text.
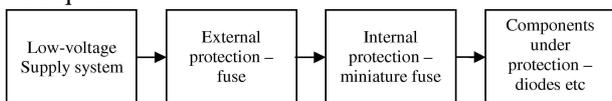
Fig. 11. Protection coordination example.

External Protection
All consumer SMPS devices are connected to the low-voltage network using an insulated cable and fused plug; in the UK, the plug fuses are either 3 A or 13 A.

Internal Protection
SMPS devices are fitted with an internal fuse, called a "miniature fuse", whose purpose is to protect the device from internal faults and overcurrent conditions. Typically, SMPS' use time-delayed miniature fuses.

Internal Components
All electrical components have thermal stress limits and will break/damage with prolonged exposure to excessive currents. In this paper, diodes from the bridge rectifier are selected for the analysis of influence of inrush currents on SMPS' internal components.

A. Melting Integral
The melting integral (MI) is a measure of the thermal energy required to melt a fuse. The MI is defined as the integral of I^2T (9).

$$MI = \int_{t_1}^{t_2} i^2(t)dt \qquad (9)$$

where: MI - melting integral (A^2S), t_1 and t_2 - define the time of the considered current waveform and i(t) - instantaneous current waveform.

The MI can also be calculated for other electrical components, e.g. diodes. Although MI is not explicitly stated for diodes, a peak/maximum sinusoidal current is specified. This can be converted into MI using (10), which is derived from (9) assuming that i(t) is sinusoidal.

$$MI = \frac{I_{peak}^2 T}{2} \qquad (10)$$

where: I_{peak} - peak value of the current waveform and T - period of the current waveform (t_1 and t_2 from (9)).

Figure 12 shows that, as the interruption duration increases (i.e. as the inrush current increases), the value of the MI will also increase.
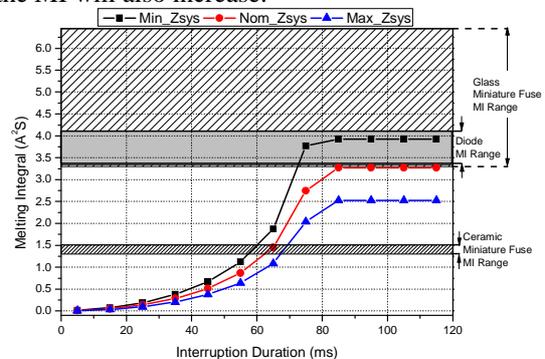
Fig. 12. Melting integral with increasing interruption duration for low-power SMPS for minimum, nominal and maximum Zs_{ys}

Table II offers a comparison between the MI values required to activate external/internal protection (i.e. fuses), the MI values possibly leading to a damage of internal components (i.e. rectifier diodes) and the actual MI values calculated using analytical SMPS model.

The results in Table II highlight that the external fuse will have higher MI value in comparison to MIs of internal fuses and components. In practice, this means that the internal fuse will be activated before the external fuse. Figure 12 indicates the range of MI values that may damage diodes (Table II) in comparison with MI values for low-power SMPS obtained using analytical model (5), suggesting nuisance tripping in case of a ceramic miniature fuse (but successful protection of the diodes), and possible damage of diodes if protected by a glass miniature fuse.

Table II: Protection co-ordination example [9, 10, 11, 12, 13, 14].

Device: SMPS		External Protection: Fuse		Internal Protection: Miniature Fuse			Component: Rectifier Diode	
Rating [W]	MI [A^{2}s]	Rating [A]	MI [A^{2}s]	Rating [A]	Material	MI [A^{2}s]	Rating [A]	MI [A^{2}s]
75	0.008→3.27	3	9.9→14.8	1	Ceramic	1.1→1.28	1	3.37→4.11
		13	124.8→136	1	Glass	3.3→6.45		

Note: The range of SMPS MI represents the increasing MI with voltage interruption duration (Fig. 12), range of external protection MI represents design tolerance and range of miniature fuse and diode component MI represents values from different manufacturers.

8. Conclusions

This paper analyses the occurrence of high inrush currents in modern low-power dc power supplies, and presents an analytical model for the correct representation and characterisation of inrush currents due to voltage sags and short interruptions.

The proposed analytical model is compared with previously developed full circuit model and equivalent circuit model ([4]), both validated in experimental measurements. Afterwards, the proposed analytical model is used to investigate the key influencing factors on the magnitude of inrush current: size of dc link capacitor, loading conditions, point on wave of voltage recovery and system impedance.

A comparison with the only available solution in existing literature highlighted both the improved accuracy and wider applicability of the proposed analytical model. Further work on the simplification of the presented analytical model is expected to increase the computational speed and to provide a basis for the development of the dynamic load models of SMPS devices.

Finally, the analysis of the occurrence of high inrush currents was discussed from an important practical point of view, by comparing the melting integral values of external/internal protection and internal SMPS components with the actual values of melting integrals due to post-disturbance inrush current. It was shown that the melting integral due to post-disturbance high inrush currents in SMPS' may cause either nuisance tripping of internal miniature fuses, or permanent damage of SMPS' circuit components.

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