# History of the amorphous silicon on crystalline silicon heterojunction solar cell

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**Abstract.** Some commercially available solar panels with very high efficiencies for terrestrial photovoltaic applications are based on the amorphous silicon on crystalline silicon material system. This type of heterostructure has a more than 40 years old history. The early development of the technology and the results, obtained in the last years with this type of solar cell are reviewed. In particular it is demonstrated how the physical understanding of the interface properties and band-structure was important for the development of high efficiency solar cells.

## Key words

Amorphous silicon, crystalline silicon, heterojunction, HIT solar cell, history

## 1. History of the a-Si/c-Si solar cell

The investigation of the heterojunction between amorphous silicon and crystalline silicon started more than 40 years ago. The first reported a-Si/c-Si heterojunction has been fabricated by Grigorivici et al. [1] by evaporation of amorphous non-hydrogenated silicon at room temperature on top of n-type or p-type crystalline silicon. The device structure is shown in Fig.1. This deposition method resulted in a highly defective amorphous silicon layer and the study aimed to determine the transport mechanism in the amorphous silicon layer. In Fig.2 it is seen, that a much better rectification has been observed for the a-Si/p-type c-Si heterojunction as compared to the a-Si/n-type c-Si heterojunction. Only a few years later, on a similar structure good rectification has been obtained and - using capacitance-voltage measurements for the electrical characterization - a rather high built-in-voltage of 0.7V has been measured [2]. The authors attributed the improved characteristics to a better interface, obtained by heating under vacuum conditions of the crystalline silicon substrate to 400°C prior of the amorphous silicon deposition. More than 20 years later, in-situ Transient Microwave Conductance (TRMC) measurements during heating and cooling of crystalline

silicon wafers confirmed the importance of the c-Si substrate heating before amorphous silicon deposition, measuring directly the change of the minority carrier lifetime during this heat treatment [3].
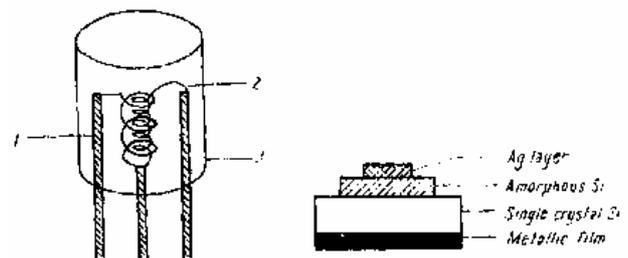


Fig.1    Deposition setup and schematical drawing of the first a-Si/c-Si heterojunction diode in 1968 (from [1]).
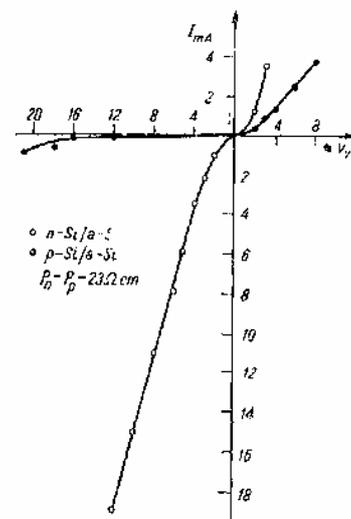


Fig.2    Comparison of the current-voltage characteristics of the first heterojunction diodes (1968), manufactured by amorphous silicon deposition on p-type and n-type c-Si substrates  (from [1]).

In 1974 the first deposition of hydrogenated amorphous silicon on crystalline silicon has been reported by Fuhs et al. [4], resulting in an amorphous silicon top layer with a lower defect density, where electrical transport in the amorphous layer was not anymore dominated by variable-range hopping [5]. It should be noted, that a series of other types of amorphous semiconductor on crystalline silicon heterojunctions have been investigated in these early years, for example with amorphous germanium [1], amorphous oxides [6] and amorphous chalcogenides [6] as top layers. Photovoltaic effects, observed on these devices are already mentioned [7]. A detailed analysis of the current transport mechanisms in an intrinsic amorphous silicon on crystalline silicon heterojunction and a detailed comparison with Schottky diodes is firstly given by Brodsky et al. [8]. The authors already discussed the difference of the barrier heights depending on the substrate doping polarity and found a higher barrier for the a-Si/p-type c-Si junction. In these early years all a-Si/c-Si heterojunctions have been manufactured using intrinsic amorphous silicon either on n-type or on p-type Czochralski grown crystalline substrate. Only in 1975 the possibility of a substitutional doping of amorphous silicon has been demonstrated [8]. In the following years the presently still used multi-tunneling capture-emission model, regarding the electronic transport over at the heterojunction in an i-a-Si:H on p-c-Si with different c-Si resistivities has been developed by Matsuura et al., based on C-V and temperature dependent dark I-V measurements [9]. A picture of the transport mechanisms at the heterointerface is shown in Fig.3.
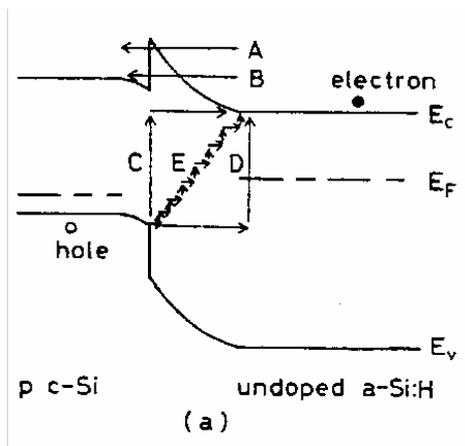


Fig.3    Tunneling model for the a-Si/c-Si heterojunction (from [9]).

Often, like already mentioned in the first publications, the heterojunction has been just used to determine the material parameters of the amorphous silicon top layers, as for example using C-V measurements an intrinsic a-Si:H on n-type crystalline silicon structure by Sasaki et al. [10].
Similar measurements, but in a MOS configuration, have been performed later, where the highly doped c-Si substrate served just as gate electrode and for the growth of a high quality thermal oxide [11]. First industrial applications of the heterojunction focused on the vidicon

operation and in this case, indeed, a top intrinsic amorphous silicon layer is required in order to avoid lateral current transport and hence "blooming" effects [12]. An important parameter of heterojunctions is the relative distribution of the hetero-bandoffset between valence- and conduction-band. While most authors hypothized a mayor contribution of the band-offset in the valence-band [9, 13], also the contrary has been proposed, based on internal photoemission measurements [14]. These authors propose the band-structure of the a-Si/c-Si heterojunction with the mayor contribution of the hetero-bndoffset in the conduction band, as depicted in Fig.4. This controversy has an analogy in the history of the GaAlAs/GaAs heterojunction, where in earlier times the Dingle rule [15] assumed a 85:15% distribution of the hetero-bandoffset between conduction- and valence-band, while later on a 60:40% distribution has been found [16]. This shows, that even in classical III-V semiconductor heterojunctions the interfacial properties are not easy to determine. An excellent discussion of this history is given by Kroemer [17].
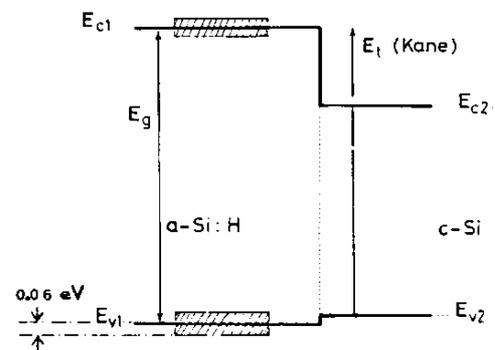


Fig.4    Band diagram of the a-Si/c-Si heterojunction (from [14]).

Some years later, however, a strong interest in photovoltaic applications of the a-Si:H/c-Si heterojunction emerged. Initially, n-type a-Si:H on p-type polycrystalline silicon as low-cost single junction cells [18] or a-Si:H/ribbon c-Si as bottom-cell of a TANDEM solar cell with a top pin-a-Si:H junction [19] have been manufactured. In the case of the TANDEM device, a three terminal configuration has been chosen in order to avoid the top/bottom cell current matching problem and an initial efficiency of 11% has been reported. In this early period all photovoltaic a-Si/c-Si heterojunction devices are n-type amorphous on p-type (poly)crystalline devices. As mentioned before in a very early stage there was already the importance of the interface preparation for this kind of heterojunction taken into account [3].
More emphasis on the interface recombination influence on the device properties has been given in the moment when specific characterization tools have been developed. In particular the application of the contactless (TRMC) technique [20] as in-situ technique first for the characterization of a-Si:H layer growth on glass substrates [21] and then on crystalline silicon substrates [22] enabled the monitoring of the interface recombination during the growth of the amorphous layer. In the case of the monitoring of the heterojunction formation, initially a strong damaging of the crystalline silicon substrate due to

the plasma process, followed by a successive passivation during a-Si:H growth has been observed [22, 23]. This is shown in Fig. 5.
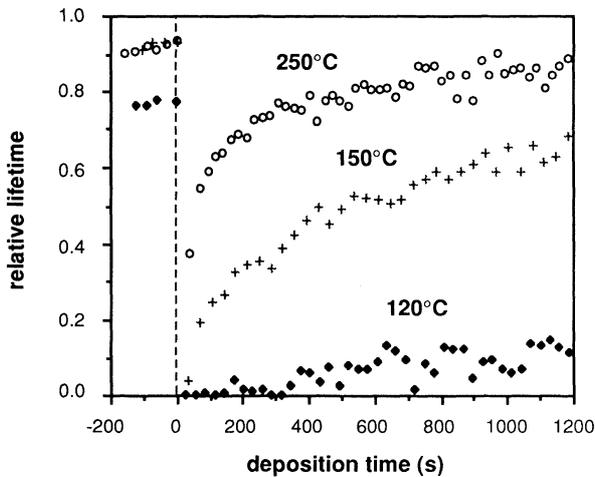


Fig.5 Relative lifetime, as measured by in-situ contactless TRMC measurements during the initial growth of intrinsic amorphous silicon at different temperatures on top of p-type crystalline silicon (from [23]).

The combination of the in-situ TRMC technique with in-situ spectrally resolved ellipsometry enabled at the same time monitoring of the electronical properties and of the structural evolution of the c-Si surface during plasma processing [24].



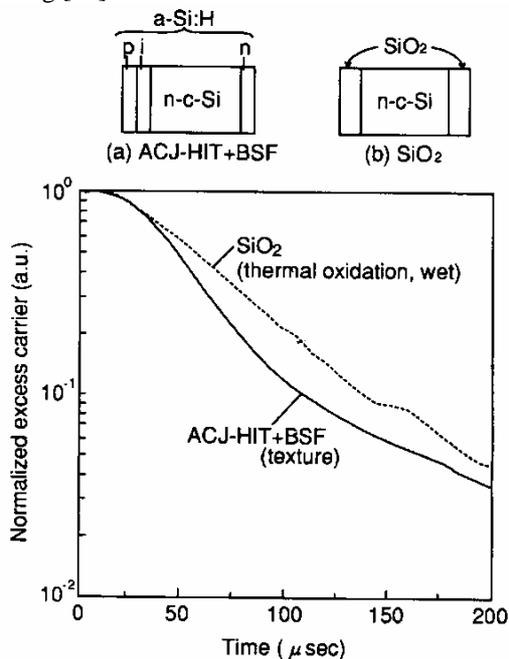Fig.6 Comparison of the passivation efficiency of amorphous silicon, as compared to SiO₂ (from [27]).

Another result of the in-situ TRMC-measurements is the direct observation of the charge carrier injection from the amorphous layer into the crystalline silicon substrate. In particular the dependence of the injection efficiency on the a-Si:H bulk layer and interface properties has been investigated [25] and correlated with the electrical characteristics of the finished heterojunction device [26]. Due to the knowledge, that amorphous silicon layers are as efficient as $SiO_2$ layers for the surface passivation of crystalline silicon substrates, as determined again by the TRMC technique [27] (see Fig.6), in 1992 a new type of a-Si/c-Si heterojunction solar cell has been presented by SANYO – namely the HIT solar cell – having a p-type amorphous on n-type crystalline silicon structure with additionally a thin intrinsic amorphous silicon interface layer and an n-type amorphous silicon back passivation layer [28]. Already the first publications reported a 18.7% conversion efficiency for small area HIT solar cells [27]. The structure and the current-voltage characteristics of a small area cell under AM1.5 illumination conditions are shown in Fig. 7. For large area (100cm²) HIT solar cells in 1992 already an efficiency of 13.6% has been reported [27].
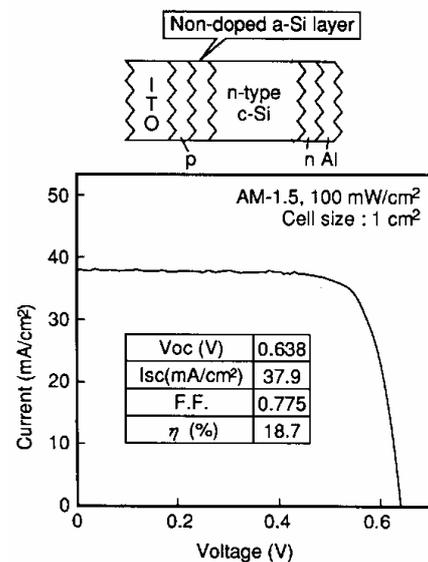


Fig.7 Device structure and current-voltage charac-teristics under AM1.5 illumination of an early (1992) small area HIT solar cell (from [27]).
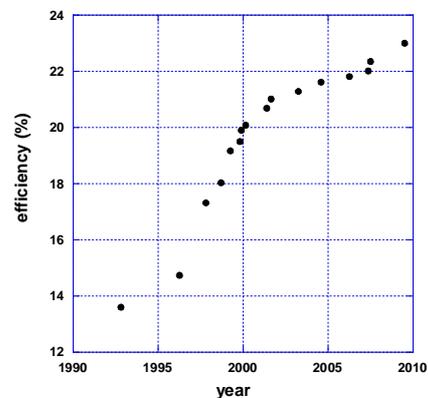


Fig.8 Development of the large area HIT solar cell efficiencies (R&D) during the last years (data from [27,29,30]).

In the following years a continuous progress has been seen regarding the conversion efficiency of the HIT solar cell and nowadays 23.0% have been achieved for a large area (100cm$^2$) HIT solar cell [29] (Fig.8).

The authors apologize for the bad quality of some historical figures, which were not available in better conditions.

## References

1 R.Grigorovici, R.Croitoru, N.Marina and I.Natasi, Rev. Roumaine Phys., vol.13 (1968), 317
2 T.S. Jayadevalah and O. Busmundrud, El. Lett., vol.8 (1972), 75
3 H.C. Neitzert and W.Hirsch, Phys. Stat. Sol. (a), vol.151 (1995), 371
4 W. Fuhs, K. Niemann and J. Stuke, Proc. Internat. Conf. Tedrahedrally Bonded Amorphous Semiconductors, Yorktown (1974), p.345
5 N.F. Mott, J. Non-Cryst. Solids, 1 (1968), 1
6 B.Dunn, J.D.Mackenzie, J.K.Clifton and J.V. Masi, Appl.Phys.Lett., vol.26 (1975), 85
7 M.H. Brodsky, G.H.Doehler and P.J.Steinhardt, Phys.Stat.Sol. (b), vol.72 (1975), 761
8 W. E. Spear and P. G. Le Comber Solid State Communication, vol.17 (1975), 1193
9 H.Matsuura, T.Okuno, H.Okushi and K.Tanaka, J.Appl.Phys., vol.55 (1984), 1012
10 G.Sasaki, S.Fujita and A.Sasaki, J.Appl.Phys., vol.53 (1982), 1013
11 E. Klausmann. W.R.Fahrner, S. Loeffler and H.C.Neitzert, J. of the Electrochemical Soc., vol.140 (1993), 2323
12 H.Mimura and Y.Hatanaka, J.Appl. Phys., vol.61 (1987), 2575
13 F.A.Rubinelli, Solid-State Electronics, vol.30 (1987), 345
14 M.Cuniot and Y.Marfaing, Phil. Mag. B, vol.57 (1988), 291
15 R. Dingle, Crit. Rev. Solid State Sci., vol.5 (1975), 555
16 R.C.Miller, D.A.Kleistman and A.C.Gossard, Phys.Rev.B., vol.29 (1984, 3740
17 H. Kroemer, J.Vac.Sci.Technol. B, vol.11 (1993), 1354
18 K. Okuda, H. Okamoto and Y. Hamakawa, Jpn. J. Appl. Phys., vol.22 (1983), L605
19 H.Nozagi, T.Hatayama, H.Ito, K.Ide and M.Nakagawa, Technical Digest of the PVCEC-1, Kobe (1984), pp.167-170
20 Kunst and Beck, J. Appl.Phys., 63 (1988), 1093
21 M.Kunst and A.Werner, Solid State Comm., vol.54 (1985), 119
22 H.C.Neitzert and M.Kunst, W.Hirsch, C.Swiatkowski and M. Kunst, Technical Digest of the PVCEC-5, Kyoto (1990), pp.825-827
23 H.C.Neitzert and M.Kunst, Phys. Rev. B, vol.47 (1993), 4080
24 H.C.Neitzert, N.Layadi, P.Roca I Cabarrocas, R. Vanderhaghen and M.Kunst, Material Science Forum, vol.173-174 (1995), 209
25 H.C.Neitzert and M.Kunst, Phys. Rev. B, vol.48 (1993), 4481
26 H.C. Neitzert, SPIE Proceedings, vol. 1985 (1993), 530
27 T.Takahama, M.Taguchi, S.Kuroda, T.Matsuyama, M.Tanaka, S.Tsuda, S.Nakano and Y.Kuwano, Proc. of the 11th European Photovoltaic Solar Energy Conference, Montreux (1992), pp.1057-1060
28 M.Tanaka, M.Taguchi, T.Matsuyama, T.Sawada, S.Tsuda, S.Nakano, H.Hanafusa and Y.Kuwano, Jpn.J.Appl.Phys., vol.31 (1992), 3518
29 H. Kanno, D. Ide, Y. Tsunomura, S. Taira, T. Baba, Y. Yoshimine, M. Taguchi, T. Kinishita, H. Sakata, E. Maruyama, Proc. of the 123rd European Photovoltaic Solar Energy Conference, Valencia (2008), pp.1136-1139
30 SANYO Corp., May 2009, unpublished results