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Modeling, Control and Simulation of a High-Current DC-DC Converter for Fuel Cell Applications

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Abstract. In this paper, a high-current two-stage DC-DC converter fed by a Proton Exchange Membrane Fuel Cell (PEMFC) is studied. The converter consists of two three-phase full-bridge inverters connected through three AC coupled inductors. The mathematical models of both converter and PEMFC are first presented, and a control scheme that ensures a high power factor at the AC stage and a regulated voltage at the DC load is then implemented. The performance of the proposed control system is verified through digital simulations.

Key words

DC-DC converter, three-phase inverters, six-switch rectifiers, fuel cells, high currents, modeling, control.

1. Introduction

During the last two decades, several DC-DC topologies that cover a wide power range have been proposed. Most of them, based on the use of MOSFETs, were dedicated to low power applications, and are generally provided with a high frequency transformer that ensures galvanic isolation at the mid-stage. In addition, the input stage of such converters is limited to a two-leg inverter, whereas the output stage consists only of rectifying diodes, yielding thus a unidirectional power flow.

In high current applications, the use of two-leg topologies becomes insufficient, and the extension to the abovementioned converters to the three-phase case becomes mandatory due to the limited ratings of the available semiconductors [1]. Furthermore, in order to decrease the current ratings in such converters without affecting the power level, a high power factor is required at the AC mid-stage. This feature makes necessary the replacement of the conventional diode bridge output stage by a fully controlled six-switch rectifier. This topological modification will have other advantages: 1) the power flow becomes now bi-directional, 2) the regulation of the DC voltage at the rectifier output becomes possible, 3) the power losses in the cupper and the magnetic core are reduced, which is due essentially to the reduction of the RMS-currents and the elimination of low-frequency current harmonics, 4) the power efficiency is consequently increased, 5) the size, weight and cost of the magnetic core are reduced, and 6) the EMI disturbances become negligible.

The DC-DC topology considered in this paper is described in Fig. 1. It is used to connect a Proton Exchange Membrane Fuel Cell (PEMFC) to a DC load at different voltage level. The converter consists of two sixswitch inverters connected through three AC inductors coupled on a same magnetic core. The bulkiness of the magnetic core could be easily and significantly reduced by increasing the fundamental frequency at the AC stage.

In this paper, mathematical models for the PEMFC source and DC-DC converter are presented, upon which a control scheme has been designed. Both six-switch bridges are controlled using the fixed-frequency carrier-based Pulse-Width-Modulation technique [2]. An open-loop control is applied to the inverter, whereas closed-loops current and voltage regulators are designed to control the rectifier on the basis of the state-space averaged model of the two-stage converter [3]. The proposed control system is tested through simulations for a resistive load, and the results have shown good performance regarding load voltage regulation and high power quality at the AC intermediate stage.



Fig. 1. Two-stage DC-DC converter for PEMFC

2. Modeling of the Power Stage

A. PEMFC Model

Based on the work presented in [4], a PEMFC stack can be modeled as illustrated in Fig. 2. The stack output voltage v_{fc} is expressed in terms of the cell current i_{fc} and the stack parameters as follows:

$$v_{fc} = E - R_{fc} i_{if} = E_{oc} - NA \ln\left(\frac{i_{fc}}{i_0}\right) \cdot \frac{1}{T_d s + 1} - R_{fc} i_{fc} \quad (1)$$

$$E_{oc} = NE_n \tag{2}$$

where R_{fc} denotes the stack resistance, E_{oc} the open circuit voltage, N the number of cells in series, E_n the Nernst voltage, A the Tafel slope, i_0 the exchange current and T_d the fuel cell response time.



Fig. 2. PEMFC stack model.

B. Sate-Space Average Model of the DC-DC Converter

According to [3], the state-space average model of the two-stage DC-DC converter is given as:

$$L\frac{di_d}{dt} = -Ri_d + L\omega i_q + d_d v_{fc} - d'_d v_0$$
(3)

$$L\frac{di_q}{dt} = -Ri_q - L\omega i_d + d_q v_{fc} - d'_q v_0$$
(4)

$$C_0 \frac{dv_0}{dt} = \frac{3}{2} \left(d'_d i_d + d'_q i_q \right) - \frac{v_0}{R_0}$$
(5)

where i_d and i_q represent respectively the *d*-axis and *q*-axis components of currents i_A , i_B and i_C in the synchronous frame, v_0 is the DC-load voltage, d_d and d_q are respectively the *d*-axis and *q*-axis components of the duty cycles corresponding to the inverter upper switches, expressed in the synchronous frame, d'_d and d'_q are respectively the *d*-axis and *q*-axis components of the duty cycles the synchronous frame, d'_d and d'_q are respectively the *d*-axis and *q*-axis components of the duty cycles the synchronous frame, d'_d and d'_q are respectively the *d*-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles the d-axis and *q*-axis components of the duty cycles cycles the d-axis and *q*-axis components of the duty cycles cycles the d-axis and *q*-axis cycles cycles the d-axis and *q*-axis cycles cycl

cycles corresponding to the rectifier upper switches, expressed in the synchronous frame, R_0 and R represent respectively the DC load and power losses in each AC-side inductor, and ω is the angular frequency at the intermediate AC stage.

3. Control System

A. Inverter Control

The three system outputs are all controllable by operating only the output stage rectifier. In this case, the inverter control becomes quite simple, and would consist only of an open loop gate signals generation using the conventional sine-triangle pulse-width-modulation technique. Hence, by denoting u_A , u_B and u_C the inverter reference signals defined as:

$$u_{A}(t) = \hat{u} \cdot \sin(\omega t)$$

$$u_{B}(t) = \hat{u} \cdot \sin(\omega t - 2\pi/3)$$

$$u_{C}(t) = \hat{u} \cdot \sin(\omega t - 4\pi/3)$$
(6)

which would be compared to a common high-frequency triangular carrier with a peak value \hat{v}_{tri} , the expressions of the duty cycles that correspond to the inverter upper switches become in the stationary frame:

$$d_{A}(t) = \frac{1}{2} + \frac{r}{2}\sin(\omega t)$$

$$d_{B}(t) = \frac{1}{2} + \frac{r}{2}\sin(\omega t - 2\pi/3)$$

$$d_{C}(t) = \frac{1}{2} + \frac{r}{2}\sin(\omega t - 4\pi/3)$$
(7)

and in the rotating frame:

$$d_{d} = \frac{r}{2}$$

$$d_{q} = 0$$

$$d_{0} = \frac{3}{2}$$
(8)

where $r = \hat{u}/\hat{v}_{tri}$ denotes the voltage regulation parameter, and d_0 the zero-sequence component of inverter upper switches duty cycles.

Furthermore, in order to minimize the current constraints at rated power consumption, the parameter r is set to its maximum value $r_{\text{max}} = 1$.

B. Rectifier Control

A multiple-loops linear control system is designed for the rectifier using the averaged model in the rotating frame given in section 2.*B*. The control scheme is presented in Fig. 3. **K** represents the stationary/synchronous frame transformation. The current references i_d^* and i_q^* are generated as follows [3]:



Fig. 3. Rectifier control scheme.

$$i_{d}^{*} = \frac{\hat{i}^{*}}{\sqrt{v_{d,0}^{2} + v_{q,0}^{2}}} v_{d,0}$$

$$i_{q}^{*} = \frac{\hat{i}^{*}}{\sqrt{v_{d,0}^{2} + v_{q,0}^{2}}} v_{q,0}$$
(9)

where \hat{i}^* denotes the peak value of the reference currents, $v_{d,0}$ and $v_{q,0}$ are respectively the DC-components of $d_d \cdot v_{fc}$ and $d_q \cdot v_{fc}$. Note that these components represent also the fundamental voltage at the inverter output.

 K_i and K_v are respectively the current and voltage loops feedback-scaling gains. The Proportional-Integral (PI) type inner regulators $H_{i,d}(s)$, $H_{i,q}(s)$ and outer regulator $H_v(s)$ are designed independently by using the successive feedback looping approach described in [5]. That means that all the cross-coupling between the control inputs and the system outputs was not considered. The control outputs u'_A , u'_B and u'_C are compared to the highfrequency triangular carrier in order to generate the rectifier gate signals.

On the other hand, the outer loop is designed to be slower enough than the inner ones in order to ensure high stability to the control system.

4. Simulation Results

The system in Fig. 1 and its control circuit in Fig. 3 are implemented numerically using Matlab/Simulink. A 6kW-45V PEMFC stack from NedStack (NedStack PS6) has been chosen as the source of energy. The corresponding current-voltage and current-power curves are given in Fig. 4 [6]. The DC-DC converter has been implemented according to its switching-functions-based model developed in [7]. The numerical values of the system parameters and operating set point are given in

the appendix. The mid-stage fundamental frequency is intentionally chosen relatively high in order to reduce the value of the three-phase inductors and the size of the magnetic core. The power losses in the inductors are neglected ($R \approx 0$).

The simulation results showing the system performance in the steady-state are presented in Fig. 5. The system operates with a regulated voltage at the DC output stage and a nearly unity power factor at the AC mid-stage. The Total Harmonic Distortion of the mid-stage currents is less than 1%. Fig. 6 shows the system's response to load step changes in the under-load range, whereas Fig. 7 presents the system's response to load step changes in the over-load region. In all cases, the load steps are applied at t = 1 s, and the obtained system response time is near 4 s.



Fig. 4. I-V and I-P curves of a NedStack PS6 PEMFC.

5. Conclusion

In this paper, a two-stage high-current DC-DC converter for fuel cell applications has been studied. Mathematical models for the PEMFC source and the power conversion stage has been presented, and a multiple-loop control scheme that ensures a high power factor at the AC stage and a regulated voltage at the DC load has been designed. The steady-state and dynamic performance of the proposed control system was verified through numerical simulations. It was shown that the converter exhibits high operation quality in term of mid-stage current distortion and power factor.

Appendix

A. PEMFC Parameters

Open circuit voltage	$E_{oc} = 65 \text{ V}$
Number of cells in series	<i>N</i> = 65
Nernst voltage	$E_n = 1 \text{ V}$
Tafel slope	A = 30.7 mV
Exchange current	$i_0 = 0.94 \text{ A}$
Fuel cell response time	$T_d = 10 \text{ s}$
Stack resistance	$R_{fc} = 75.8 \text{ m}\Omega$

B. DC-DC Converter and Control System Parameters

Desired DC load voltage v_0^* Nominal load powerP =Fundamental frequencyf =Switching frequency $f_s =$ AC-side inductorsL =DC-side capacitor C_0 Feedback scaling gains $K_i =$ Inner regulators $H_{i,d}$

Outer regulator

ge
$$v_0 = 150 \text{ V}$$

 $P = 6 \text{ kW}$
 $y \quad f = \omega/2\pi = 200 \text{ Hz}$
 $f_s = 20 \text{ kHz}$
 $L = 100 \mu\text{H}, \text{ each}$
 $C_0 = 1 \text{ mF}$
 $K_i = K_v = 1$
 $H_{i,d}(s) = H_{i,q}(s) = -\frac{s+45}{s}$
 $H_v(s) = 3\frac{s+1}{s}$



Fig. 5. Steady-state waveforms of (a) the DC load voltage and the PEMFC stack output voltage, (b) the AC mid-stage currents, (c) the cell current and (d) the voltage across the inductor in phase A.



Fig. 6. Impacts of a load step decrease (from 6kW to 3kW) and increase (from 3kW to 6kW) on the DC load voltage and the PEMFC stack output voltage (Figs. 6.a and 6.c respectively), and on the AC mid-stage currents (Figs. 6.b and 6.d respectively).

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Fig. 7. Impacts of a load step increase (from 6kW to 12kW) and decrease (from 12kW to 6kW) on the DC load voltage and the PEMFC stack output voltage (Figs. 7.a and 7.c respectively), and on the AC mid-stage currents (Figs. 7.b and 7.d respectively).