# FPGA Implementation of a Multiphase Space Vector Modulation for Asymmetrical Dual Three–phase AC Machines

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**Abstract.** Current control in conventional motor drives is normally based on controllers with sub harmonic voltage modulation techniques. Space vector modulation (SVM) for three–leg VSI and conventional motor drives has recently become a standard current control technique due to its benefits. That's why modern microcontrollers and DSPs offer internal peripheral to implement SVM technique for conventional drives. Multiphase (more than three phases) drives possess interesting advantages over conventional three–phase drives. Over the last years, topics related to the extension of control schemes to these specific drives have been covered in depth in literature. However, implementation of SVM for multiphase drives is rare due to its complexity and the specific control peripherals absence. This paper presents the FPGA implementation of a SVM strategy for a very interesting and discussed multiphase drive: the asymmetrical dual three–phase AC machine.

**Keywords**

Multiphase systems, current control techniques, Space Vector Modulation.

## 1.  Introduction

Multiphase electrical drives have been recently proposed for applications where some specific advantages can be better exploited. The most important ones are: lower torque pulsations, less DC link current harmonics, higher overall system reliability and better power distribution per phase [1]. Among multiphase drives, a very interesting and discussed in the literature multiphase solution is the dual three–phase induction machine having two sets of three–phase windings spatially shifted by 30 electrical degrees with isolated neutral points (also called asymmetrical dual three–phase ac machine). The asymmetrical dual three–phase ac machine has been used in specific applications since the late 1920s [2]. For instance, in applications like electrical vehicles, the low available DC–link voltage imposes high phase currents

for a three–phase drive. In this case, the dual three–phase induction machine is an interesting alternative to the conventional three–phase counterpart [3].

Current control in conventional motor drives is usually based on controllers with sub harmonic voltage modulation (PWM or Space Vector) techniques [4]. Space vector PWM technique for the dual three–phase induction machine has been recently studied [5]–[6]. However, practical implementation in the above literature using embedded systems is very harsh, complex, and expensive. For instance, a dSpace evaluation board is used in [5], with a Power PC processor to implement the current control algorithm and a Texas Instruments DSP TMS320F240 as a PWM control peripheral. These initial developments motivate us to implement the multiphase SVM strategy in a FPGA–based peripheral.

In this paper, a new hardware implementation based on a FPGA is proposed to solve the problem. The paper is organized as follows. First, the general principles of the SVM method for an asymmetrical dual three–phase AC machine are shown in section 2. Then, section 3 details the implementation of the multiphase SVM in a FPGA. Section 4 presents the results obtained using the FPGA as a SVM peripheral. Finally, the conclusions are given in the last section.

## 2.  SVM in the dual 3–phase AC machine

The asymmetrical dual three–phase ac machine is a hex–phase induction machine having two sets of three–phase windings spatially shifted by 30 electrical degrees with isolated neutral points. A detailed scheme of the drive is provided in Fig. 1.

The analytical description of this machine follows two different paths: the double d–q winding approach and the vector space decomposition (VSD) approach. According to the first one [7], the machine can be represented with two pairs of d–q–o windings corresponding to the two three–phase stator windings. From this point of view, the analytical model of the asymmetrical dual three–phase induction machine is an extension of the conventional three–phase induction machine model. The d–q–o reference frame transformation decomposes the original three–dimensional vector space into direct sum of a d–q subspace and a zero sequence subspace which is orthogonal to d–q, decoupling the components that produce rotating m.m.f. and the components of zero sequence.



$$\begin{bmatrix} u_{\alpha s} \\ u_{\beta s} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_s & 0 & 0 & 0 \\ 0 & R_s & 0 & 0 \\ 0 & \omega_r \cdot L_m & R_r & \omega_r \cdot L_r \\ -\omega_r \cdot L_m & 0 & -\omega_r \cdot L_r & R_r \end{bmatrix} \cdot \begin{bmatrix} i_{\alpha s} \\ i_{\beta s} \\ i_{\alpha r} \\ i_{\beta r} \end{bmatrix}$$

$$+ \begin{bmatrix} L_s & 0 & L_m & 0 \\ 0 & L_s & 0 & L_m \\ L_m & 0 & L_r & 0 \\ 0 & L_m & 0 & L_r \end{bmatrix} \cdot p \cdot \begin{bmatrix} i_{\alpha s} \\ i_{\beta s} \\ i_{\alpha r} \\ i_{\beta r} \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} u_{xs} \\ u_{ys} \end{bmatrix} = \begin{bmatrix} R_s & 0 \\ 0 & R_s \end{bmatrix} \cdot \begin{bmatrix} i_{xs} \\ i_{ys} \end{bmatrix} + \begin{bmatrix} L_{ls} & 0 \\ 0 & L_{ls} \end{bmatrix} \cdot p \cdot \begin{bmatrix} i_{xs} \\ i_{ys} \end{bmatrix} \tag{2}$$

where $p$ is the time derivative operator, $\omega_r$ the rotor angular speed, and $R_s$, $L_s = L_{ls} + L_m$, $R_r$, $L_r = L_{lr} + L_m$ and $L_m$ the electrical parameters of the machine.

The Voltage Source Inverter (VSI) is characterized with $2^6 = 64$ vectors (60 active and 4 zero) which are mapped in the α–β and x–y subspaces. Figure 2 shows the active vectors in the α–β and x–y subspaces, where each vector switching state is identified using the switching function by two octal numbers corresponding to the binary numbers $[S_a S_b S_c]$ and $[S_d S_e S_f]$, respectively. In fact, as shown on Fig. 2, the redundancy of the switching states results in only 49 different vectors (48 active and 1 zero). Anyway, the complexity of the required algorithm for the implementation of the SVM current control method increases a lot in six–phase electrical drives compared with conventional three–phase machines.

Fig. 1. A general scheme of an asymmetrical dual three–phase AC drive.

According to the VSD approach [8], the machine can be represented with three stator–rotor pairs of windings in orthogonal subspaces. One stator–rotor pair engages with electromechanical energy conversion (α–β subspace in what follows), while the others do not. The first stator–rotor pair represents the fundamental supply component plus supply harmonic of the order 12n±1 (n=1,2,3,…). The other stator–rotor pairs represent supply harmonic of the order 6n±1 (x–y subspace with n=1,3,5,…) plus the zero sequence harmonic components which disappear if isolated neutral points are assumed.

The VSD approach under standard assumptions (negligible space harmonic and magnetic saturation) explains the presence of low–order current harmonics in the machine current spectrum, in contrast to the double d–q winding approach. Using this approach, the original six–dimensional space of the machine is decomposed into two orthogonal subspaces, α–β and x–y, and a practical model suitable for control is obtained as follows in the stationary reference frame, considering a normal squirrel cage induction motor:



Fig. 2. Voltage vectors applied in the α–β and x–y subspaces using a 6–phase VSI. Notice that the same VSI switching state produces different voltage vector in α–β and x–y subspaces.

The goal of the SVM control technique is to synthesize the (α, β) voltage vectors in a sampling period to satisfy the machine's torque control requirements and, at the same time, to maintain near zero the average voltage on the other subspaces because they do not contribute to the electromechanical energy conversion. Consequently, the following equation must be accomplished:

$$\begin{bmatrix} tV1 \\ tV2 \\ tV3 \\ tV4 \\ tV0 \end{bmatrix} = \begin{bmatrix} v_\alpha^1 & v_\alpha^2 & v_\alpha^3 & v_\alpha^4 & v_\alpha^0 \\ v_\beta^1 & v_\beta^2 & v_\beta^3 & v_\beta^4 & v_\beta^0 \\ v_x^1 & v_x^2 & v_x^3 & v_x^4 & v_x^0 \\ v_y^1 & v_y^2 & v_y^3 & v_y^4 & v_y^0 \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix}^{-1} \cdot \begin{bmatrix} v_\alpha^* \\ v_\beta^* \\ 0 \\ 0 \\ 1 \end{bmatrix} \cdot T_s \tag{3}$$

where $v_m^k$ is the projection of the $k_{th}$ voltage vector on the m-axis, and $tVk$ is the dwell time of that vector during time interval $T_s$. The quantities $v_\alpha^*$, $v_\beta^*$ represent the reference voltage in the α–β subspace.

During each sampling period $T_s$ and depending on location of reference vector (Fig. 3), a set of five voltage vectors must be chosen to reach the reference voltage and to guarantee that each $tVk$ has a positive and unique solution. The implemented space vector PWM strategy is similar to the one proposed in [8], where the number of considered voltage vectors is reduced to the outermost active voltage vector in the α–β subspace plus the null voltage vectors. Four adjacent active voltage vectors are chosen according to the reference voltage vector position. The fifth voltage vector, the null one, is selected from the zero vectors set. This assumption is commonly used in current control of the asymmetrical dual three–phase ac machine assuming sinusoidal output voltage [5], [6], [8], [9]. For instance, if only the 12 outer vectors (the largest ones) are considered, the SVM can be implemented using only 16 possible stator voltage vectors (12 active and 4 zero vectors). The SVM technique considering 16 switching vectors is simpler, requires less computing time, guarantees a unique and feasible solution, and favors the real–time implementation of the control algorithm. Notice that these 12 active vectors are the largest ones in the α–β subspace, producing the highest torque reference, but the lowest one in the x–y subspace, favoring the minimum voltage supply of the 6n±1 (with n=1,3,5,…) harmonic.
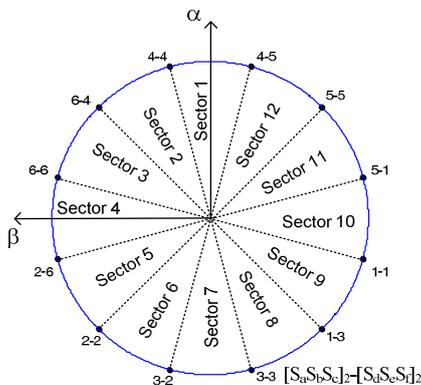


Fig. 3. Sectors in the α–β subspace.

An exhaustive study for the real time implementation of the SVM control technique for the dual asymmetrical three–phase induction machine, using the aforementioned methodology, can be found in [5]. It concludes that six different times must be calculated for each sampling period:

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} = \frac{T_s}{V_{DC}} \begin{bmatrix} -(\sqrt{3}-2) & -1 \\ (\sqrt{3}-1) & -(\sqrt{3}-1) \\ 1 & (\sqrt{3}-2) \\ 1 & -(\sqrt{3}-2) \\ (\sqrt{3}-1) & (\sqrt{3}-1) \\ -(\sqrt{3}-2) & 1 \end{bmatrix} \cdot \begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} \quad (4)$$

Then, the dwell times of the active voltage vectors $tVi, i \in \{1,2,3,4,5\}$, are found according to Table I, while the zero voltage vector is applied during the dwell time $tV0$, evaluated from the following equation:

$$tV0 = T_s - tV1 - tV2 - tV3 - tV4 \quad (5)$$

TABLE I. Calculation of dwell time $tV_i$ according to the reference voltage vector location (sector number).

| | | tV1 | tV2 | tV3 | tV4 |
|---|---|---|---|---|---|
| | 1 | +T1 | +T2 | +T5 | +T6 |
| | 2 | +T2 | +T3 | +T6 | -T1 |
| | 3 | +T3 | +T4 | -T1 | -T2 |
| | 4 | +T4 | +T5 | -T2 | -T3 |
| | 5 | +T5 | +T6 | -T3 | -T4 |
| Sector | 6 | +T6 | -T1 | -T4 | -T5 |
| | 7 | -T1 | -T2 | -T5 | -T6 |
| | 8 | -T2 | -T3 | -T6 | +T1 |
| | 9 | -T3 | -T4 | +T1 | +T2 |
| | 10 | -T4 | -T5 | +T2 | +T3 |
| | 11 | -T5 | -T6 | +T3 | +T4 |
| | 12 | -T6 | +T1 | +T4 | +T5 |

The switching sequence of the chosen voltage vectors must be also defined. Continuous and discontinuous switching sequences can be applied [5]. A continuous switching sequence is a modulation technique which guarantees two changes (from ON to OFF state, or vice versa) for all inverter legs within a sampling period. A discontinuous switching sequence occurs when one (or even more than one) inverter leg stops switching during a sampling period.

The proposed switching sequence is the continuous modulation presented in table II. The zero voltage vector is conveniently chosen to guarantee that each inverter leg switches twice (from the ON to the OFF state, and then to the ON state again, or vice versa) in a sampling period. There is one leg in each sector that switches four times. Figure 4 details the switching states using a reference voltage vector which is placed in sector 1. It can be seen that leg c is the special leg that switches four times for this sector. The zero voltage vector is applied three times during a sampling period: at the beginning and at the end of the sampling period during a $tV0/4$ dwell time, and at the middle of the sampling period during a $tV0/2$ dwell time.

TABLE II. Proposed switching sequence for each sector (rows)
and sample period segment (colums)

| Sector | $T_s$ | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | tV0/4 | tV1/2 | tV2/2 | tV3/2 | tV4/2 | tV0/2 | tV4/2 | tV3/2 | tV2/2 | tV1/2 | tV0/4 |
| I | 0-7 | 5-5 | 4-5 | 4-4 | 6-4 | 7-0 | 6-4 | 4-4 | 4-5 | 5-5 | 0-7 |
| II | 0-0 | 4-5 | 4-4 | 6-4 | 6-6 | 7-7 | 6-6 | 6-4 | 4-4 | 4-5 | 0-0 |
| III | 7-0 | 4-4 | 6-4 | 6-6 | 2-6 | 0-7 | 2-6 | 6-6 | 6-4 | 4-4 | 7-0 |
| IV | 7-7 | 6-4 | 6-6 | 2-6 | 2-2 | 0-0 | 2-2 | 2-6 | 6-6 | 6-4 | 7-7 |
| V | 0-7 | 6-6 | 2-6 | 2-2 | 3-2 | 7-0 | 3-2 | 2-2 | 2-6 | 6-6 | 0-7 |
| VI | 0-0 | 2-6 | 2-2 | 3-2 | 3-3 | 7-7 | 3-3 | 3-2 | 2-2 | 2-6 | 0-0 |
| VII | 7-0 | 2-2 | 3-2 | 3-3 | 1-3 | 0-7 | 1-3 | 3-3 | 3-2 | 2-2 | 7-0 |
| VIII | 7-7 | 3-2 | 3-3 | 1-3 | 1-1 | 0-0 | 1-1 | 1-3 | 3-3 | 3-2 | 7-7 |
| IX | 0-7 | 3-3 | 1-3 | 1-1 | 5-1 | 7-0 | 5-1 | 1-1 | 1-3 | 3-3 | 0-7 |
| X | 0-0 | 1-3 | 1-1 | 5-1 | 5-5 | 7-7 | 5-5 | 5-1 | 1-1 | 1-3 | 0-0 |
| XI | 7-0 | 1-1 | 5-1 | 5-5 | 4-5 | 0-7 | 4-5 | 5-5 | 5-1 | 1-1 | 7-0 |
| XII | 7-7 | 5-1 | 5-5 | 4-5 | 4-4 | 0-0 | 4-4 | 4-5 | 5-5 | 5-1 | 7-7 |
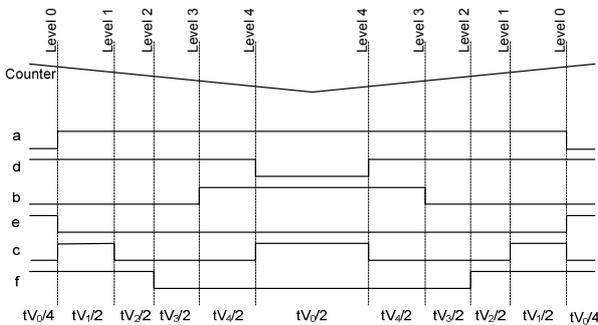


Fig. 4. Example of a continuous switching sequence using a
reference voltage vector located in sector 1.

## 3. FPGA implementation of the multiphase SVM

The system is shown in Fig. 5. The SVM technique is
implemented using a Xilinx Virtex IV FPGA [10], and
the reference is provided by an external microcontroller.
It also can be supplied by a PowerPC 405 processor
which is embedded into the FPGA, and use it to
implement the control algorithm. Figure 6 presents a
scheme of the FPGA implemented circuitry.
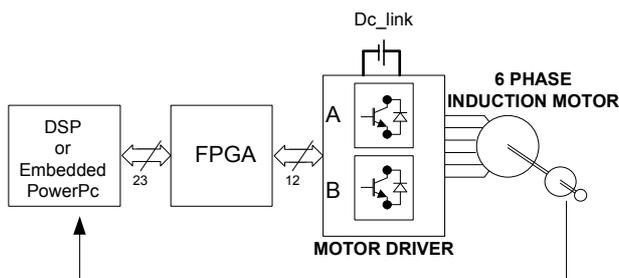


Fig. 5. System of the asymmetrical dual three–phase AC
machine.
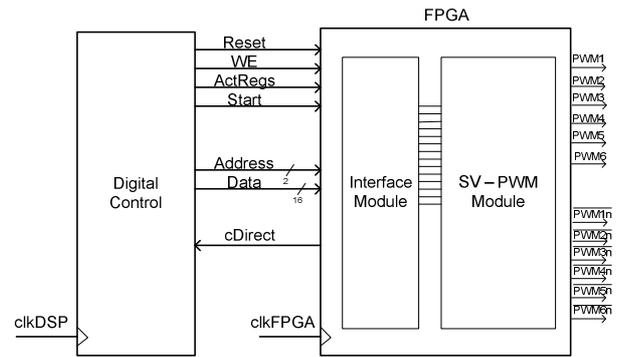


Fig. 6. Architecture of the proposed multiphase SVM control
technique.

Two modules have been designed: the interface and the
operational modules. The interface module allows
microprocessor access and indicates the control status.
The operational module, called SV–PWM module, gates
de VSI legs using the following input data: the reference
voltage vector in (α, β) coordinates, the sampling period
($T_s$), and the programmable dead time. A 23–bits data bus
links both modules. A detailed block diagram of the
interface module is shown in Fig. 7, while Fig. 8 depicts
the SV–PWM module.
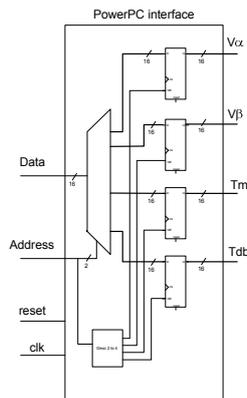


Fig. 7. Internal architecture of the interface module.
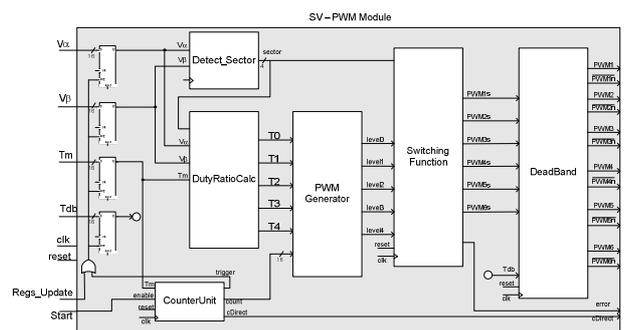


Fig. 8. Internal architecture of the SV–PWM module.

The basis of the SVM multiphase control technique is the
SV–PWM module which incorporates the following six
sub modules:

- The "CounterUnit" sub module which produces a
  triangular waveform using an up–down counter. It
  generates an end of sampling period signal to the
  microprocessor.
- The "Detect_Sector" sub module which evaluates
  the sector where the reference voltage vector is
  located.

- The "DutyRatioCalc" sub module which computes $tV0$ to $tV4$ dwell times and rescales them into a digital value, according to the sampling period.
- The "PWM Generator" sub module, that compares the outputs from the "CounterUnit" and the "DutyRatioCalc" sub modules.
- The "Switching Function" sub module, a Moore finite state machine which produces the ON/OFF gate times to the VSI legs, following a preconfigured sequence.
- The "Deadband" sub module which avoids short circuits in the VSI legs.

## 4. Obtained results

The overall design was downloaded and tested in the Xilinx ML403 Evaluation Board, using a XC4VFX12–100MHz FPGA. A picture of the experimental setup is shown in Fig. 9, while Table III summarizes the FPGA resources utilization. It can be deduced that the amount of available resources is large enough for the proposed application.
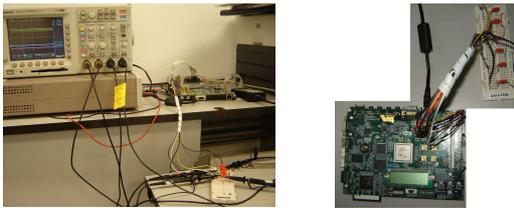
Fig 9. Pictures of the experimental setup.

TABLE III. Device utilization summary.

| Logic Utilization | Used | Available | Utilization |
|---|---|---|---|
| Number of Slice Flip Flops | 512 | 10,944 | 4% |
| Number of 4 input LUTs | 1,897 | 10,944 | 17% |
| Logic Distribution | | | |
| Number of occupied Slices | 1,091 | 5,472 | 19% |
| Total Number of 4 input LUTs | 1,907 | 10,944 | 17% |
| Number used as logic | 1,897 | | |
| Number of bonded IOBs | 36 | 320 | 11% |
| Number of DSP48s | 25 | 32 | 78% |

A series of experimental tests were performed in order to examine the properties of the implemented circuitry. Figures 10 to 14 show the obtained results. Figure 10 depicts the obtained voltage waveforms using a 50Hz stator voltage reference vector. The VSI leg pulsing outputs have been filtered using a low–pass filter to show the fundamental component. Four waveforms are shown; one corresponding to the VSI gate signal while the other are VSI gate filtered signals. Figure 11 shows two different phase voltages. The designed peripheral can achieve the full range of values of the reference module.
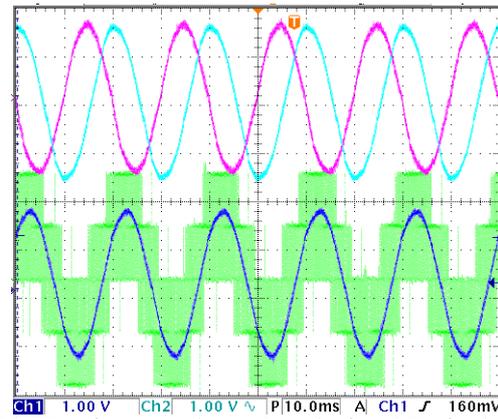
Fig. 10. Waveform experimental results for 50 Hz fundamental

For experimental purposes two values 0.7 and 0.5 are presented in figures 11.a and 11.b respectively. As well, it can be configured signal fundamental frequency, as can be seen in fig. 12.

It is important to remark that carrier frequency is also programmable. For a system clock of 100 MHz, the minimum carrier frequency is around 763 Hz, and it could reach up to a maximum 45 kHz. Some different carrier frequencies were tested and its results are presented in Fig. 13.
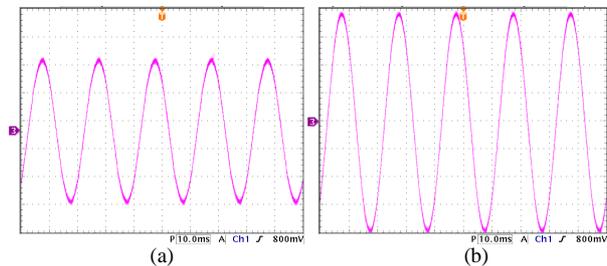
Fig. 11. Waveform experimental results for 50 Hz fundamental for two different reference vector modules. a) 0.7*VdcLink , b) 0.5* VdcLink.
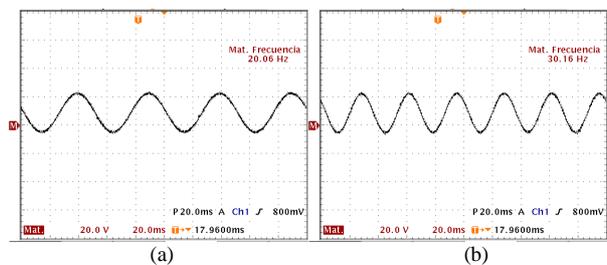
Fig. 12. Waveform experimental results for 6 kHz carrier frequency and 0.7*VdcLink reference. a) 20 Hz fundamental, b) 30 Hz.
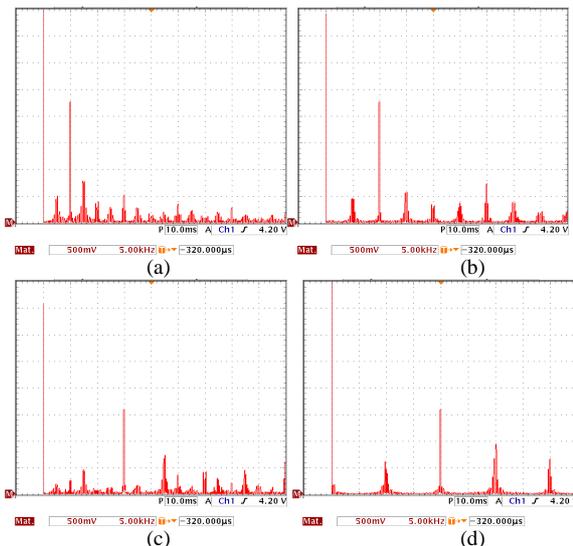
Fig. 13. Spectrum of SVM for different carrier frequencies. a)
2.5 kHz, b) 5 kHz, c) 7.5 kHz, d) 10kHz

Different dead band times can be configured depending on the system clock. In this case, it is programmable up to 2.56 us. This programmable dead time is sufficient for all kinds of power semi-conductors. Finally, Fig. 14 shows the "DeadBand" sub module behaviour for two different values that have been used: 1 and 1.5 us.
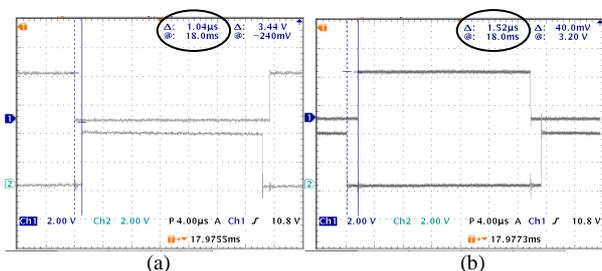


Fig. 14. Deadband module behaviour for a) 1us, b) 1.45us.

## 5. Conclusions

The area of multiphase induction motor drives has experienced a substantial growth in recent years. Research has been conducted worldwide and numerous interesting developments have been reported in the literature, particularly in the VSI–drive asymmetrical dual three–phase ac machine. However, the development of new microprocessor peripherals is necessary for the translation to multiphase applications of advanced digital control techniques like SVM techniques. This paper presents the design and implementation of a programmable SVM control IC for asymmetrical dual three–phase AC machines. The architecture of the FPGA implemented SVM multiphase control technique is discussed in deep, and experimental results are provided to examine the potential of the control method.

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