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e-Diagnostics of the Switchgear Equipment Using IEC 61850

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Abstract. The proposed implementation of e-diagnostics of switchgear equipment aims to improve the reliability indicators of the equipment and to reduce the costs of its exploitation. As far as fundamental diagnostics problems are concerned it is still essential to develop methods of calculating tests and diagnostic procedures, which are a base for an inference on the reliability state of the object. Generally it is done based on symptoms (characteristic for non-stationary acting object), which additionally expose processes of aging and wear, or based on functional model of a discrete object.
At the present, in many cases the digital part of IEDs is tested by application of a response function compression method. This method characterizes with relatively small control test effectiveness and it does not enable subordinating the tests results to the specific node of the IEC 61850 standard.
The paper introduces diagnostics of the digital part of IED's. It presents a certain inference engine on which one of the elements of the digital circuit is (with determined probability) in the inoperable state, if for any pin, (of some element) a fail result of the functional test has been observed. That conclusion is reached by applying the probability approach and knowledge of the digital circuit information net, being a certain digraph respectively described. The method of determining the important causal-effectual relation between the determined inoperable state of the circuit element and the fail result observed on some pins of the other element, using the information net of the circuit is presented.
Thereafter we provide some remarks on how to build the IED digital part functional testing, which may be executed under the command e.g. sent from the data concentrator.

Key words

fault localization, reliability model of IED's digital circuit, tests, diagnostic procedure, built in self-test.

1. Introduction

The main problems of the technical diagnostics of elements of the substation in the designed system have been divided in three different areas, in which different diagnostics methods and tools will be applied.

The structural model of a simplified switchgear system of the substation, in which the e-diagnostics is implemented, is shown in fig.1.

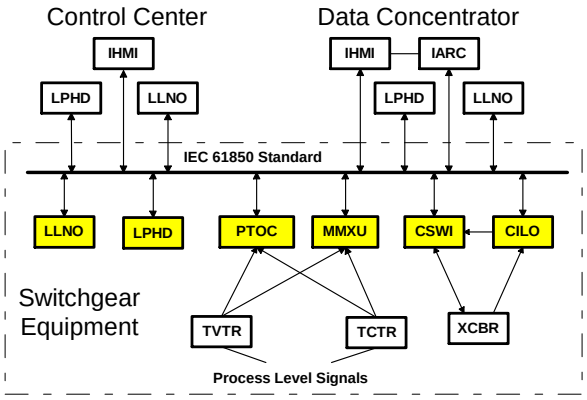

Fig. 1. Structure of the switchgear equipment as the logical nodes of IEC 61850(the yellow indicate the nodes, which are the virtual reproduce of the elements of IED digital part)

There are three areas distinguished within the switchgear equipment: the switched non-stationary elements (e.g. circuit breaker), converter of analogue signal inputs (from the process bus) that is a part of IED's (called shortly merging unit) and digital part of IED's device, treated as a discrete object.
For the circuit breaker the method of the symptom diagnostics will be put into practice ([14]). Some conclusions may be drawn about the technical state of such an object by observing how the object operates i.e. its main output (product) and dissipated output, where different kinds of residual processes are being observed as e.g.: the temperature, distortions, electromagnetic phenomena, oscillation or the noise. The information about the symptoms will be collected in a database of the data concentrator, which (from a point of view of the IEC 61850 standard) is serving in the system as „Client/Server".

Simultaneously a data concentrator software application enables us to learn about the reliability state of diagnosed objects and supports us in making the right diagnosing decision.
As for the analogue inputs of IED's (the merging Unit) a new diagnosing method will be applied. The method is based on assumption that the reliability state of the merging unit is tracked on-line systematically.
A separate paper will be devoted to the method. In brief the method relies on periodic injection of an analogue test signal to the tested inputs. If the measured value rises by the test value with a determined probability it is possible to say that the merging unit is in its operable state.
As for the discrete objects (digital circuit) a diagnostic testing based on a functional model of these objects will be applied.

In this paper we would like to present some methods and tools to solve the problem of control testing of the IED's digital part. The strategy of the diagnosing the technical object by the functional testing of its clusters is known and applied in the many fields of the engineering. In the discussed case, the problem lies in applying that approach to the modern digital circuit and searching the practical method of its solution by a minimum amount of the object information and generally by the many technical limitations, which specify the set of the clusters accessible for the functional testing circuit. Typical modern digital circuit, as a rule, contains the bidirectional information pins, complex switching elements, and redundant aids and is made in the surface mounting technology and characterized by a high degree of the structural complexity.

The digital device diagnosis (by control testing of its clusters), among other things, requires the solution of problems relating to the assignation of digital circuit clusters, the generation of control tests for these clusters, the determination of the expected value of the generalized cost of implementing of the testing of these clusters, "the largest" (possible obtainable) diagnostic insight and the method of the inference on the reliability state of the circuit elements based on the result of the cluster test. The formal description of the information net of the digital circuit and the method of the inference on the reliability state of the circuit elements based on the knowledge of its information net and the observed response function of the test of the determined circuit cluster, are presented.

In many cases the digital part of IED is tested by application of the response function compression method (for example, different types of signature analysis). This method characterizes with relatively small test checking effectiveness and generally small diagnostic insight (thoroughness). It does not give the possibility of subordinating the tests results to specific node of IEC 61850 communication standard, and obtaining the same right answer on the request for the node "health" (the reliability state of elements, mapped in the form of the node).
Modern digital equipment is characterized by a generally very high degree of structural complexity, the presence of integrated circuits with very large scale integration, the complex switching components and bi-directional information terminals, the assembly of the electronic packages and the use of the redundant elements and/or built-in diagnostics (including diagnostic bus IEEE 1149.1, or BIST module - Built-In Self Test). Normally, the BIST features of the digital equipment are intended to test specific subsets of its components (a cluster). Thus, it is easy to use the testing strategies of the clusters digital circuit for the localization of the faulty element of such a device.

In may cases, solving the above problems without computer support is impossible.
Thus, it has become necessary to develop new computer-aided tools supporting the testing and diagnosis of digital devices. One such tool, based on an analysis of the functional-reliability structure of the digital device, is its information net.

2. Information net of the digital device

An adequate reliability model of digital device can be built in such way that both the device as a whole and each of its separate elements can be considered as certain finite automata and the rules of interaction of these elements result from the connections network between specific pins of device (as a whole) and each of its separate elements. Of course, it must comply with the requirement that if a set of isolated elements of the device ignores some of its modules, it is either known that these modules are in the functional operable state, or we know what is the impact of their faults on the type of transformations carried out by certain isolated device elements or/and the rules for their interaction.

Let us remind that a functional reliability model of the digital circuit is the relation $S \to (N \equiv A)$, where S and N mean respective sets of real and abstract reliability states of the circuit, and A, $(A = X \to Y)$ is a set of the deterministic finite automaton with such edition, that $n_o, (n_0 \in N)$ called operable state is identified with automaton A_0, $(A_0 \in A)$ describing proper circuit operation, and each state n'', $(n'' \in N \setminus n_0)$ called the inoperable state is identified with respective automaton A'', $(A'' \in A \setminus A_0)$ describing determined faulty operation of the circuit.
Of course: $Card\ \ N \equiv Card\ \ A = Card\ \ Y^{Card\ \ X}$.

Let $P(N') = \{N_1', \ldots, N_K'\}$ denote K- divided ($K \geq 2$) division of set N', ($N' \subseteq N$).
Forced input state w is called *a test towards division* $P(N')$ if the reliability states n', n'' being in a different division subset, in which the circuit reactions are different, exist, that is if:

$$\exists [n', n'' \in N' : (n' \in N_j') \Rightarrow (n'' \notin N_j'), 1 \leq j \leq K] : \\ : r(w, n') \neq r(w, n'') \quad (1)$$

where: $r(w,n)$, $(w \in W)$ is the reaction (functional response) of the circuit being in the reliability state n, $(n \in N)$.
The test towards the division $P(N) = \{n_0, N \setminus n_0\}$ is called *a control test*, while the test towards the division

$P(N \setminus n_0)$ - *a localization test* against the required depth localization of the fault, as defined by the division.

The error of the control test is *a' posteriori* probability of the event $n \neq n_0$; thereafter occurs the event $r(w) = r(w, n_0)$.

$$\gamma(w) = \Pr\{ n \neq n_0 \mid r(w) = r(w, n_0)\} \quad (2)$$

The definitions mentioned above help us to determine the diagnostic procedure for the digital circuit part of IED.

The information net of digital device is called a described digraph without loops built on the set of all information digital device pins that response function (reaction on the test) observed in any of these pins, contrary to the standard reaction (reaction [response] in device operable state) suggests that the fault element of the device is an anti-attainable element (in this digraph) from this node. Since digital devices generally include bi-directional pins, and the information net is a digraph, each bi-directional pin (occurring in the device) is presented in the form of two (twin) nodes in the set of the digraph, respectively symbolizing that pin, where it meets the input and output features (the specific component or device as a whole).

The reliability-information matrix $M(e)$ of the element e, ($e \in E$) is called a binary matrix such that $m_{jk} = 1$, ($m_{jk} \in M(e)$) if and only if the transformation carried out on the output v_k ($v_k \in V^-(e)$) of element e in its operable state $n_0(e)$ depends significantly on changes at its input v_j, ($v_j \in V^+(e)$).

The information graph $G(e)$, ($G(e) = < V(e), U(e) >$) of the element e ($e \in E$) is called a graph, which transmission matrix is the reliability-information matrix $M(e)$ of this element. Of course, the graph $G(e)$ is a simple graph, it is two divisible Berge's graph.

Note also that among the elements of E, there may be present elements (for example, multiplexers, decoders, FET-switches), which due to their nature realize transformation requiring graph $G(e)$ probabilistic description.

Let $V^s(e)$, ($V^s(e) \subseteq V^+(e)$) denote the node set referring to the control input pins of the element e, and $v^p(u)$ and $v^k(u)$ - beginning and ending node of the arc u, ($u \in U$) respectively.

Let us denote:

$$U^s(e) = \{ u \in U(e) : [v^p(u) \notin V^s(e)] \wedge \wedge [v^k(u) \in \Gamma V^s(e)] \}, \ (e \in E) \quad (3)$$

where: $\Gamma V^s(e)$ denotes the consequent set (in the graph $G(e)$) of the node set $V^s(e)$, (Fig. 2) and: $U^s = \bigcup_{e \in E} U^s(e)$.

Let $\rho(u)$, ($u \in U^s$) denote the probability, that in the stationary conditions of the operable state of the digital circuit, the value of the variable $y(v^k(u))$, referring to the node $v^k(u)$, is equal to the value of the variable $x(v^p(u))$ referring to the node $v^p(u)$ (the probability, that the data transfer performs by the arc u):

$$\rho(u) = Pr\{ y(v^k(u)) = x(v^p(u))\} . \quad (4)$$

Of course: $0 < \rho(u) < 1$, ($u \in U^s$).

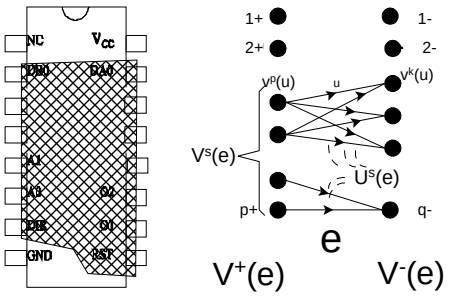

Fig.2. The sample graph G(e) of a integrated circuit.

The information net of the digital device we called the three ordered:

$$I = < G \ ; \psi(v), v \in V^{BD-} ; \ \rho(u), u \in U^s > \quad (5)$$

where:

G - a Berge's graph $G = < V, U >$ without loops ($< v', v' > \notin U, v' \in V$) defined on the set of information pins of elements and the device;

$\psi(v)$ - the probability that a bidirectional information pin corresponding to the node v of graph G, meets (in stationary operating conditions of the operable device) an output function.

Thus, the graph $G = < V, U >$ is defined on the set of nodes V, the size of which is equal to the sum of the number of the unidirectional information pins and the doubled number of bidirectional information pins of the individual elements of the device and the device (as a whole denoted as e_0) and on the arcs set U, which are interaction net mapping arcs (calculated based on the network connections), and the arcs of graph $G(e)$ ($e \in E$), while usually the graph $G(e)$ is even the subgraph of the graph G.

The formalized description of the construction of information nets, as well as some of its properties are given herein [7]. One way to reduce the computational complexity of solving the problems is the device decomposition into "sub-circuits" (clusters) that can be diagnosed independently. The criteria of this decomposition should meet the following requirements :

$$\neg \exists P' \in P^2(V^+(e_0)); P'' \in P^2(V^-(e_0)); A \in P'; \ B \in P'' : [\forall v \in B : V(e_0, n_0, v) \cap A \neq \varnothing] \quad (6)$$

where $P^2(C)$ denotes bipartite division of the set C, $V^+(e_0)$ and $V^-(e_0)$ mean respectively the sets of nodes in graph G corresponding with inputs and outputs of the device (as a whole) and $V(e_0, n_0, v)$ - a set of the information inputs of the device on which (in the operable state n_0 of the device) the state of the output

signal mapped as a node v depends significantly.

Note, that the device information net includes information, which (among other things) is used to support the process of analyzing diagnostic properties of the device, the device decomposition into modules, calculating the tests and diagnostic procedures, the design of the device with the built-in self-test module, or to support the diagnosis of the device. In general, the information net of the device may be derived from a CAD system ([8]), supporting the design of the device. Additional knowledge, for example, of the reliability model adopted by the elements and the device (as a whole) must be entered by an expert. Without going into details, let us note, that the acquisition of the knowledge of specific expression (5) is a separate problem, which may be solved by the analytical methods, or (and) the simulation test methods.

3. Control testing of the digital clusters of the IED

We call the cluster F of a digital device an ordered three:

$$F =< E(F); \{A(e)\}, e \in E(F); I(F) > \quad (7)$$

such that:

$$(\exists e \in E(F) : A(e) \neq A_0(e)) \Rightarrow (A(F) \neq A_0(F)) \quad (8)$$

where $E(F)$ - a set of elements of a fragment F, ($E[F] \subset E$), $A_0(e)$ - the transformation performed by the element e, in its operable state; $A_0(F)$ - the transformation carried out by the cluster F, in case when all elements of that cluster are in their operable states; $I[F]$ - the information net between the elements of the cluster F. The cluster of a digital device is thus a new system created (for the diagnosis) with a system, which is the digital device. Net $I[F]$ (in this particular case) may be a partial graph, the subgraph of the information net graph G, or the modification of the information net, that describes a newly-organized net of the interaction between the elements e ($e \in E(F)$).

Of course, the newly-organized interaction net cannot conceal any fault, which should be verified by checking the designated subset of such elements. Together with the cluster information net it has to meet the requirements specified in the definition of the cluster. Only such a cluster can be considered acceptable for the control testing.

The control testing of the functional cluster is understood as a particular type of experiment [measurement], which aim is inference based on the observed responses [answer] $r(F,w)$ to the force in the functional input states w, ($w \in W(X(F))$) on whether the unknown reliability state of the cluster F is an operable state or one of its possible inoperable states. The reasoning for this is generally based on an appropriate comparison of the observed response $r(F,w)$ to the forced functional input states w with the known standard response $r(F,w,n_0)$ in the operable state of the cluster.

One of the major problem for diagnosis (in terms of faulty element localization) that needs to be solved is development of methods of inference (with a specified credibility) of the a' posteriori probability distribution of the elements fault of the digital device based on the observation of the response $r(F,w)$. As a result of comparing the obtained response $r(F,w)$ with the standard (expected) response we obtain either $r(F,w) \neq r(F,w,n_0)$ or $r(F,w) = r(F,w,n_0)$. In the first case it is known that the forced input states w ($w \in W(X(F))$) is a test in respect to some fault of the cluster F, and so the inoperable elements of device is the element of the set $E(F)$. In the second case, either the inoperable element is an element of $E \setminus E(F)$, or an element of $E(F)$, anyhow the forced input states w are not a test in respect to the specific fault of that cluster F.

The inference way based on the information net on which of the elements (with a specified probability) of the device in its inoperable state, if for some output pin (some element of the device) test results were incorrect, is given in work [4]. Of course, from the definition of the cluster one can also derive a definition of the sets $X(F)$ and $Y(F)$ of the cluster, which are respectively domain and the image of the transformation $A_0(F)$, performed by the cluster in the device operable state. A cluster control test that is testing the correct performance of the transformation $A_0(F)$ may be build on these sets.

A passive cluster of digital device is called cluster F, for which $X(F) \subseteq X$ and $Y(F) \subseteq Y$ (X and Y are, respectively, the domain and the image of the transformation $A: X \rightarrow Y$, performed by the device).

An active cluster is called cluster F for which $X(F) \not\subset X$. Note that, that the active fragmentation may be performed, for example, by application of the diagnostic bus by IEEE 1149.1 standard.

4. The localization procedure of the faulty digital item of the IED

Let $\Phi(E)$ denote the set of all possible to create clusters from the elements subsets of the set E elements of the device.

The cluster F ($F \in \Phi[E]$) created from the elements of the set $E(F)$ is called generalized device test in respect to the set E' ($E' \subseteq E$, $Card\ E' \geq 2$) of the recognized elements of the device, if:

$$(E' \cap E(F) \neq \varnothing) \wedge (E' \not\subset E(F)) \quad (9)$$

and a bipartite division of $P_F^2(E')$ the set E' such that:

$$\{E' \cap E(F), E' \setminus E' \cap E(F)\} \quad (10)$$

is called the product of a generalized test F in respect to the set E'.

Let $T(E')$, ($T(E') \subseteq \Phi[E]$) denote the set of generalized tests in respect to a set of E'. The set $T^C(E)$ is called a generalized complete test for the elements of division $P(E)$ if:

$$\forall E' \in \Lambda[P(E)] \exists F \in \Phi[E] : F \in T^C(E') \quad (11)$$

where: $\Lambda[P(E)] = \{e', e'' \in E : e' \in E'' \Rightarrow e'' \notin E''\}$, $(E'' \in P(E))$.

Analysis of the information net of the device is expected to seek the best possible way to separate the possible set of clusters of the device, for which control test for these clusters can locate the inoperable cluster of the device with the required degree of insight.

The localization procedure φ, which consists of the clusters control tests of the device can be presented in the form a described, binary dendrite G ($G =< V, U >$):

$$\varphi =< G; \{E(v')\}, v' \in V; \{F(v'')\}, v'' \in V \setminus V^K; \{\delta(u)\}, u \in U > \quad (12)$$

such that:

$E(v_0) = E$, ($\Gamma^{-1}(v_0) = \varnothing$) and $F(v) \in T(E(v))$,

where: $E(v)$ denotes, recognized in the v-step of the procedure, the set of elements devices which include the inoperable element, $\delta(u)$ - the function assigning the arc u of the response value to forced input states applied in this step of procedure, corresponding to such a node (in the graph G), which is the beginning node of that arc, while $V^K = \{v \in V : \Gamma(v) = \varnothing\}$.

The set $T_\varphi = \{ F(v) \} v \in V \setminus V^K$ is called *the generalized base test of the procedure* φ, and division $P_\varphi [E] = \{ E(v) \} v \in V^K$ - *the product* of this procedure.

Note that generally in many practical cases there is a large number of localization procedures, meeting certain requirements. Thus arises the practical problem of determining the procedures optimal in the specified sense.

Let $K(F)$ denote the generalized costs of the cluster F, taking into account both the cost of necessary modifications to the interaction net device (the cluster isolation) and the cost of implementing a control test of this cluster. Knowing the generalized cost $K(F)$ of the clusters, belonging to T_φ, we can determine the expected value $E[K(\varphi)]$ of the generalized cost of this procedure. In determining the quasi-optimal procedures (e.g. such that: $E[K(\varphi)] \cong \min$), we usually build on the fact that :

$$T_\varphi \in T^C[P(E)] \Rightarrow (P_\varphi(E) \prec P(E)) \quad (13)$$

and

$$E[K(\varphi)] \le \sum_{F \in T_\varphi} K(F). \quad (14)$$

In order to reduce the computational complexity of algorithms for determining quasi-optimal procedure in the first place, we can (basing on the information net) designate a set of the clusters of the device, which is a generalized complete test of $P(E)$ (required insight localization of the inoperable element) and the sum of the clusters cost of this set has the minimum value. Then, using only clusters of this set a quasi-optimal procedure can be designated e.g. by application of the maximum efficiency information method.

We said, that the circuit is ($P(E), K$) testable (diagnosable), if the diagnostic procedure φ such, that the product of this procedure $P_\varphi(E)$ is sub-partition of the required partition $P(E)$ (required localization insight of the circuit inoperable element), exists, and the expected value $E[K(\varphi)]$ of the generalized cost $K(\varphi)$ of this procedure realization does not exceed the value K, that is if:

$$[P_\varphi(E) \prec P(E)] \wedge [E[K(\varphi)] < K \quad . \quad (15)$$

Using the inference mechanism, based on the information net of the device, we can designate a quasi-optimal subset of the possible clusters of a device, based on which a quasi-optimal (in terms of the generalized cost of implementation) localization procedure $\varphi_{q\,opt}$, which meets the requirement(15), can be designated.

5. Some remarks on the design of the built-in tests in the IED digital part

The IEC 61850 standard is a reply to the need of standardizing of the communication methods, which describes the way of the information exchange between station devices. This standard is being more and more universally applied in the world power industry.

The IEC 61850 standard (among other issues) will have an impact on the functional properties testing. Using the substation configuration language, an automation of the functional tests is possible. A test strategy (defined by the diagnostic procedure) is required to optimize the number of tests, their effectiveness and diagnostic insight.

Let us notice, that the features offered by the IEC 61850 standard (among other things) give us the possibility to put logical node (or logical device) in the test mode. This possibility is introduced to support the ability to perform certain forms of functional testing while the system is in operation.

As described in the IEC 61850 standard (part 7-4) certain features have been introduced as additional quality identifiers (e.g.“Mod” - mode) that should be used to distinguish between the different functional modes (e.g. "test", ”test-blocked“, “operating blocked” “operating OFF” and "operating ON" mode). Each logical node contains a data attribute "Mod" (mode). If “Mod” equals “test” or “blocked test”, it moves the functionality of the logical node into the test mode. If the specified mode is set, then the data attribute “Beh” (behavior) reproduces the mode settings. If the mode is set in the logical node 0 (LLN0), it changes automatically the mode of the other logical nodes of that logical device.

Generally, due to the construction of the IED digital part, it will be difficult to unambiguously subordinate the logical nodes of IEC 61850 standard, to the definite clusters of the IED digital part. In particular, this applies to such elements as: communications processor, memory, etc., which are usually partially mapped in several logical nodes.

These new concepts, introduced by the standard, are required in particular during the isolation of the cluster under test from the rest of the digital part of IED. The use of the active clusters (i.e. clusters created specifically at the time of testing), usually gives us the

opportunity to such isolation as well as enables us to perform the tests on-line. The disadvantage of such solution is the need to expand the system (the electronic circuitry) with additional components required to change the networks connections, aiming at separation of the cluster (thus increasing the size of the tested elements set).

The passive fragments do not require the electronic circuitry expansion, neither do they map the sufficiently exact nodes of the standard, and make executing tests (as a rule) off-line possible. The exception is such designing of the digital part of IED, that during the design there is opportunity to create the tests (i.e. so called the concurrent designing) using the design for testability (DFT) techniques.

In any case, embedding of the diagnostics requires the development of the control tests of the clusters and their standard reactions (responses in the operable state). Depending on the structure of the electronic circuits different method for the cluster control test generation are used. Let us only remind, that for the regular structure of the circuits (e.g. the memory) the algorithmic method of test generation is used, and for the irregular structure (e.g. the processor) the exhaustive or pseudo-exhaustive methods are used. The developed tests (the matrix of input forced states and the matrix of responses expected in the operable state of tested cluster) should be built into some digital circuitry of the IED. These built-in elements should be so design that it should be possible to start the test execution after receiving an external command (e.g. command having data attribute “Mod” equals “test” or “test-blocked”) sent from the data concentrator for a given logical node of IEC 61850 standard.

After completing the test, the global information about the test result is passed to the data concentrator as a command data attribute “Health”. For real-time communication ([10]), a test flag of GOOSE seems to be more suitable. The GOOSE values should not be used for operational purposes in that case.

The global information received about test result requires a careful analysis of inference about the state of each node of the IEC 61850 standard, if separate clusters do not reflect virtual nodes, and it seems that the result of their testing may indicate the fault, which concerns several nodes.

Therefore, building of an appropriate diagnostic procedure ([11]) is very important. Without going into details, it should only be noted, that (generally) for a given set of the clusters a lot of control and localization procedures can be build. Choosing one of them (in terms of inference about the state of each logical node) is one of the major problems at the design stage of the built-in tests and the procedure.

6. Conclusion

The approach presented above is based on the diagnostic strategy of control testing of circuit clusters. The described approach to the localization of the faulty element of a digital part of the IED is of course not the only one possible. It seems that the distinguishing feature of this approach is the ability to search for the best partitioning variant (passive and active clusters) of the device, providing the insight required localization of the inoperable element. This should (among other things) contribute to the wealth of the design tools for devices having redundancy and self-diagnosis.

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