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High efficiency Bridgeless Unity Power factor CUK converter Topology

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Abstract: A step-up bridgeless single phase ac-dc power factor correction (PFC) rectifier based on Cuk topology is proposed for high voltage battery charger application. The proposed topology consists of common input stage and parallel output stages. It utilizes one control signal over the whole line cycle. In addition, the proposed converter exhibits low inrush current and low magnetic emissions as classical Cuk topology. The bridgeless topology results in lower conduction losses as compared with conventional Cuk converter. Simulation and experimental results are presented along with the theoretical analysis.

Key words

Bridgeless rectifier, Cuk topology, DCM, low in-rush current and PFC.

1. Introduction

Power supplies with active power factor correction (PFC) techniques are required for wide range of applications for communication, automotive, computer and biomedical industries. All of these applications are required to meet industry standards such as the IEC 61000-3-2. In addition, it is highly recommended to meet new industry standards such as the 80 PLUS initiative. Many papers have been published in the literature to provide a solution for single-stage power factor correction (PFC) integrated topologies [1-7]. These solutions have been effective to provide cost-effective approach for achieving both the function of high PFC and fast output voltage regulation.

Most of the PFC rectifiers utilize boost converter at their front end. Boost converter provides many advantages such as natural power factor correction capability and simple control. However, low voltage applications such as telecommunication or computer industry an additional converter or an isolation transformer is required to step down the voltage. However, classical boost arrangement has lower efficiency due to significant losses in the diode bridge [1]. In addition, boost converters suffer from high inrush current which increases the cost of safety required disconnection devices between the load and the line voltage. To minimize the losses of the full bridge, many bridgeless PFC rectifiers have been introduced to improve the rectifier power density and/or reduced noise emissions [2]-[5] via soft switching techniques or coupled magnetic topologies.

Several non-boost bridgeless rectifiers have been published lately [6]-[10]. A bridgeless PFC rectifier based on Sepic topology is presented in [8]. However, the topology has only a step up capability like a boost transformer; however, an isolation transformer can be used to step down the voltage, hence increasing the cost and size of the rectifier. Even though Cuk converter topology is typically a lower efficiency converter, however it presents many advantages, such as isolation capability, step up/step down output voltage, continuous output current and lower electromagnetic emissions.

In this paper, high efficiency Cuk topology is proposed. The proposed topology is performance is evaluated based on component count, efficiency, total harmonic distortion (THD) and complexity. The proposed topology has an inherent low inrush current. In addition the proposed topology performance is compared with full bridge Cuk converter.

2. The Proposed CUK PFC Converter: Operation & Analysis

Figure 1a shows the proposed Cuk topology. This converter consists of single input stage for both the positive and negative half cycles of the line voltage. On the other hand, it has two output stages connected to the switched input voltage; each stage operates during one half line cycle. The converter active components during the positive half cycle are shown in Fig. 1b while the converter equivalent circuit during the negative half cycle is shown in Fig. 1c. The proposed converter utilizes two switches (Q_1 & Q_2). Q_1 is turned on/off during the

positive half-line cycle while Q_2 is switched on/off during the negative half cycle. The converter has inherent high power factor when operating in discontinuous inductor conduction mode (DICM) because the line current is proportional to the input voltage. The converter operation during the positive half-line cycle is discussed below:

Stage 1 [0, D_1T_s]: In this stage, switch Q_1 is switched on and diode D_{o1} is reversed biased by the capacitor voltage (V_{c1}). The output diode D_{o2} is reversed biased by capacitor voltage (V_{c2}). The input voltage is connected to ground directly. The three inductors are charging up by the input voltage as shown in Fig. 2a. This stage ends when switch Q_1 is turned off.

Stage 2 [D_1T_s, D_2T_s]: This stage starts after Q_1 is switched off and diode D_{o1} turns on simultaneously as shown in Fig. 2b to provide current path for the output inductor current L_{o1}. This stage ends when diode (D_{o1}) current goes to zero.

Stage 3 [D_2T_s, T_s], this stage is reached when both the active switch and the output diode are off. The equivalent converter circuit of this stage is shown in Fig. 2c. Notice that there are no semiconductor devices conducting in this stage. The freewheeling stage ends when the new switching period starts. It shall be noted that to guarantee DCIM operation D_2T_s must be less than T_s. Theoretical inductor currents waveforms over one switching cycle during the positive half cycle of the input voltage are shown in Fig. 3.

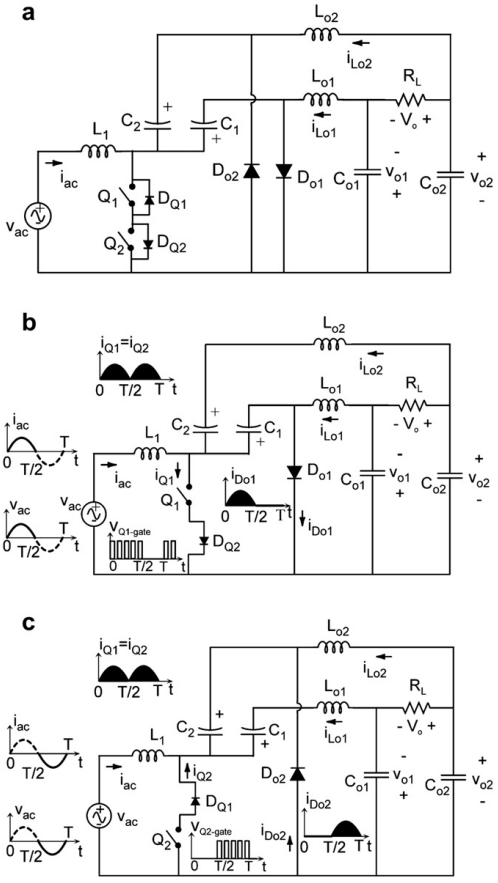

Fig. 1. (a) Proposed bridgeless Cuk rectifier (b) Positive half line cycle, (c) Negative half line cycle.

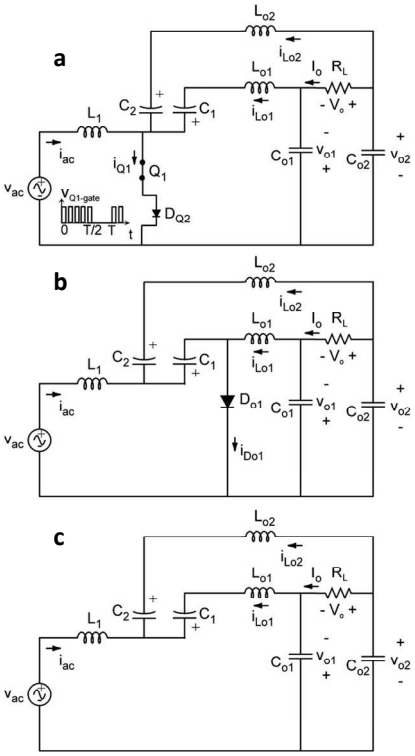

Fig. 2. The converter equivalent cycle over one switching cycle (a) First stage, (b) Second stage, and (c) Third stage.

A. Steady State Analysis

The proposed topology is analysed assuming lossless system and pure sinusoidal input voltage. In addition the output capacitors are assumed to be large enough to hold the output voltage constant over the whole line cycle while capacitors C1 and C2 are assumed large enough to hold the voltage constant over switching cycle. The input output voltage ratio is obtained by applying the volt second balance on the inductor and expressed as:

$$D_2 = \frac{2D_1}{M}\sin(\omega t) \tag{1}$$

where, $M = \dfrac{V_o}{V_m}$ is the conversion ratio of the average output voltage (V_o) to the amplitude of the input voltage (V_m) and ω is the line angular frequency

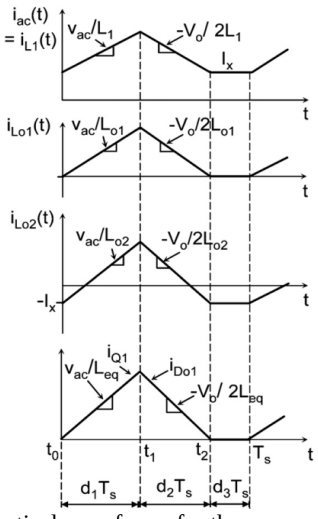

Fig. 3. Theoretical waveforms for the proposed converter.

B. Voltage Conversion Ratio M (D1, K)

The voltage conversion ratio as a function of the conduction parameter K is obtained by equating the input and output powers.

$$M(D_1,K)=\frac{D_1}{\sqrt{2K}} \tag{2}$$

where, K is a unit-less parameter and can be expressed as:

$$K=\frac{2L_{eq}}{RT_S} \tag{3}$$

C. DICM Operation Constraints (K_{crit})

To operate in DICM, The following inequalities must be held:

$$D_1+D_2<1 \tag{4}$$

The critical value of K as function of M to operate in DICM (K_{crit}) is obtained by substituting Eq. (1) and (4) into Eq. (2).

$$K_{crit}<\frac{1}{2(2\sin\omega t+M)^2} \tag{5}$$

D. Large Signal Model

The input-output ratio can be derived as expressed in the following equation.

$$M=\frac{V_o}{V_m}=\sqrt{\frac{R_L}{2R_e}}\ \text{Where}\ R_e=\frac{2L_e}{D_1^2T_S} \tag{6}$$

Where L_e is the parallel combination of inductors L_1, L_{o1}& L_{o2}, D_1 is the duty cycle where switch Q_1 is on and T_S is the switching period of Q_1. The network input and output port can be expressed as shown in Fig. 4.

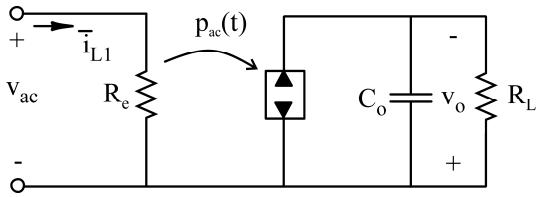

Fig. 4. Large signal model of the general averaged equivalent circuit in a converter operating DCM.

E. Stresses

The voltage stresses of the switches are shown in Fig. 5. The voltage and current stresses of the converter components are shown in Table I. All stresses are normalized with respect to the output voltage and load current. Converter stresses are required for design purposes.

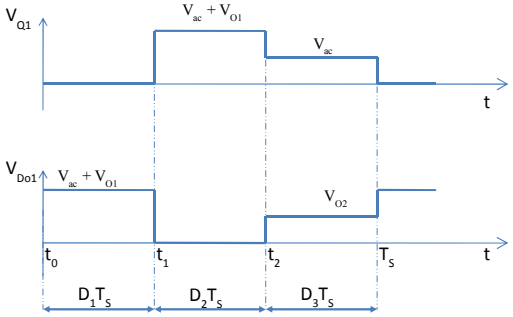

Fig. 5. The semiconductor switch and the diode voltage stresses.

Table I. – Current and voltage stresses

Component	Voltage	Current
Q_1, Q_2	$\frac{2+M}{2M}$	M
D_{o1}, D_{o2}	$\frac{2+M}{2M}$	M
C_1, C_2	$\frac{2+M}{2M}$	$\pm\frac{3}{2}$
C_{o1}, C_{o2}	$\frac{1}{2}$	$\frac{1}{2}$
L_1	$\frac{1}{2}$	M
L_{o1}, L_{o2}	$\frac{1}{2}$	$\pm\frac{3}{2}$

3. Simulation Results

The proposed modified Cuk rectifier is designed for the following operating point: peak input voltage of 100 V_{rms}, line frequency of 50 Hz, output voltage of 250 V, switching frequency of 50 kHz, and output power of 125 W. For accurate simulation models, actual semiconductor devices are used in the simulation; D1N5402 are used for the diodes and irfb4332pbf for the active power switches. The circuit components used in the simulation are chosen as follows: L_1 =2 mH, L_{o1} = L_{o2}= 50 µH. Moreover, an equivalent series resistor (ESR) of 20 mΩ is placed in series with all the inductors to model the inductor losses and a 50 mΩ ESR is placed in series with all capacitors to model the capacitor losses. Simulation studies were performed using ORCAD software package, to verify the analysis results.

The input voltage and current are in-phase as shown in Fig. 6(a). The total harmonic distortion in the line current is 0.17% and the efficiency is 94%. The output voltage with respect to the input voltage is shown in Fig. 6(b), where the output voltage meets the requirements. It should be noted that the diode starts conducting after the switch is turned off and the current goes to zero before the end of the cycle which ensures DCM as shown in Fig. 7(a). Fig. 7(b) shows the three inductor currents over a switching cycle. The inductor currents have proportional slopes over the three different stages of a switching cycle. Thus, the three inductors can be coupled which lead to lower costs and smaller size. In addition, the three inductors are being charged by the input voltage when the Q_1 is conducting, but when the diode D_{o1} is conducting, the three inductors are discharging through the output capacitors. The proposed rectifier harmonics is shown in Fig. 8 along with standard EN 61000-3-2 requirements. As shown in Fig 8, the converter satisfies EN 61000-3-2 requirements.

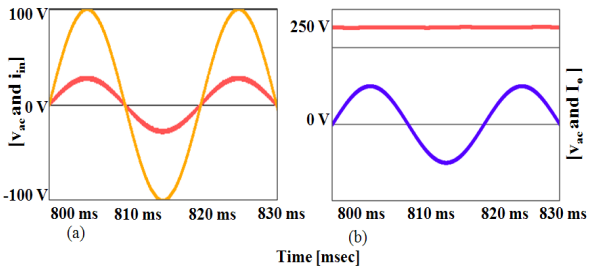

Fig. 6. Simulation results for the proposed rectifier: (a) Input current and input voltage, (b) Output voltage with respect to the input voltage.

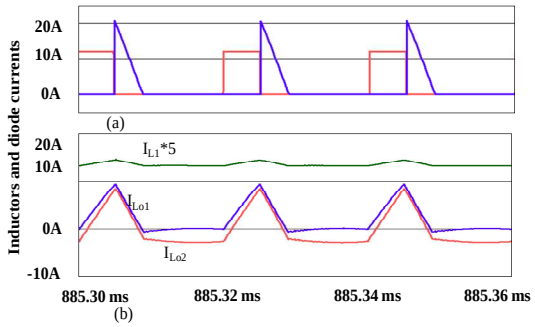

Fig. 7. Simulation results: (a) V_{Q1} and i_{Do1}, (b)I_{L1}, I_{Lo1}, and I_{Lo2} .

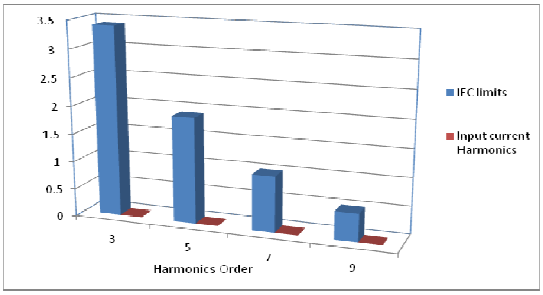

Fig. 8. Simulated input current harmonics of the proposed rectifier as compared with IEC 1000-3-2 standard

4. Experimental Results

The bridgeless DCM Cuk rectifier prototype test is validated at the same operating point as the simulation. A high frequency input filter is used at the voltage input to rectify the high frequency switching component of the line current. Fig. 9(a) shows the input current and line voltage. It can be seen that the line current and phase voltage are in phase. The load current and output voltage are shown in Fig. 9(b).The inductor currents I_{L1} and I_{Lo2} over a switching cycle are shown in Fig. 9(c), while Fig. 9(d) shows I_{Lo1} and I_{Lo2} waveforms. The current waveforms are in DICM as expected. The converter efficiency was measured to be about 94% at the desired operating point.

5. Conventional Cuk versus the proposed Cuk Rectifier

Comparison between the conventional Cuk and the proposed Cuk rectifier is shown in Table 2. The proposed bridgeless topology has fewer semiconductors in the current conduction path over the whole switching cycle. However, it has one additional switch compared with the conventional Cuk. Nonetheless, the switching losses are the same because only one switch is active over a switching cycle. The current stress in the output diode of the proposed rectifier is less because it conducts only over half line cycle. Also, the proposed rectifier has a floating switch which requires additional gating circuitry. In addition, the output voltage of the proposed topology is floating with respect to the input voltage. The efficiency for the conventional Cuk is 92% while it is 94% for the proposed Cuk rectifier. Moreover, the THD is 1%, which is higher as compared to the THD of the proposed topology.

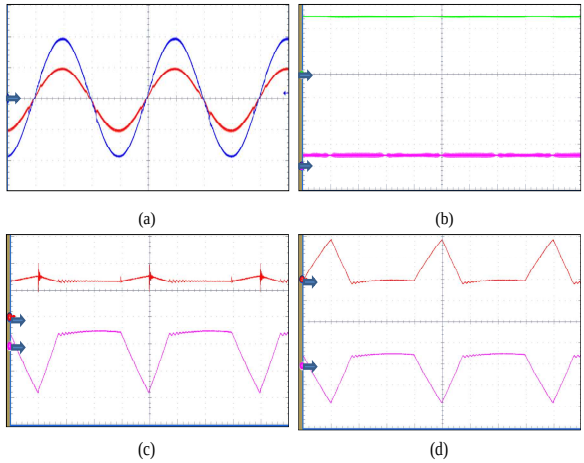

Fig. 9. Experimental results for the proposed rectifier: (a) Input current (3A/div.), input voltage (50V/div) over line cycle (time scale: 5ms/div.), (b) Output voltage (100V/div), output current (1A/div) over line cycle (time scale: 5ms/div), (c) I_{L1} (2A/div) and I_{Lo2} (5A/div) over switching cycle (time scale: 5µs/div), (d) I_{Lo1} and I_{Lo2} (5A/div) over switching cycle (time scale: 5µs/div).

Table II. – Comparison between conventional and bridgeless Cuk rectifier in DCM mode

	Conventional Cuk	Proposed Cuk Rectifier
Diodes	4 slow and 1 fast	2 fast
Switch	1	2
Current conduction path in stage 1	2 slow diodes and 1 switch	1 body diode and 1 switch
Current conduction path in stage 2	3 diodes(2 slow and 1 fast)	1 fast diode
Current conduction path in stage 3	2 slow diodes	----------
# of components	10	11
Integrated magnetic	One core for 2 inductors	One core for 3 inductors
Deriver circuit complexity	1 non-floating	1 floating and 1 non-floating
Ground	Non-floating	Floating

6. Conclusion

A bridgeless Cuk rectifier operating in DICM has been introduced. The Cuk rectifier has lower number of silicon components in the current path versus the conventional full bridge Cuk rectifier; hence higher efficiency is possible. The capability of this topology is verified via simulation and experimental results. Converter efficiency of 94% is achieved at low input voltage of 100 V_{rms}. Simulation and experimental results are shown and they corroborate theoretical analysis. The proposed circuit meets IEC-1000-3-2 requirements. The proposed rectifier at 125W and full load has THD of 0.17%.

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