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# Reduction of Zero Sequence Components in Three-Phase Transformerless Multiterminal DC-link based on Voltage Source Converters

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**Abstract.** This paper is focused on the analysis and reduction of zero sequence currents which appear in multiterminal DC-links based on Voltage Source Converters (VSCs). A zero sequence current may flow between the VSCs due to the absence of the coupling transformer, in spite of this application is intended for three-phase three-wire system. The proposed solutions to mitigate this issue have been tested through simulation and experimental results.

## Key words
Distribution networks, multiterminal DC-links, Voltage Source Converters (VSCs), Pulse Width modulation (PWM), Zero Sequence Harmonics.

## 1. Introduction

The traditional operation and design of Medium Voltage (MV) distribution networks has been performed using a radial scheme where the power flows from MV substation to the loads. Nowadays these networks are changing due to increasing load levels, a deep penetration of distributed generation (DG), monitoring, automation and introduction of new technologies leading to a new operation of these systems. In this actual context the main objective is to perform an optimal operation of the MV distribution networks. A possible solution is to mesh the radial feeders using a power electronic based DC-link to regulate the power flow flexibly between the feeders [1].

This DC-link can be composed of several Voltage Source Converters (VSCs) sharing a common DC bus as shown in Fig. 1. Usually the AC side of each VSC is connected through a transformer to the distribution network because of the low voltage level of the power electronics components. In recent years, however, this restriction is being solved technologically by increasing the reverse blocking capability of the semiconductors and the development of multilevel topologies [2]. For this reason, it is possible to think about using transformerless VSCs directly connected to the distribution network as shown Fig. 1 [3].

The transformerless topology reduces the total losses, cost and size of the multiterminal DC-link. However, it has to be considered that the power quality can be deteriorated due to the uncontrolled flow of zero sequence currents between VSCs. These current components can be caused by a DC voltage difference in each VSC (voltage drops occur in the DC-link), different PWM control strategies and unequal switching frequencies [4].

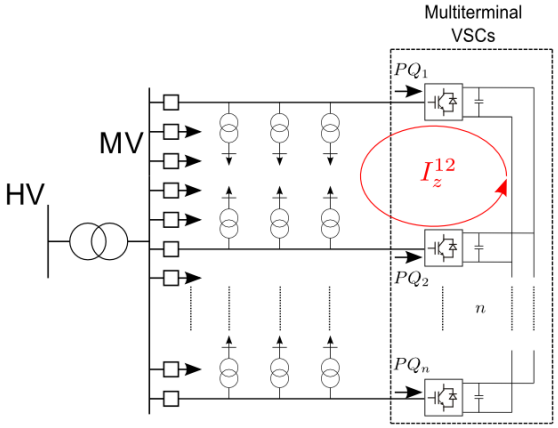

Fig. 1. Multiterminal transformerless DC-link.

The aim of this work is to analyze the causes motivating the zero sequence harmonic flow between transformerless multiterminal VSCs sharing a common DC bus. Once the cause of this power flow has been detected, a control strategy to reduce these components is proposed. The paper supports this proposal including simulation and experimental results.

## 2. Zero sequence harmonics

Three-phase three-wire VSC is a well-known device used in numerous applications. This device uses self-commuted IGBT modules which are operated using a modulation strategy. Pulse width modulation (PWM) technique is a classical algorithm which consists on comparing two signals. The modulating or control signal is compared with a higher frequency wave named carrier. The result of this comparison leads to a train of pulses which faithfully represents the modulating information and inherited unwanted harmonics. DC component and baseband harmonics appear close to the fundamental frequency of which the third harmonics is the most

representative. In addition, sideband harmonics appears around the carrier frequency being the two adjacent harmonics the most representative ones [5].

PWM techniques offer a wide range of different possibilities to manage both the carrier and the modulating waveforms which give rise to different spectrum harmonics. Among them, asymmetrical regular sampled PWM has been used in this work. Asymmetrical regular sampled PWM requires that the ratio of frequencies between the modulating and triangular carrier waveform has to be an even number.

Zero sequence VSC voltages are mainly composed by three harmonic components: DC, third and switching harmonics (corresponding to the frequency of the triangular carrier signal). This last component appears as usually the same triangular carrier signal is used for the three phases. The zero sequence voltage of the *j-th* VSC can be formulated as:

$$v_z^j(t) = V_0^j + \sqrt{2}V_3^j \cos(\omega_3 t + \alpha_j) + \sqrt{2}V_{sw}^j \cos(\omega_{sw}^j t + \beta_{j,sw}) \quad (1)$$

Note that the transformerless configuration shown in Fig. 1 is characterized by a common DC bus which allows the circulation of the zero sequence currents. Therefore, a zero sequence current flow may be generated if the zero sequence voltages of each VSC, detailed in (1), are not exactly the same. In this sense, it is possible to assume the following classification in order to justify the differences between the VSC zero sequence voltages and, consequently, the zero sequence current flow:

- DC voltage. The DC bus is composed of different paralleled VSC capacitors with unequal voltage due to the voltage drop caused by the active power flow between the VSCs. Note that the DC current is only limited by the resistive elements of the path shown in Fig. 1.

- Third and switching voltage harmonics. These harmonics are generated by the PWM technique and depend on the DC capacitor voltage, the carrier waveform (frequency and sequence) and the dead-time required to avoid short-circuits during the commutation of IGBTs. On the one hand, the third harmonic voltage has a reduced value from a theoretical point of view which can be higher in practice due to the required dead-time. On the other hand, the switching harmonic voltage presents always a high value which mainly depends on the modulation index. However, the currents related to both harmonic components can be extraordinarily high depending on the voltage phase difference and the harmonic impedance of the electrical circuit.

The following section is devoted to analyze the alternatives to reduce the zero sequence current due to the zero sequence voltages between the DC-link VSCs.

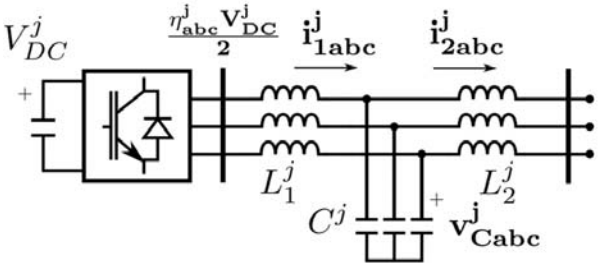


Fig. 2. Three-phase electrical circuit of a VSC with a LCL coupling filter.

## 3. Reduction of zero sequence current harmonics

A control strategy including not only positive and negative but also zero sequence components is proposed to reduce the zero sequence current flow. This control algorithm is combined with a modulation scheme which reduces the zero sequence components around the switching frequency.

A traditional modelling approach for VSCs in *abc* and *zdq* coordinates has been considered to develop the control strategy to reduce the low order harmonics, Fig. 1 shows *n* VSCs sharing a common DC bus and connected to the same substation. For the sake of simplicity, the analysis will be applied to a pair of VSCs. The dynamic equations using the *abc* frame of each VSC, as shown in Fig. 2, can be formulated as:

$$\frac{d}{dt}\begin{pmatrix} L_1^j \mathbf{i}_{1abc}^j \\ L_2^j \mathbf{i}_{2abc}^j \\ C^j \mathbf{v}_{Cabc}^j \end{pmatrix} = \begin{pmatrix} \boldsymbol{\eta}_{abc}^j V_{DC}^j / 2 - R_1^j \mathbf{i}_{1abc}^j - \mathbf{v}_{Cabc}^j \\ \mathbf{v}_{Cabc}^j - R_2^j \mathbf{i}_{2abc}^j - \mathbf{v}_{abc}^j \\ \mathbf{i}_{1abc}^j - \mathbf{i}_{2abc}^j \end{pmatrix} \quad (2)$$

where $\boldsymbol{\eta}_{abc}$ corresponds to the duty cycles of each pair of IGBTs. The use of control algorithms designed for tracking sinusoidal magnitudes is not straightforward because constant values are preferred in steady state. As a consequence, the transformation of the proposed model in *abc* coordinates to the classical *zdq* axis is applied to (2) leading to the following expression:

$$\left(L_1^j + L_2^j\right)\frac{d\mathbf{i}_{zdq}^j}{dt} = \frac{\boldsymbol{\eta}_{zdq}^j V_{DC}^j}{2} - \mathbf{M}^j \mathbf{i}_{zdq}^j - \mathbf{v}_{zdq}^j \quad (3)$$

Note that the dynamic of the filter capacitor has been eliminated as its influence at low frequencies is reduced. The following matrix has been introduced in order to obtain a compact formulation of the dynamic equations:

$$\mathbf{M}^j = \begin{pmatrix} R_1^j + R_2^j & 0 & 0 \\ 0 & R_1^j + R_2^j & \omega\left(L_1^j + L_2^j\right) \\ 0 & -\omega\left(L_1^j + L_2^j\right) & R_1^j + R_2^j \end{pmatrix} \quad (4)$$

The currents and voltages in *z* axis will be null in a three-phase three-wire isolated DC bus system. However, zero sequence currents appear in the proposed scheme as the

VSCs share a common DC bus. The control strategy for positive sequence, *dq* frame, has been designed using a PI controller [6]. Similar control strategy can be considered for zero sequence using the equation in *z* coordinates from (3):

$$\left(L_1^j + L_2^j\right)\frac{di_z^j}{dt} = \frac{\eta_z^j V_{DC}^j}{2} - \left(R_1^j + R_2^j\right)i_z^j - v_z^j \qquad (5)$$

A brief representation of the proposed *zdq* control algorithm is shown in Fig. 3. The active and reactive power references determine the *dq* currents while the *z* current reference is set to zero.

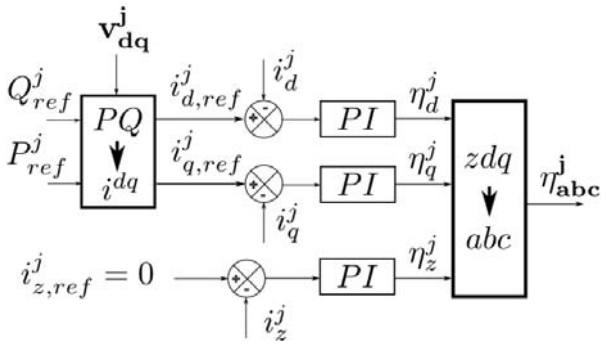


Fig. 3. Proposed *zdq* current control algorithm.

However, the reduction of the zero sequence current corresponding to the switching frequency cannot be achieved using this strategy. The main reason is that the bandwidth of any control algorithm is lower than the VSC switching frequency. Two possible strategies can be implemented in order to overcome this shortcoming:

- Modification of the carrier signals. As previously mentioned, usually the same carrier signal is used for the three phases of the VSC. As a result, a zero sequence voltage appears in the switching frequency while positive and negative sequences are related to the sideband harmonics. A brief summary of how the sequence of the triangular carrier affects the sequence of the voltage harmonics around the switching frequency is shown in Table 1. Other possibility is to use a staggered PWM strategy which consists on generating the carrier signals with a phase shift of 120 degrees (positive sequence). In this case, a positive sequence voltage appears in the switching frequency while the sideband harmonics are negative and zero sequence components. Therefore, the voltage harmonics corresponding to the switching frequency could be eliminated using a suitable LCL coupling filter. However, this strategy presents two shortcomings. On the one hand, the capacitor of the LCL filter has to be oversized as the harmonic voltage magnitude corresponding to the switching frequency is high compared to these of the side band harmonics, as can be seen in Fig. 4. On the other hand, the zero sequence current is not completely eliminated as the sideband harmonics are non-negligible as shown in Fig. 4.

Table I. Relationships between the sequence of the carrier signal and the sequence of the harmonics around the switching frequency.

| Triangular carrier sequence | Sideband $f_{sw-2}$ | Carrier $f_{sw}$ | Sideband $f_{sw+2}$ |
|---|---|---|---|
| Zero | Positive | Zero | Negative |
| Positive | Negative | Positive | Zero |
| Negative | Zero | Negative | Positive |

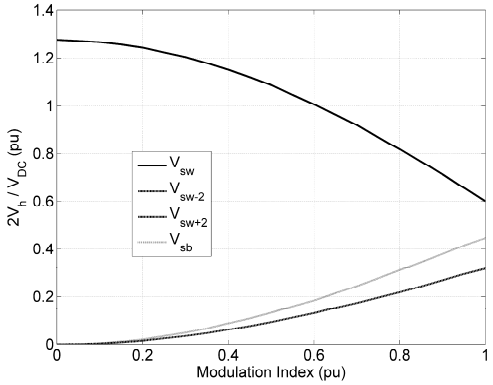


Fig. 4. Carrier and sideband harmonics as a function of the modulation index.

- Synchronization of the carrier signals. This strategy is based on using a synchronized carrier signal for all the VSCs. As a result, the phase of the zero sequence voltage switching harmonic is almost the same for all the VSCs. Therefore, the zero sequence current flow is considerably reduced as the phase difference between the zero sequence voltages is negligible. In addition, the cost of the coupling LCL filter gets reduced.

This paper proposes to use this second option as the zero sequence current flow can be limited effectively without oversizing the LCL coupling filter.

## 4. Simulation Results

In this section two VSCs connected to the same point of common coupling (PCC) and sharing a common DC bus has been analyzed. The rated characteristics of the VSCs considered in the simulations are shown in Table II. The simulation includes a small resistance between both DC capacitors in order to simulate a reduced voltage drop.

Table II. Rated characteristics of the VSCs.

| $S_{rat}$ (kVA) | $V_{dc}$ (V) | $V_{PCC}$ (V) | $f_{sw}$ (kHz) | $L_1$ (mH) | $L_2$ (mH) | $C$ (μF) |
|---|---|---|---|---|---|---|
| 100 | 800 | 400 | 5 | 5 | 5 | 30 |

Three cases have been simulated in order to evaluate the benefits of using the proposed approach to reduce the zero sequence current flow:

- Case 1: the system has been simulated using a conventional *dq* current control algorithm with unsynchronized PWM. The results of this simulation are shown in Fig. 5.(a) where the VSC phase currents and the related zero sequence current have been detailed. This figure shows an

important high frequency ripple on the phase currents corresponding to a zero sequence component and a non-negligible DC component.

- Case 2: the system has been simulated using a conventional *dq* current control algorithm with synchronized PWM. The results are shown in Fig. 5.(b) where it is possible observe the reduction on the high frequency ripple. However, an important DC term in the zero sequence current still remains.
- Case 3: the system has been simulated using the proposed z*dq* current control algorithm with synchronized PWM. In this case, the DC current is completely eliminated and the high frequency ripple is also lower due to the synchronized PWM implementation.

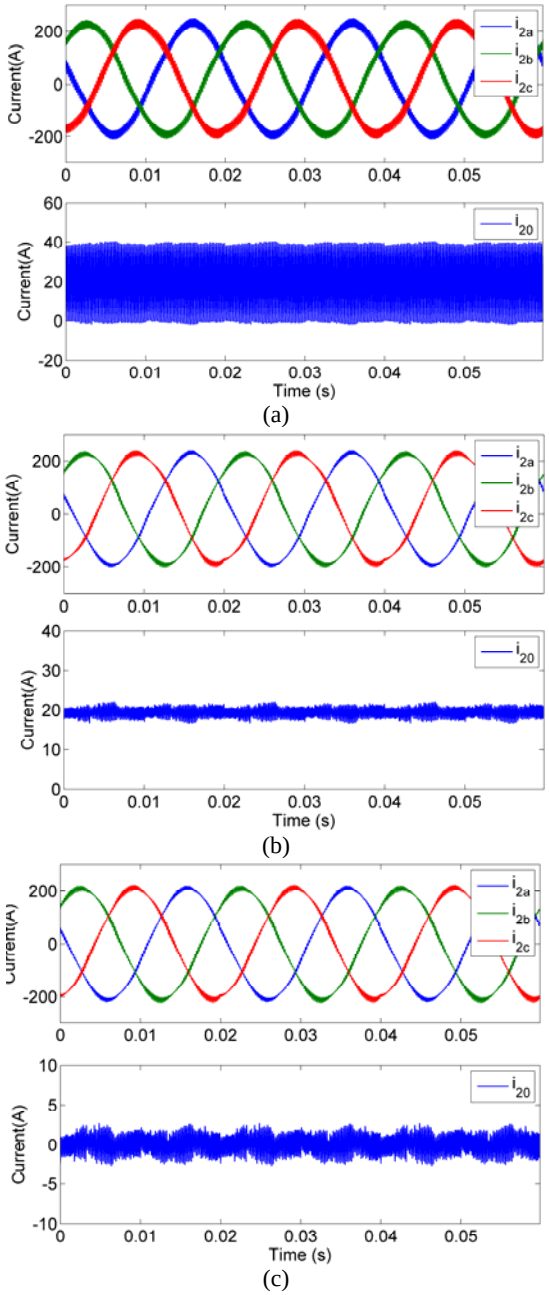


Fig. 5. Simulated results. Phase currents in the time domain. (a) Conventional *dq* control algorithm without PWM synchronization. (b) Conventional *dq* control algorithm with PWM synchronization (c) Proposed z*dq* control algorithm with PWM synchronization.

These qualitative conclusions can be also stated in case of analysing the harmonic spectrum of the VSC currents which is shown in Fig. 6. Note that two harmonic ranges have been detailed in order to clearly asses the influence of the proposed strategies. Fig 6.(a) shows the presence of a DC current, low order, switching and sideband harmonics. Due to the PWM synchronization the switching harmonic has been reduced from 10% to less than 1% as shown in Fig. 6.(b). The implementation of the *zdq* control algorithm considerable reduces the DC and low order harmonic currents as shown in Fig. 6.(c). However, it is worth noting that the sideband harmonics around switching frequency remain almost constant because these components cannot be reduced using either the *zdq* current control algorithm or the synchronization. The magnitude of these harmonic components is exclusively related to the efficiency of the LCL coupling filter.

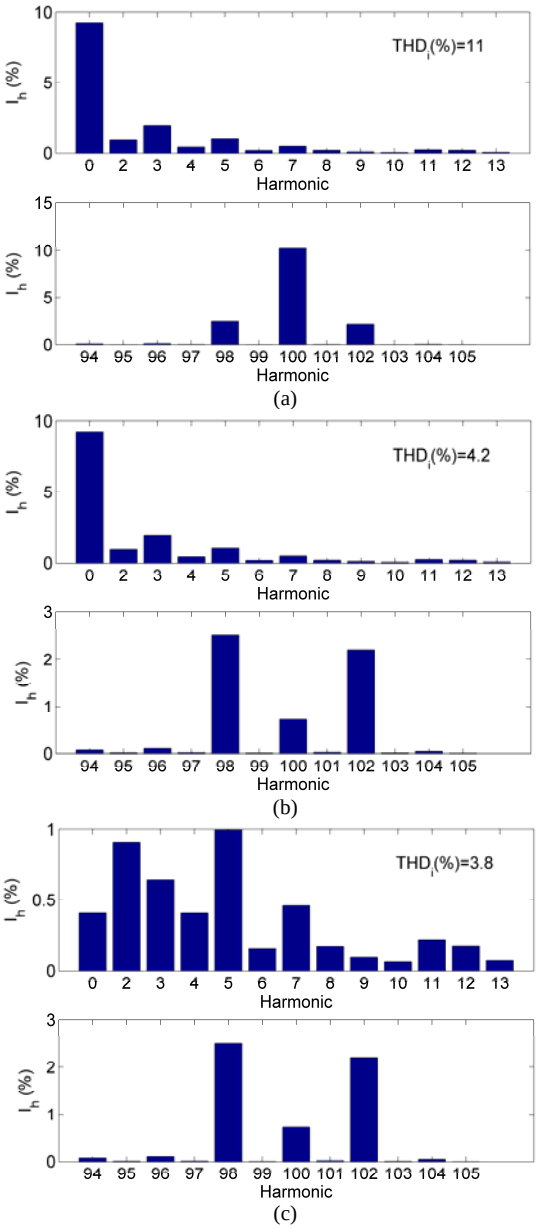


Fig. 6. Simulated results. Frequency spectrum of the VSC phase current. (a) Conventional *dq* control algorithm without PWM synchronization. (b) Conventional *dq* control algorithm with PWM synchronization (c) Proposed z*dq* control algorithm with PWM synchronization.

The value of the THD and zero sequence components of the different simulations are summarized in Table III.

Table III. Performance of the control schemes using simulated results.

| Control algorithm | PWM | *THD* (%) | $I_z^{dc}$ (%) | $I_z^3$ (%) | $I_z^{sw}$ (%) |
|---|---|---|---|---|---|
| *dq* | No synchro. | 11.0 | 9.3 | 1.9 | 10.2 |
| *dq* | Synchro. | 4.2 | 9.3 | 1.9 | 0.7 |
| *zdq* | Synchro. | 3.8 | 0.4 | 0.6 | 0.7 |

## 5. Experimental Results

This section presents experimental results comparing the previously analyzed control strategies. The experimental setup is composed by two 100 kVA VSCs with the rated characteristics shown in Table II. The control of these power electronic VSCs have been implemented on a real-time RT-LAB platform developed by Opal-RT Technologies.

Fig. 7. Experimental setup.

The control algorithms previously analyzed have been tested in the laboratory with similar results than those of the simulations. Fig. 8 details the phase currents and the zero sequence current for these algorithms. Fig. 8.(a) shows a higly distorted phase current with DC, third and switching harmonics. It is worth noting that the third harmonic content is higher than the predicted by the simulations. Probably the erorr related to the voltage transducer which measures the voltage at the point of common coupling is the cause of this behaviour. The zero sequence current flow between VSCs, as previously analyzed, is due to a difference in the VSC zero sequence voltages. Therefore, in spite that both VSCs are coupled to the same point, any small error on the voltage measurement may motivate this third harmonic current flow. Fig. 8.(b) clearly reveals the drastic reduction of the zero sequence switching frequency using the synchronization, however, the low order harmonics are quite large. Fig. 8.(c) shows an almost sinusodial current injection. Note that the ripple of this current is even better than the simulated one. The reason is that the simulations do not include the network impedance at the point of common coupling.

Fig. 9 details the harmonic spectra of the phase currents for the implemented control algorithms. The analysis of the VSC current harmonics currents support from a quantitative point of view the previous comments done using the time domain magnitudes.

The performance of the control algorithms in the experimental implementation has been included in Table IV.

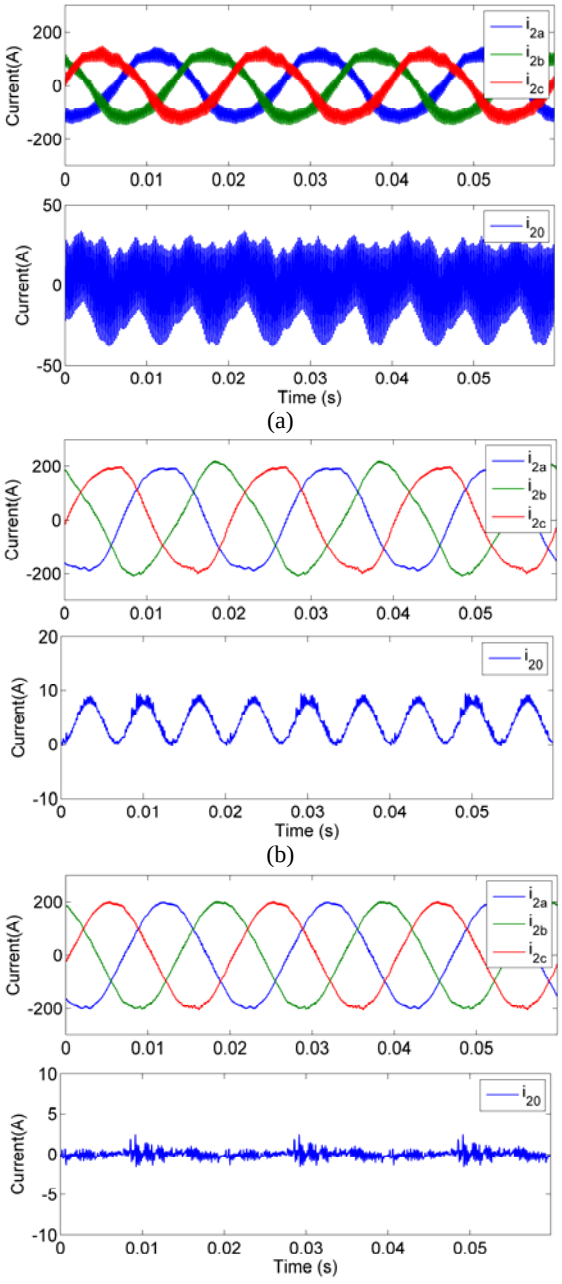


Fig. 8. Experimental results. Phase currents in the time domain. (a) Conventional *dq* control algorithm without PWM synchronization. (b) Conventional *dq* control algorithm with PWM synchronization (c) Proposed z*dq* control algorithm with PWM synchronization.

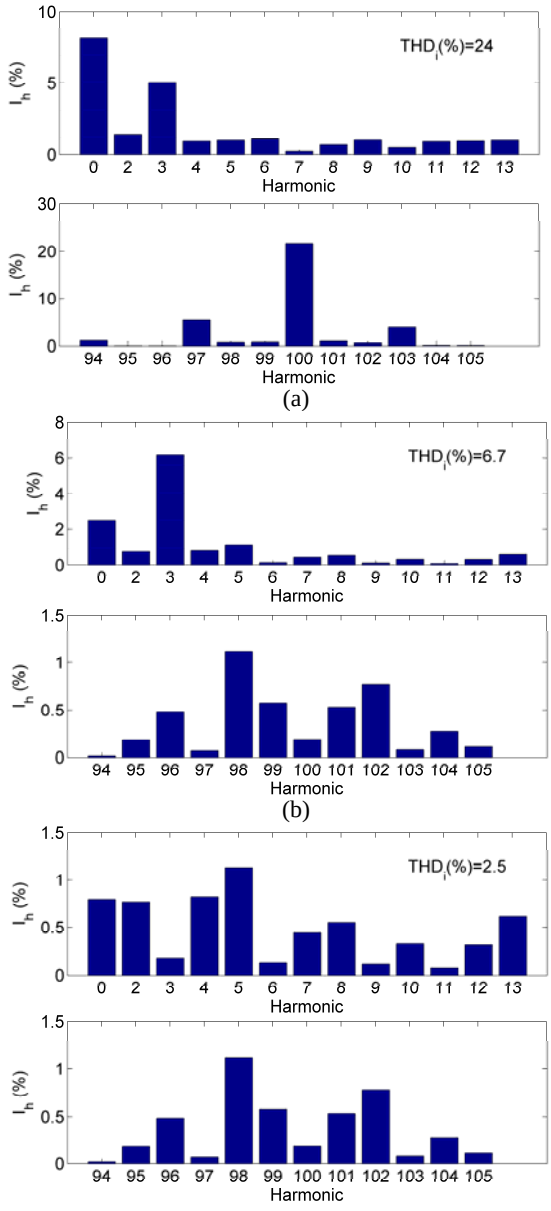


Fig. 9. Experimental results. Frequency spectrum of the VSC phase current. (a) Conventional *dq* control algorithm without PWM synchronization. (b) Conventional *dq* control algorithm with PWM synchronization (c) Proposed z*dq* control algorithm with PWM synchronization.

Table IV. Performance of the control schemes using experimental results.

| Control algorithm | PWM | *THD* (%) | $I_z^{dc}$ (%) | $I_z^3$ (%) | $I_z^{sw}$ (%) |
|---|---|---|---|---|---|
| *dq* | No synchro. | 24 | 8.3 | 5.1 | 21.8 |
| *dq* | Synchro. | 6.7 | 2.5 | 6.2 | 0.2 |
| *zdq* | Synchro. | 2.5 | 0.8 | 0.2 | 0.2 |

## 6. Conclusions

This paper has presented the problems that may arise in multiterminal DC-links based on transformerless VSCs. In this topology conventional *dq* control algorithms intended for three-phase three-wire applications and independent PWM strategies for each VSC without any synchronization lead to an uncontrolled and non-negligible zero sequence current flowing between the VSCs. This paper has proposed a control strategy based on a *zdq* control algorithm which effectively reduces the zero sequence low order harmonics. In addition, a synchronized PWM scheme is recommended to reduce the zero sequence content of the switching harmonics. The proposal has been supported through simulation and experimental results.

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