



Advanced PLL structures for grid synchronization in distributed generation

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Abstract— The actual grid code requirements include specific demands for grid connected wind power generation facilities. The Transmission System Operators are specially concerned about the Low Voltage Ride Through requirements which are becoming more restrictive in terms of the admissible disconnection conditions, but also in the active/reactive power that wind farms should inject to the network under fault conditions to support the grid. Solutions based on the installation of STATCOMs and DVRs, as well as on advanced control functionalities for the existing power converters of wind power plants, have contributed to enhance their response under faulty and distorted scenarios, and hence to fulfill these requirements. However, in order to achieve satisfactory results with such systems it is necessary to count on accurate and fast grid voltage synchronization algorithms, able to work under unbalanced and distorted conditions. This paper analyzes the synchronization capability of three advanced synchronization systems: the DDSRF-PLL, the DSOGI-PLL and the 3phEPLL, designed to work under such conditions. In the following the different algorithms will be presented and discretized and finally their performance, as well as its computational cost, will be tested in an experimental setup controlled by a means of a TMS28335 floating point DSP.

Index Terms — Frequency estimation, Synchronization, Frequency locked loops, Harmonic analysis, Monitoring, Electrical Engineering, Electric variables measurements.

I. INTRODUCTION

AT the present time wind power systems provide between the 5% - 5.2% of the total EU electricity demand and is expected to grow up to the 20% - 28% by the end of 2030 [1]. The increasing penetration of this technology in the electrical network has reinforced the already existing concern about their influence in the grid stability among the transmission system operators (TSO), as a consequence, the grid connection standards are becoming more restrictive for wind power plants worldwide [2]-[6].

In the actual grid codes requirements (GCR) special constrains for the operation of wind power plants under grid

voltage fault conditions, have gained a great importance. These requirements determine the fault boundaries among the ones a grid connected wind turbine shall remain connected to the network, giving rise to specific voltage profiles that specify the depth and clearance time of the voltage sags that wind turbines must withstand without tripping. Such requirements are known as Fault Ride Through (FRT) or Low Voltage Ride Through (LVRT) and they are described by a voltage vs time characteristic, denoting the minimum required immunity of the wind power station [7].

Although the LVRT requirements in the different standards can be very different, as shown in [8], the first issue that wind power systems must afford when a voltage sag occurs is the limitation of their transient response, in order to avoid its protective disconnection from the network. This is the case, for instance, of fixed speed WTs based on squirrel cage induction generators (SCIG), where the voltage drop in the stator windings can conduct the generator to an overspeed tripping, as shown in [9]. Likewise, variable speed WTs based on doubly fed induction generators (DFIG) may loose the controllability in the injection of active/reactive power due to the disconnection of the rotor side converter under such conditions [10]-[11].

Solutions based on the development of auxiliary systems such as STATCOMs and DVRs have played a decisive role for enhancing the FRT capability of SCIGs WTs, as demonstrated in [12]-[16]. Likewise, advanced control functionalities for the power converters of wind power facilities have been also proposed for reducing overcurrents in DFIGs under these conditions in [10]-[11] and [17]-[18]. In any case a fast detection of the fault contributes to improve the effects of these solutions, and as a consequence the FRT capability of the system.

In certain countries the TSO provide also the active/reactive power pattern to be injected to the network during a voltage sag, this is the case of the German e-on [2] and the Spanish REE [3]. This trend has being followed by the rest of the TSOs, moreover, it is believed that this operation requirement will be extended and specific demands for balanced and

unbalanced sags will arise in the following versions of the grid codes worldwide [19].

Regarding the operation of the WT under balanced and unbalanced fault conditions relevant contributions, such as [20]-[29] can be also found in the bibliography. However, these solutions are based on advanced control systems that need to have an accurate information of the grid voltage variables in order to work properly, something that has launched the importance of grid synchronization algorithms in these applications.

Phase-locked technology has been broadly used in communications, aerospace and consumer electronics systems where a local oscillator is synchronized with some external signal. In power systems, the Synchronous Reference Frame PLL (SRF-PLL) is the most extended technique for synchronizing with three-phase systems [30]. Nevertheless, and despite the fact that the performance of SRF-PLL is satisfactory under balanced conditions, its response can be inadequate under unbalanced, faulty or distorted conditions [31]-[33].

In this paper three advanced grid synchronization systems: the Decoupled Double synchronous reference frame PLL (DDSRF PLL) [34], the Dual SOGI PLL (DSOGI PLL) [35] and the Three Phase Enhanced PLL (3phEPLL PLL) [36] will be studied. The analysis will evaluate their performance and reliability on the amplitude and phase detection of the positive sequence of the voltage, under unbalanced and distorted situations, that, in order to reach a more realistic approach, have been implemented according to experimental grid fault patterns extracted from [37]-[38].

In the following sections the discrete representation of each PLL will be detailed (§IV), after a brief description of the different structures (§III). Next their behavior will be tested in an experimental setup (§VI), and their performance will be discussed, taking specially into account the accuracy in the positive sequence detection and their computational cost (§VII).

II. DESCRIPTION OF THE THREE SYNCHRONIZATION SYSTEMS

Many of the positive sequence detection algorithms are based on synchronous reference frame PLL's (SRF PLL) [32]. Despite having a good response under balanced conditions, their performance become insufficient in unbalanced faulty grids (95% of cases) and their good operation is highly conditioned to the frequency stability, something incompatible with the idea of a robust synchronization system. Many authors have been discussing about different advanced models, able to overcome the problems of the classical PLL, by means of building frequency, and amplitude adaptive structures, able to deal with unbalanced, faulty and harmonic polluted grids. In the framework of these topologies we could find the three PLLs discussed in this paper.

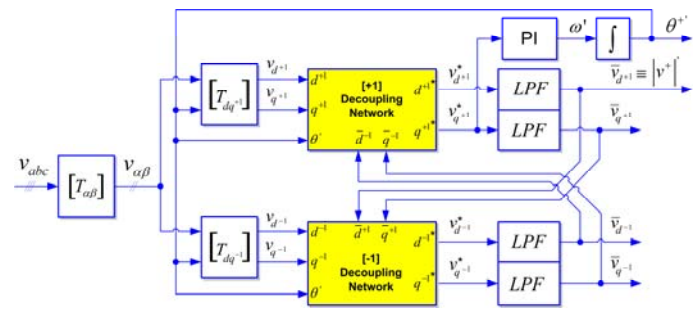


Fig. 1. DDSRF PLL block diagram

A. Decoupled Double synchronous reference frame PLL (DDSRF PLL)

The DDSRF-PLL, published in [34], [41], stems from improving the conventional SRF-PLL. This synchronization system exploits two synchronous reference frames rotating at the fundamental utility frequency, one counter-clockwise and another one clockwise, in order to achieve an accurate detection of the positive and negative sequence components of the grid voltage vector when it is affected by unbalanced grid faults. The diagram of the DDSRF-PLL is shown in Fig.1.

When the three-phase grid voltage is unbalanced, the fundamental positive-sequence voltage vector appears as a DC voltage on the dq^{+1} axes of the positive-sequence SRF and as ac voltages at twice the fundamental utility frequency on the dq^{-1} axes of the negative-sequence SRF. On the contrary, the negative-sequence voltage vector will cause a dc component on the negative-sequence SRF and an ac oscillation on the positive-sequence SRF. Since the amplitude of the oscillation on the positive-sequence SRF matches to the DC level on the negative-sequence SRF, and vice versa, a decoupling network is applied to signals on the dq positive/negative SRF axes in order to cancel out such ac oscillations. Low-pass filters in Fig.1 are in charge of extracting the DC component from the signal on the decoupled SRFs axes. These DC components collect the information about the amplitude and phase-angle of the positive- and negative-sequence components of the grid voltage vector.

The loop controller of the DDSRF-PLL works on the decoupled q -axis signal of the positive-sequence SRF ($v_{q^{+1}}^*$). This signal is free of ac components due to the effect of the decoupling cells and the bandwidth of the loop controller can be consequently increased.

B. Dual SOGI PLL (DSOGI PLL)

The operating principle of the DSOGI-PLL for estimating the positive and negative-sequence components of the grid voltage vectors is based on using the instantaneous symmetrical components (ISC) method on the $\alpha\beta$ stationary reference frame, as explained in [35]. The diagram of the DSOGI-PLL is shown in Fig.4. As it can be noticed in this figure, the ISC method is implemented by the positive sequence calculation block (PSC).

To apply the ISC method, it is necessary to have a set of signals $v_\alpha - v_\beta$ representing the input voltage vector on the $\alpha\beta$ stationary reference frame together with another set of signals $qv_\alpha - qv_\beta$ which are in-quadrature and lagged respect to $v_\alpha - v_\beta$. In the DSOGI-PLL, these signals to be supplied to the ISC method are obtained by using a dual second order generalized integrator (DSOGI) which is an adaptive band pass filter based on the generalized integrator concept [42]. The DSOGI provides at its output four signals, namely, v'_α and v'_β which are filtered versions of v_α and v_β , respectively, and qv'_α and qv'_β which are the in-quadrature versions of v'_α and v'_β .

A conventional synchronous reference frame phase-locked loop (SRF-PLL) is applied on the estimated positive-sequence voltage vector, $v_{\alpha\beta}^+$, to make this synchronization system frequency adaptive. In particular, the $v_{\alpha\beta}^+$ voltage vector is translated to the rotating SRF and the signal on the q axis, v_q^+ , is applied at the input of the loop controller. As a consequence, the fundamental grid frequency (ω) and the phase-angle of the positive-sequence voltage vector (θ^{+}) are estimated by this loop. The estimated frequency for the fundamental grid component is feedback to adapt the center frequency of the DSOGI.

C. Three phase enhanced PLL (3phEPLL PLL)

The enhanced phase locked loop (EPLL) is a synchronization system that had proven to perform good results in one-phase synchronization systems [43]. An EPLL is essentially an adaptive bandpass filter, able to adjust the cutoff frequency in function of the input signal. Its structure was later adapted for the three phase case [44], in order to detect the positive sequence vector of a three phase signals, obtaining the 3phEPLL PLL that is represented in Fig.3.

In this case, each input phase voltage is being processed independently by an EPLL. This block filters the input signal and generates two sinusoidal outputs of the same amplitude and frequency, v'_n and jv'_n , being the second one 90° leaded with respect v'_n . The resulting signals constitute the input for the computational unit. This block implements the ISC method on the 'abc' stationary reference frame for extracting the positive-sequence voltage component, v_{abc}^+ .

III. DISCRETE IMPLEMENTATION

The reliability of a discretized system depends upon the approximation made to their continuous equations [45]. Some methods, as the Forward Euler, the Backward Euler and the Tustin (Trapezoidal) numerical integration offer a good performance when used for discretizing other synchronization systems, as shown in [46]-[47], however the Euler methods

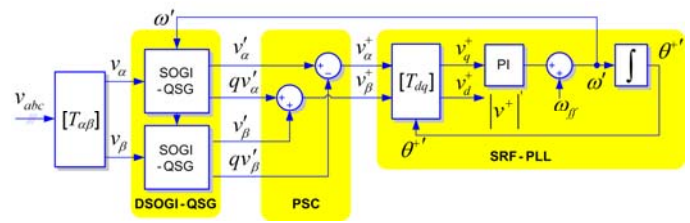


Fig. 2. DSOGI PLL block diagram

can be inadequate under certain conditions, due to the need of introducing additional sample delays [48]. Therefore, and according to the specific needs of the presented topologies, in this section the discrete representation of each PLL will be described independently. In order to facilitate the comprehension of the process the different building blocks that appear at Fig.1, Fig.2 and Fig.3 will be referenced. The values of the different parameters used in each case are summarized in an appendix at the end of this paper.

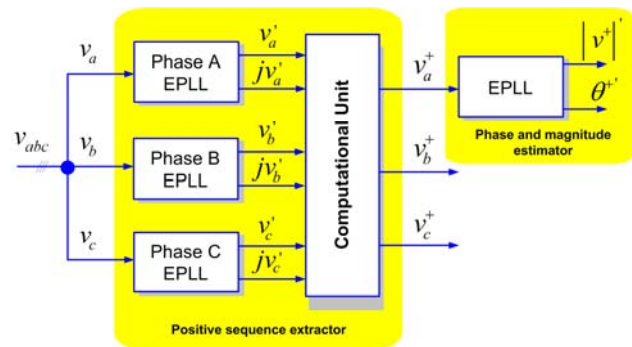


Fig. 3. 3ph EPLL PLL block diagram

A. DDSRF PLL discretization

The discrete model of this PLL can be easily obtained, since the continuous representation of several parts does not change in the discrete domain. This is obviously the case of the transformation blocks: $T_{\alpha\beta}$, $T_{dq^{+1}}$ and $T_{dq^{-1}}$, whose description can be found in previous papers and general scope bibliography [49].

1. Positive and negative sequence decoupling networks

The decoupling network constitutes one of the most important contributions of this synchronization tool. The discrete equations of these blocks are shown in (1), being almost the same as in the continuous domain [41]. It is just necessary to consider the one sample delay of θ^+ , $\bar{v}_{d^{-1}}$, $\bar{v}_{q^{-1}}$, $\bar{v}_{d^{+1}}$ and $\bar{v}_{q^{+1}}$ in order to avoid algebraic loops.

2. Phase and magnitude estimator discretization

In the DDSRF-PLL the decoupling network appears embedded in the classical SRF-PLL loop (Fig.4). However this does not affect the discretization of the phase and magnitude estimator, since v_{d+1}^* and v_{q+1}^* act as the input of this block.

$$\begin{aligned} \begin{bmatrix} v_{d+1}^*[n+1] \\ v_{q+1}^*[n+1] \end{bmatrix} &= \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d+1}^*[n] \\ v_{q+1}^*[n] \end{bmatrix} \\ &+ \begin{bmatrix} -\cos(2\theta'[n]) & -\sin(2\theta'[n]) \\ \sin(2\theta'[n]) & -\cos(2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d-1}[n] \\ \bar{v}_{q-1}[n] \end{bmatrix} \\ \begin{bmatrix} v_{d-1}^*[n+1] \\ v_{q-1}^*[n+1] \end{bmatrix} &= \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d-1}^*[n] \\ v_{q-1}^*[n] \end{bmatrix} \\ &+ \begin{bmatrix} -\cos(-2\theta'[n]) & -\sin(-2\theta'[n]) \\ \sin(-2\theta'[n]) & -\cos(-2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d+1}[n] \\ \bar{v}_{q+1}[n] \end{bmatrix} \end{aligned} \quad (1)$$

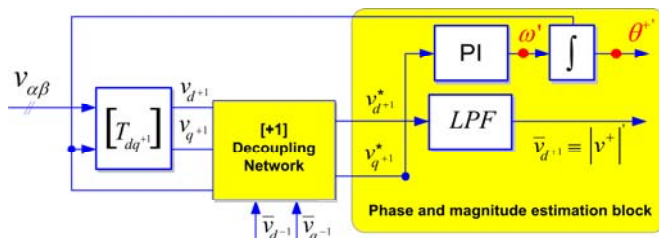


Fig. 4. Phase and magnitude estimation loop of the DDSRF PLL

The discrete controller and the integrator can be build using a backward numerical approximation. The frequency and phase can be then represented in the z-domain (2) considering v_{q+1}^* as the error to be minimized. In this equation a feedforward of the nominal frequency is given by means of ω_{ff} .

$$\begin{aligned} W'(z) &= \frac{(k_p + k_i \cdot T_s)z - k_p}{z - 1} \cdot V_{q+1}^*(z) + \omega_{ff} \\ \theta^+ &= \frac{T_s \cdot z}{z - 1} \cdot W'(z) \end{aligned} \quad (2)$$

A sampled based representation delivers finally, (3) which are the expressions to be programmed.

$$\begin{aligned} \omega'[n+1] &= \omega'[n] - k_p \cdot v_{q+1}^*[n] + (k_p + k_i \cdot T_s) \cdot v_{q+1}^*[n+1] \\ \theta^+[n+1] &= \theta^+[n] + T_s \cdot \omega'[n+1] \end{aligned} \quad (3)$$

In these equations a frequency feedforward has been included by introducing a initial condition to w' .

3. Lowpass filter block discretization

The amplitude of the dq positive and negative sequence components are the outputs of the decoupling networks. However, four IIR low pass filters extract the ripple from each sequence estimation, in order to reinforce the performance of the PLL in case of harmonic pollution. A first order filter with a cutoff frequency, ω_f , equal to the half of the grid one was originally proposed in [41], hence the same transfer function has been implemented in this work for evaluation purposes in (4).

$$\begin{aligned} y[n] &= \frac{1}{T_s \cdot \omega_f + 1} \cdot x[n] + \frac{T_s \cdot \omega_f}{T_s \cdot \omega_f + 1} \cdot u[n] \\ x[n+1] &= y[n] \end{aligned} \quad (4)$$

B. DSOGI PLL discretization

1. DSOGI-QSG block discretization

As it was previously mentioned in §II, the DSOGI based quadrature signal generator of Fig. 4 consist of two independent and decoupled SOGIs. Therefore each SOGI-based quadrature signal generator can be discretized individually, facilitating thus its mathematical description. In Fig.5 the block diagram of the SOGI implemented in this work is shown.

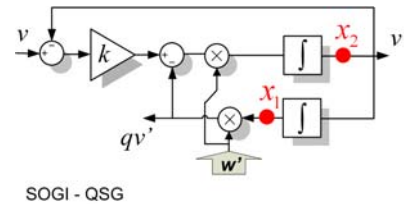


Fig.5. Quadrature signal generator based on a second order generalized integrator (SOGI-QSG)

This QSG is a linear system itself, therefore a discrete representation can be systematically obtained if the continuous state space is previously deduced. The equations of the SOGI state space appear detailed in (5) where v constitutes the input while v' and qv' are the two in-quadrature output signals.

$$\begin{aligned} \dot{x}_n &= A \cdot x_n + B \cdot v \\ y_n &= C \cdot x_n \end{aligned} \quad \left. \vphantom{\begin{aligned} \dot{x}_n &= A \cdot x_n + B \cdot v \\ y_n &= C \cdot x_n \end{aligned}} \right\}; \quad x_n = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \quad y_n = \begin{bmatrix} v' \\ qv' \end{bmatrix} \quad (5)$$

$$A = \begin{bmatrix} 0 & 1 \\ -\omega'^2 & -k \cdot \omega' \end{bmatrix} \quad B = \begin{bmatrix} 0 \\ k \cdot \omega' \end{bmatrix} \quad C = \begin{bmatrix} 0 & 1 \\ \omega' & 0 \end{bmatrix}$$

The discretization of this system has been performed using trapezoidal integrators, as they offer a better detection of the phase, something important when dealing with sinusoidal signals [22]. The symbolic values of each matrix of (7) are detailed in (6), where T_s is the sampling time of the discrete

$$\begin{aligned}
 A' &= \gamma \begin{bmatrix} 4 + 2T_s \cdot k \cdot \omega'[n] - T_s^2 \cdot \omega'[n]^2 & 4T_s \\ -4T_s \cdot \omega'[n]^2 & 4 - 2T_s \cdot k \cdot \omega'[n] - T_s^2 \cdot \omega'[n]^2 \end{bmatrix}; B' = \gamma \begin{bmatrix} 2T_s \cdot k \cdot \omega'[n] \\ 4k \cdot \omega'[n] \end{bmatrix} \\
 C' &= \gamma \begin{bmatrix} -2T_s^2 \cdot \omega'[n]^2 & 4T_s \\ 2T_s \cdot \omega'[n] \cdot (2 + T_s \cdot k \cdot \omega'[n]) & 2T_s^2 \cdot \omega'[n] \end{bmatrix}; D' = \gamma \begin{bmatrix} 2T_s \cdot k \cdot \omega'[n] \\ k \cdot T_s^2 \cdot \omega'[n]^2 \end{bmatrix} \\
 \gamma &= \frac{1}{4 + 2 \cdot T_s \cdot k \cdot \omega'[n] + T_s^2 \cdot \omega'[n]^2}
 \end{aligned} \tag{6}$$

system while the value of $\omega'[n]$ and the k constant come from the estimation made at the SRF-PLL block in each computation step, and the SOGI gain respectively [14].

$$\begin{aligned}
 x[n+1] &= A' \cdot x[n] + B' \cdot v[n] \\
 y[n] &= C' \cdot x[n] + D' \cdot v[n]
 \end{aligned} \tag{7}$$

The discrete state space of (6) is obtained from the continuous representation by means of the mathematical procedure presented in (8) [50]-[51].

$$\begin{aligned}
 A' &= \left(I + \frac{A \cdot T_s}{2} \right) \left(I - \frac{A \cdot T_s}{2} \right)^{-1} \\
 B' &= \left(I - \frac{A \cdot T_s}{2} \right)^{-1} \cdot B \\
 C' &= T_s \cdot C \cdot \left(I - \frac{A \cdot T_s}{2} \right)^{-1} \\
 D' &= C \cdot \left(I - \frac{A \cdot T_s}{2} \right)^{-1} \cdot \frac{B \cdot T_s}{2}
 \end{aligned} \tag{8}$$

2. SRF PLL discretization

The frequency and phase detection are obtained by means of the SRF PLL shown in Fig.6 The discretization of the controller and the integrator has been performed, in this case, using the backward numerical approximation.

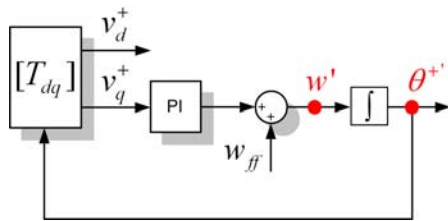


Fig. 6. State variables of the SRF PLL block

The frequency and phase can be then represented in the z-domain as shown in (9), where v_q^+ is the error to be minimized.

$$\begin{aligned}
 W'(z) &= \frac{(k_p + k_i \cdot T_s)z - k_p}{z - 1} \cdot V_{q^+}^*(z) + \omega_{ff} \\
 \theta^{+'} &= \frac{T_s \cdot z}{z - 1} \cdot W'(z)
 \end{aligned} \tag{9}$$

It can be noticed that the previous equations in (9) are equal to those written in (2), as in both cases a SRF PLL is implemented. Likewise, the sampled based representation of (9) can be written as shown in (10).

$$\begin{aligned}
 \omega'[n+1] &= \omega'[n] - k_p \cdot v_{q^+}^*[n] + (k_p + k_i \cdot T_s) \cdot v_{q^+}^*[n+1] \\
 \theta^{+'}[n+1] &= \theta^{+'}[n] + T_s \cdot \omega'[n+1]
 \end{aligned} \tag{10}$$

C. 3phEPLL PLL discretization

This three-phase grid synchronization system exploits the EPLL as a quadrature signal generator. An independent EPLL is used for processing each one of the three phase voltages. The same EPLL structure is applied again to detect the magnitude and phase of the positive-sequence voltage component.

1. QSG block - EPLL discretization

The block diagram of the EPLL implemented in this paper is presented in Fig.7.

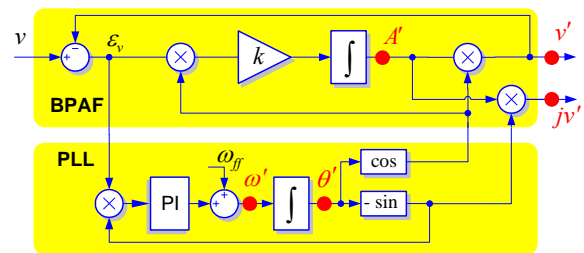


Fig.7. QSG based on an EPLL structure

According to this diagram, the state space representation of the EPLL in the continuous domain can be written as shown in (11).

$$\begin{aligned}
 \dot{A}'(t) &= k \cdot e(t) \cdot \cos \theta'(t) \\
 \dot{\omega}'(t) &= -k_i \cdot e(t) \cdot \sin \theta'(t) \\
 \dot{\theta}'(t) &= \omega'(t) + \frac{k_p}{k_i} \cdot \dot{\omega}'(t)
 \end{aligned} \tag{11}$$

The discrete state space variables representation were described in [44] using a Forward Euler approximation reaching satisfactory results, so the same method has been implemented here.

$$\begin{aligned} e[n+1] &= u[n+1] - v'[n] \\ A'[n+1] &= A'[n] + T_s \cdot k \cdot e[n] \cdot \cos(\theta'[n]) \\ \omega'[n+1] &= \omega'[n] - T_s \cdot k_i \cdot e[n] \cdot \sin(\theta'[n]) \\ \theta'[n+1] &= \theta'[n] + T_s \cdot \omega'[n] - T_s \cdot k_p \cdot e[n] \cdot \sin(\theta'[n]) \end{aligned} \quad (12)$$

Finally, after the state variables are calculated, the EPLL outputs can be obtained by (13), generating thus, the two in quadrature signals.

$$\begin{aligned} v'[n+1] &= A'[n+1] \cdot \cos(\theta'[n+1]) \\ qv'[n+1] &= -A'[n+1] \cdot \sin(\theta'[n+1]) \end{aligned} \quad (13)$$

This kind of discretization method needs a more accurate tuning, due to the fact that the stable region of the s-plane and z-plane are different [52]. However its major simplicity, compared to the Tustin or backward integration, benefits the computational speed of this block.

2. Computational unit block

The description for this block is the same in both discrete & continuous domain. Nevertheless specific equations used in this paper are shown in (13) since some little changes related to notation and some signs have been introduced respect to those presented in [44].

$$\begin{aligned} v_a^+[n] &= \frac{1}{3}v'_a[n] - \frac{1}{6}(v'_b[n] + v'_c[n]) + \frac{1}{2\sqrt{3}}(jv'_b[n] - jv'_c[n]) \\ v_c^+[n] &= \frac{1}{3}v'_c[n] - \frac{1}{6}(v'_a[n] - v'_b[n]) + \frac{1}{2\sqrt{3}}(jv'_a[n] - jv'_b[n]) \\ v_b^+[n] &= -(v_a^+[n] + v_c^+[n]) \end{aligned} \quad (14)$$

3. Phase and magnitude detection block

This element is another EPLL that estimates the phase and the magnitude of the positive-sequence fundamental component. Its discretization is equal to that shown in (12), but the outputs, are the positive sequence magnitude and phase, that corresponds directly with the states θ' and A' .

IV. TESTING SIGNALS AND EXPERIMENTAL SETUP

Following the representations in the discrete domain already deducted, the different PLL's algorithms have been implemented in a control board based on a floating point DSP Texas Instruments TMS320F28335 at 150 MHz (6.67 ns cycle time). Their capability to perform a fast and accurate

synchronization have been tested in the lab under different grid fault scenarios, where the three phase voltage waveforms experience transients due to the appearance of voltage sags, frequency variations and harmonic pollution. These unbalanced and distorted input voltages were generated by means of an AC programmable source and an auxiliary transformer. The layout of the experimental workbench used in this work is presented in Fig.8.

In this study case six representative faulty and distorted scenarios have been selected for evaluating the three synchronization systems under test:

- **Voltage sags:** The characteristics shape of four voltage sags selected in this paper. It is worth to mention that these sags are the most characteristic ones that affect distributed generation systems. In this table the magnitude and the phase of the symmetrical components of the voltage during the fault period is indicated in each case, considering that the pre-fault voltage is always equal to $V^+ = 100$, $V^- = 0$, $V^0 = 0$.

Three of the proposed sags give rise to unbalanced voltages, as explained in [37]-[38], and hence to positive and negative sequence components. The presence of the negative sequence during the fault permits to carry out a more rigorous analysis about the synchronization capability of the different algorithms under test. Moreover unbalanced faults constitute the 95% of voltage sags that affects WTs in real wind farms.

- **Harmonic polluted voltage (8% THD):** According to the EN50160 standard [53] the THD of the voltage waveforms at the output of a generation facility cannot be higher than the 8%.

- **Grid voltage frequency jumps:** By means of the programmable source a 10 Hz jump (from 50 to 60Hz) in the frequency value of the positive sequence has been applied to analyze the response of the frequency adaptive structures under test

In the following section the response of the DDSRF, DSOGI and 3PhEPLL under these transient conditions will be compared.

V. EXPERIMENTAL PERFORMANCE OF THE PLL'S

A. Behavior in case of voltage sags

1. Type 'A' Sag Test

This kind of voltage of sag appears as a consequence of three phase faults that give rise to high shortcircuit currents, and hence to a balanced voltage drop in the network. As Fig.8.e and Fig.8.i show, the DDSRF PLL and the DSOGI PLL perform a good response as both systems achieve a very fast detection (20ms) of the positive sequence components (less than two cycles). The response of the 3phEPLL, depicted in Fig.8.m, shows also a good response, but with a larger transient in the positive sequence estimation

2. Type 'B' Sag Test

This kind of fault permits to analyzing the behavior of the PLLs under test in the presence of zero-sequence components at its input. The Clarke transformation that the DSOGI PLL and the DDSRF PLL used to extract the $\alpha\beta$ components, enhance the response of these synchronization system when the faulty grid voltage presents zero-sequence components. Their response, as shown in Fig.8.f and Fig.8.j is fast and accurate. On the other hand, the 3ph EPLL does not cancel out the zero-sequence component from the input voltage, something that could affect the dynamics of the positive sequence estimation loop. However, this effect is further

attenuated by the computational unit so, as Fig.8.n shows, the steady state response is reached with no great delay as well, as detailed in Fig.8.n, showing the good behavior of this PLL under these conditions.

3.Type 'C'and 'D' Sag test

These kind of sags appear due to phase to ground and a phaseto phase shortcircuits at the primary winding of the transformer, respectively, as shown in TABLE. In a distribution network these distortions are more common than the previous ones, as they are the typical grid faults caused by lightning storms. As depicted in Fig.8.g to Fig.8.p all three

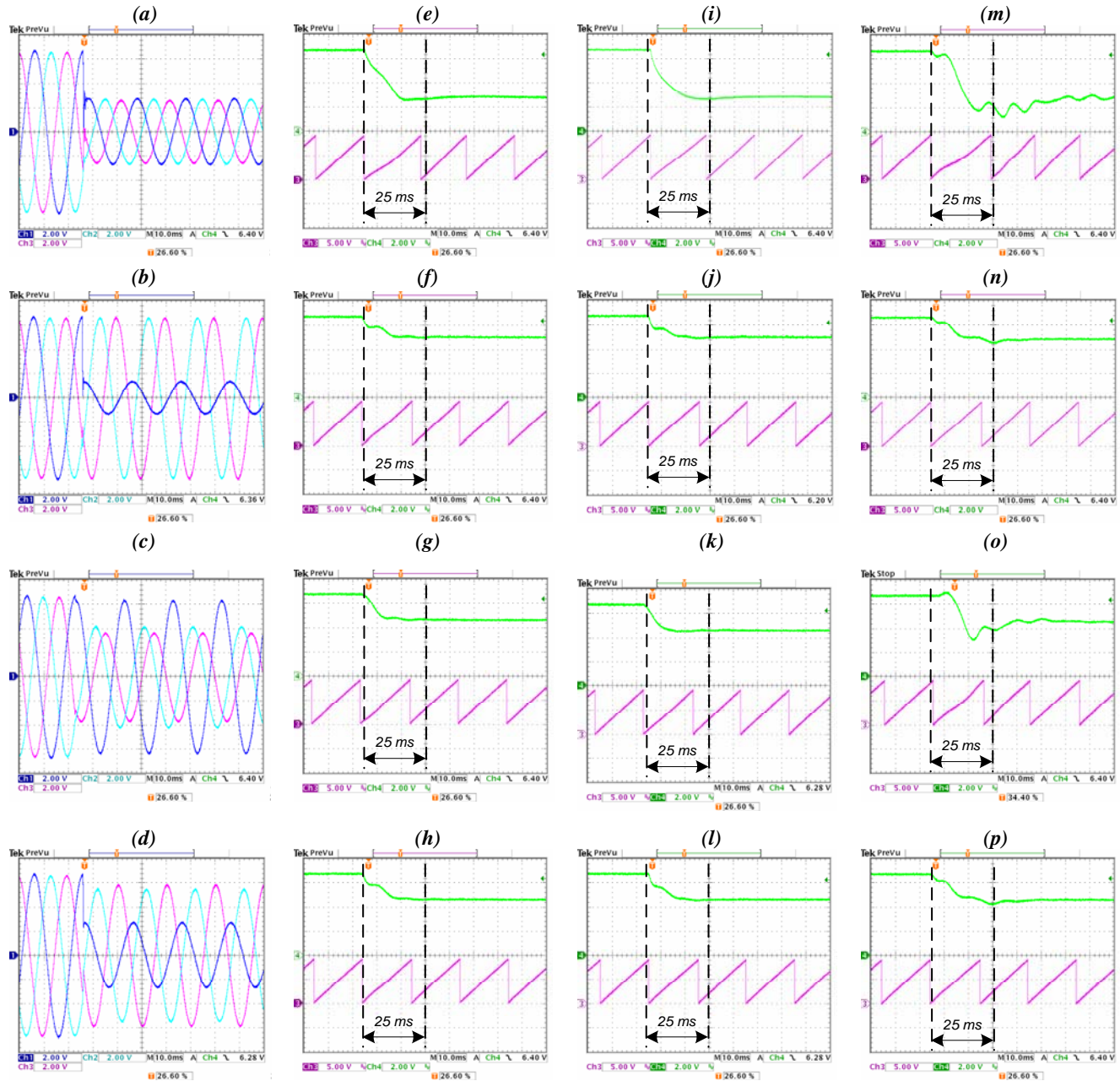


Fig. 8- Amplitude and phase estimation of the 3 tested PLL's in case of 4 type of sags. (a) – (d) Input signal (V); (e) – (h) Amplitude (V) and phase (rad) detection for the DSRF PLL; (i) – (l) Amplitude (V) and phase (rad) detection for the DSOGI PLL; (m) – (o) Amplitude (V) and phase (rad) detection for the 3phEPLL PLL. Scaling factors: Amplitude = 1:150; Phase = 1:7.

PLLs permit detecting the positive sequence between 20-30 ms, however the 3phEPLL, has a slower stabilization, as shown in Fig.8.o and Fig.8.p. This effect is a bit more noticeable with the 'C' sag where the combination of the phase jump and the magnitude change of two phases occurs, as shown in Fig.8.o.

B. Behavior in case of frequency changes (50-60Hz)

In this experiment, similar results are obtained with the DDSRF and the DSOGI PLL, as it can be noticed in Fig.9.a - Fig.9.d. The low overshooting in the amplitude estimation in both cases, Fig.9.a and Fig.9.c, is helping the good phase and frequency detection, as it is shown in Fig.9.b and Fig.9.d. Likewise the response of the 3phEPLL shows a similar settling time, as shown in Fig.9.e, however the initial oscillation in the amplitude estimation of the voltage contributes to delay a bit the stabilization of the frequency magnitude, displayed in Fig.9.f.

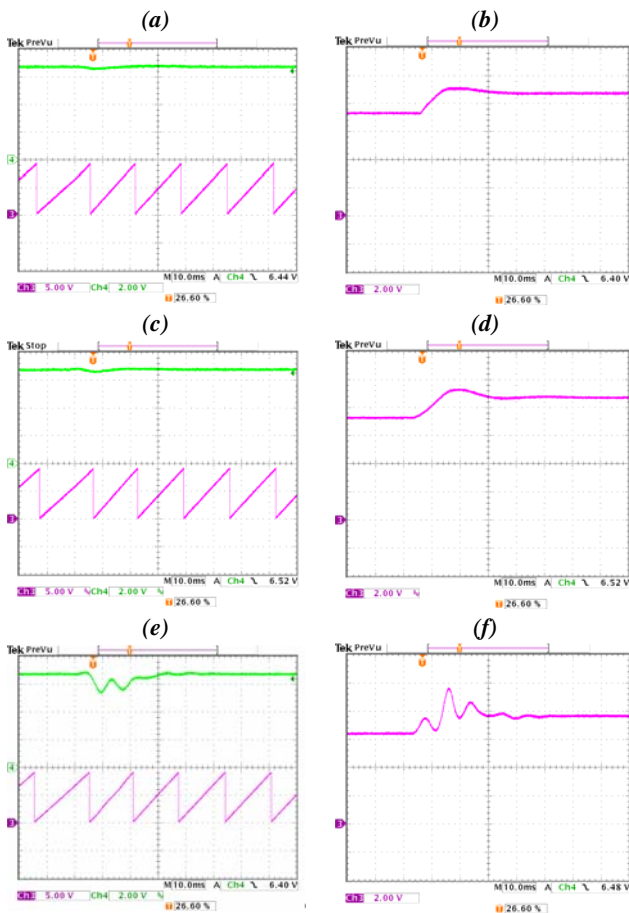


Fig. 9.- Amplitude, phase and frequency estimation of the 3 tested PLL's in a frequency jump. (a) – (b) Amplitude (V), phase (rad) and frequency detection for the DSRF PLL; (c) – (d) Amplitude (V), phase (rad) and frequency detection for the DSOGI PLL; (e) – (f) Amplitude (V), phase (rad) and frequency detection for the 3phEPLL PLL. Scaling factors: Amplitude = 1:150; Phase = 1:7; Frequency 1:70.

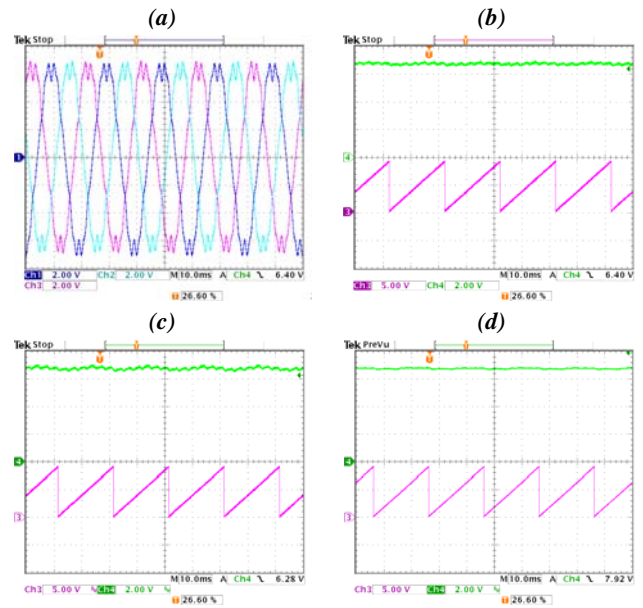


Fig. 10.- Amplitude and phase estimation of the 3 tested PLL's in a polluted grid (THD = 8%). (a) Input signal (V) ; (b) Amplitude (V) and phase detection (rad) for the DSRF PLL; (c) Amplitude (V) and phase detection (rad) for the DSOGI PLL; (d) Amplitude (V) and phase detection (rad) for the 3phEPLL PLL. Scaling factors: Amplitude = 1:150; Phase = 1:7.

C. Behavior in case of polluted grids (THD = 8%)

The 3phEPLL behaves as a bandpass filter for the input signal, something that permits filtering the input without adding extra filters. As it can be seen in Fig.10.d the 3phEPLL is offering the best filtering capability among the PLLs under test, with a clear and undistorted estimation of the magnitude and phase of the input.

The response of the DDSRF PLL, depicted in Fig.10.b, which has a first order filter at the output, is even better than the one provided by the DSOGI PLL, due to the lowpass filtering behaviour of the first one. Although the DSOGI-PLL behaves as well as a bandpass filter the tuning of its parameters, that permits a faster stabilization of the estimated signal in previous tests, plays against its immunity in front of harmonics, as shown in Fig.10.c, giving rise to small oscillations in the positive sequence estimation.

VI. CONCLUSION

As shown in this paper, the DDSRF-PLL and the DSOGI-PLL permit estimating the instantaneous symmetrical components of a three phase system working in the $\alpha\beta$ reference frame, while the 3phEPLL-PLL uses the 'abc' reference frame, working hence with three variables. As it has been proven in this work, this feature simplifies the structure of the DSOGI-PLL and the DDSRF-PLL, that permits reducing their computational burden time if compared with the 3phEPLL-PLL without affecting its performance.

The synchronization capability of the three PLLs under test have shown to be fast and accurate under faulty scenarios, permitting to detect the positive sequence of the voltage in 20-

25 ms in all cases, however the simpler structure of the DDSRF and the DSOGI permits an easier tuning of their control parameters, and therefore a more accurate control of their transient response.

The immunity of the analyzed PLLs in case of having a polluted network is better when using the 3phEPLL and the DDSRF, due to its major bandpass and lowpass filtering capability. Although the DSOGI give rise to reasonable good results as well, due to its inherent bandpass filtering structure, their response is more affected by harmonics.

Although the three of them have shown to be appropriate for synchronizing with the network voltage in wind power applications the lower computational cost of the DDSRF PLL and the DSOGI PLL, together with their robust estimation of the voltage parameters show the better tradeoff between the presented systems, making them specially suitable for wind power applications.

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