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Advanced Voltage Positive Feedback Control for Anti-islanding of a Distribution Generation Inverter

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Abstract. the paper discusses an analytical design of dq-based voltage positive feedback (VPF) control for anti-islanding of a distributed generation (DG) inverter. Design criteria for the voltage feedback gain are presented. Based on small signal stability and step response analysis, an analytical design method for lower and upper bounds of the gain is described. It is proven that conventional VPF gain is significantly influenced by real power levels of a DG. To improve this weakness, a modified VPF is proposed. Simulation study validates the analytical design method and the modified VPF control performance for a constant power- controlled inverters.

Key words
voltage positive feedback gain, dq control, anti-islanding, small signal stability

1. Introduction

Active anti-islanding schemes inject additional disturbance into DG output and destabilize an islanded system so that the system frequency or voltage can deviate from the detection limits. There have been various active methods proposed [1]-[7]. Positive feedback methods based on dq- control have little NDZ, negligible power quality impact, and minimal implement-ation cost, and are also very robust to grid disturbances [7]. Such advantages are available when the positive feedback gains are optimally designed for certain purposes.

This paper presents analytical methods for design of voltage positive feedback control. Design criteria are presented for meeting anti-islanding requirements of international standards and limiting power fluctuations owing to use of the active method. Gain design is considered for a constant-power controlled inverter (CPCI) and a constant-current controlled inverter (CCCI). Analytical expressions for lower and upper bounds of the VPF gain are derived by small signal and step response analysis, which derives that the conventional VPF control[7] significantly depends on output level of DGs. This means that anti-islanding effect and network disturbance impact varies with power output of an inverter, which makes it complicated to design an optimal gain. In order to remove real power dependence of the conventional scheme, a modified voltage positive feedback control is proposed.

Digital time-domain simulation was carried out in PSCAD/ EMTDC, an electromagnetic transient analysis package, to validate the proposed design method. Simulation results show that the proposed analytical design is accurate and reliable.

2. DQ-based Voltage Positive Feedback

A. Concept of VPF in dq control

Voltage positive feedback concept [7] can be applied into *dq*-based control as illustrated in fig. 1.

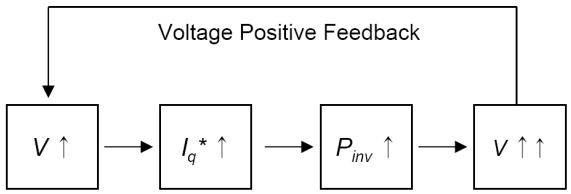

Fig. 1. Voltage positive feedback in dq-frame

If inverter output voltage increases, VPF increases q-axis current resulting in more real power generation, which accelerates the initial voltage increase in islanding until the voltage will be eventually out of bounds for detection. When the inverter is connected to the grid, real power change caused by positive feedback will be absorbed by the grid, thus the resulting voltage variation will be normally negligible. In case that voltage decreases, the same operation mechanism will apply.

B. Implementation of VPF in dq control DGs

There are various types of inverters for grid connection of DGs. In this paper, a constant-power controlled inverter with synchronous rotating dq control structure is considered for VPF implementation.

Fig. 2 shows the control schematic of a three-phase constant -power controlled inverter. Voltage positive feedback can be implemented as illustrated in fig. 3, where a proportional-integral (PI) controller is applied for real and reactive power control.

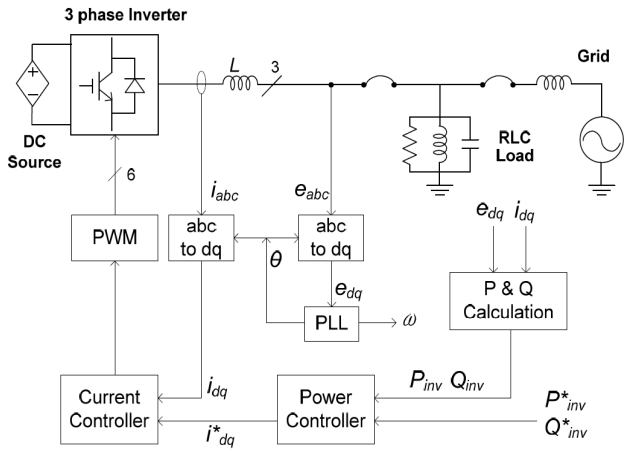

Fig 2. Control Schematic of 3-phase grid inverter

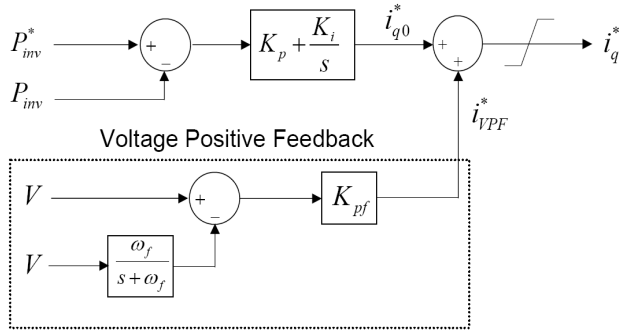

Fig. 3. Voltage positive feedback controller

3. Design of Voltage Positive Feedback Gain

A. Design Criteria

A higher gain indicates that larger disturbance becomes added to real power output of the inverter for the same amount of voltage variation. In island condition, a higher gain will positively contribute to anti-islanding, whereas, in grid-tied condition, a lower gain will mitigate negative impacts on the grid. Therefore, the following criteria are used to determine the lower and upper bounds of the VPF gain.

- For the lower bound, the VPF gain must be large enough to destabilize system voltage in island condition to be out of the specified thresholds. Here, the lower bound is defined as the lowest value at which the islanded system starts being destabilized.
- For the upper bound, the gain must be small enough to limit the real power variation due to a step change of feeder voltage in grid-connected condition within a pre-set value specified by a system designer or user.

B. Lower Bound Design

A small signal analysis is used to determine the lower bound of the VPF gain. The inverter is assumed to be in island condition.
VPF controller in fig. 4 may be described by (1). The current control loop has very fast dynamics, i.e., less than a few mili-seconds, thus in (1), the d-axis current command may be replaced by the actual current id. Linearization of (1) leads to small signal equation (2).

$$(P^* - P_{inv})(K_p + \frac{K_i}{s}) + (V - V\frac{\omega_f}{s+\omega_f})K_{pf} = i_q^* \quad (1)$$

$$-(K_p + \frac{K_i}{s})\Delta P_{inv} + K_{pf}(\frac{s}{s+\omega_f})\Delta V = \Delta i_q \quad (2)$$

For the system of (2) to be unstable, the positive feedback gain should meet the below inequality condition (3).

$$K_{pf} > \frac{6V K_p + \sqrt{2}}{R} \quad (3)$$

The q-axis current iq can be described as (4)

$$i_q = \sqrt{2}V / R \quad (4)$$

In island condition, voltage magnitude range lies between 0.88Vn and 1.1Vn, or island operation will be detected by over- or under-voltage relay protection. Thus V can be approximated as the nominal voltage Vn, and (5) can be deduced from (3) and (4).

$$K_{pf} > \left(3\sqrt{2}K_p + \frac{1}{V_n}\right)\cdot i_q \quad (5)$$

In (5), it should be noted that the lower bound of Kpf is linearly dependent on the q-axis current which is directly related by real power output level of the inverter. To eliminate this dependence, we propose that the VPF gain should be designed as voltage shift acceleration gain KV multiplied by q-axis current command.

$$K_{pf} = K_V \cdot i_q^* \quad (6)$$

From (10) and (11), then, the lower bound expression (12) for a constant-power controlled inverter is obtained.

$$K_V > 3\sqrt{2}K_p + \frac{1}{V_n} \quad (7)$$

C. Upper Bound Design

Voltage step response is analyzed to determine the upper bound. The inverter is assumed to operate in grid-connected condition.
(2) can be rewritten as its Laplace-transformed equation (8).

$$-\left(K_p + \frac{K_i}{s}\right)\Delta P_{inv}(s) + K_{pf}\left(\frac{s}{s+\omega_f}\right)\Delta V(s) = \Delta i_q(s) \quad (8)$$

From (8), the upper limit equation (9) can be obtained by voltage step response analysis.

$$K_{pf} < \frac{\eta}{\Delta V_{step}}\left(1 + \frac{3}{\sqrt{2}}V_n K_p\right)\cdot i_q \quad (9)$$

Here, let us define the criteria for real power disturbance as the ratio of the peak real power disturbance to real power output of the DG, as given in (10).

$$\eta = \frac{\Delta P_{peak}}{P_{inv}} \quad (10)$$

where Δ Ppeak is the peak real power disturbance due to voltage step change.
The upper bound depends on the q-axis current just as the lower bound does. In order to remove dependence on real

power output, Kpf is replaced by (6), and the upper bound expression (9) can be rewritten as (11).

$$K_V < \frac{\eta}{\Delta V_{step}} \left(1+\frac{3}{\sqrt{2}} V_n K_p\right) \quad (11)$$

The upper bound is significantly influenced by the Kp of the upper level controller.

It was found from (5) and (9) that the conventional PF gain had a strong dependence on the real power output of a DG. Instead when the proposed new gain of (6) is applied, the desirable range for constant-power controlled inverters can be written in an explicit expression of (12).

$$3\sqrt{2}\,K_p + \frac{1}{V_n} < K_V < \frac{\eta}{\Delta V_{step}} \left(1+\frac{3}{\sqrt{2}} V_n K_p\right) \quad (12)$$

(12) can be rewritten as (13) for constant-current controlled DGs.

$$\frac{1}{V_n} < K_V < \frac{\eta}{\Delta V_{step}} \quad (13)$$

The modified VPF scheme can be implemented as illustrated in fig. 4.

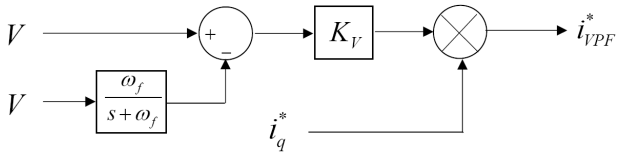

Fig. 4. Proposed voltage positive feedback controller

D. Limiter and Filtering Frequency

The limiter is required to limit the maximum allowable current injection. Normally 150% of rated current is assumed as a thermal limit. 1-10Hz band pass filter is recommended for 2-second detection requirement [8]. In this design, the voltage filtering frequency ω f is 1Hz.

4. Simulation Results

Voltage limits for islanding detection were set according to IEEE Std. 1547. Test settings of the DG inverter and passive RLC load were based on the relevant guidelines specified in the relevant standards [8]-[10].

A. Constant Power-controlled DG

The proportional gain, K_p, and integral gain K_i are both 10. Quality factor is 1.0. η is 0.1, which corresponds to 10% of inverter output, real power generation or *q*-axis current. Desirable range of the voltage shift acceleration gain K_V is calculated as below by (12).

$$47 < K_V < 85.9$$

Fig. 5 shows VPF performance with K_V set to 50. When islanding occurred at 3 [sec] very small voltage shift was captured and the q-axis current was controlled in the direction of increasing the voltage shift. The islanding, eventually, was successfully detected within the detection time requirement of 2 seconds. Fig. 6 shows voltage variations for different values of K_V in islanding condition. The islanded system started being destabilized with K_V =47, which agrees well with the result calculated

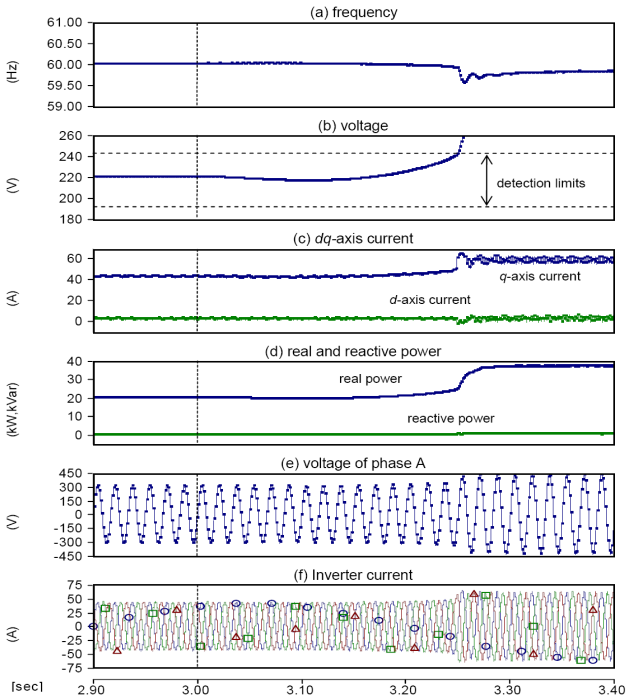

Fig. 5. VPF results for a CPCI with K_V =50

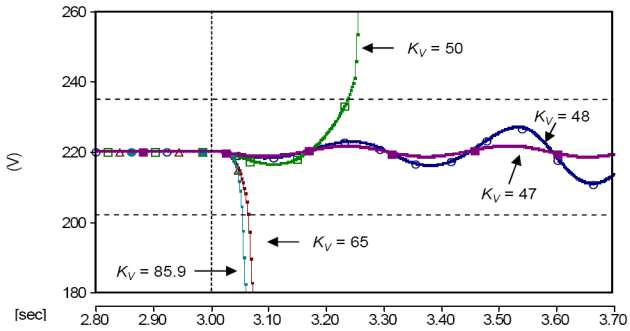

Fig. 6. Voltage variations of a CPCI for different gains of K_V when islanded

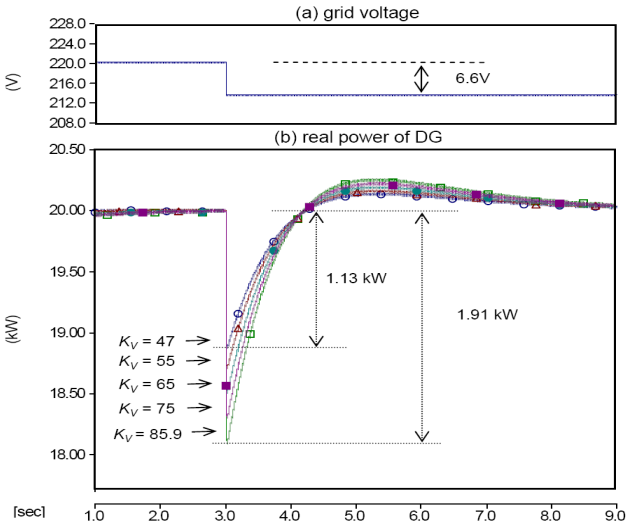

Fig. 7. Real power variations of a CPCI for a step change in grid voltage when grid-connected

by (7). Fig. 6 shows real power variations owing to a step change of in grid voltage, ΔV_{step}, 3% of nominal voltage, when the DG is in grid connected operation. When K_V was 85.9, the upper bound calculated by (7), real power variation caused by the step change of voltage was about

9.55% of real power output of the inverter, which was in good agreement with 10% of design criterion for the upper bound. As shown in figs. 6 and 7, there is a trade-off between anti-islanding and impact on power quality. Gains quite close to the lower bound may not guarantee zero NDZ, and gains close to the upper bound may give serious negative impact on quality of power into grid. It is desirable to select a medium gain between the lower and upper bounds when detailed simulation is not possible.

Tables I, II, and III show the calculated and simulated results for the lower bound of KV with different quality factors, proportional gains, and integral gains of power controller of DGs, respectively. Both the calculated and simulated results were in good agreement. The voltage shift gain is directly influenced by the proportional gain. A higher quality factor requires a higher gain but its dependence is very small: less than 1% variation over the quality factor range of 0.6 to 2.5, which is specified in the standards [8]-[10].

Table I. -Calculated and simulated lower bounds for different quality factors

Qf	Simulated	Calculated
0.6	46.9	
1.0	47.0	
1.6	47.1	47.0
2.5	47.3	
3.0	47.4	

Table II. -Calculated and simulated lower bounds for different propotrional gains

Kp	Simulated	Calculated
2	12.9	13.1
5	25.7	25.7
10	47.0	47.0
15	68.3	68.2
20	89.6	89.4
30	132.1	131.8

Table III. -Calculated and simulated lower bounds for different integral gains

Ki	Simulated	Calculated
2	47.0	
5	47.0	
10	47.0	47.0
20	47.0	
50	47.0	
100	47.1	

When a constant-power controlled is grid-connected, real power fluctuations responding to a step change in grid voltage was simulated for three cases where the inverter was generating 100%, 66%, and 33% of its rating. Results for the conventional method and the modified method are given in figs. 8 and 9. Fig. 8 shows that the step responses of real power were almost identical regardless of output level, about 2kW, which corresponded to 9.5% change for 100% of rating, 15% for 66% of rating, and 30% for 33% of rating. On the other hand, the step responses of the modified method were proportional to output levels, about 9.5% of its output level for all the cases of 100%, 66%, and 33% of rating, as shown in fig. 9. The modified method has less impact on grid in terms of power fluctuation. This is because the modified scheme removed power output dependence of the conventional scheme by incorporating q-axis current into the positive feedback gain.

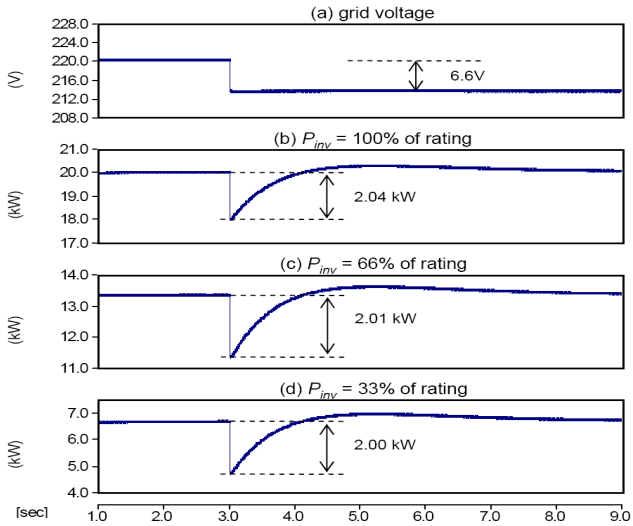

Fig. 8. Real power responses to a step change in grid voltage when the conventional VPF used (a CPCI)

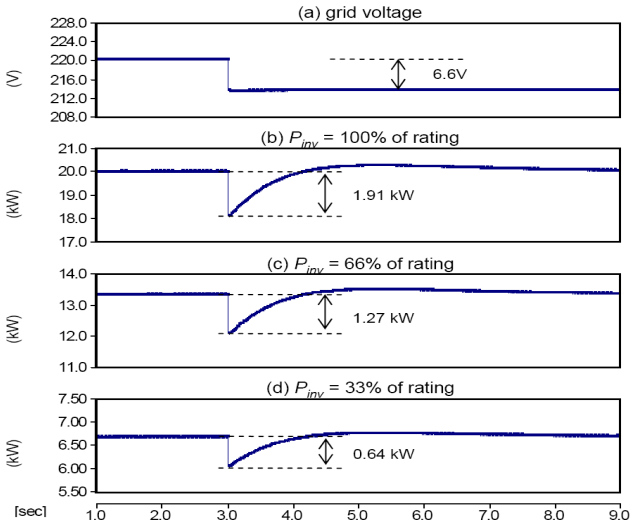

Fig. 9. Real power responses to a step change in grid voltage when the modified VPF used (a CPCI)

B. Constant Current-controlled DG

For constant current-controlled DGs, the range of K_V is determined as below by (13).

$$4.6 < K_V < 15.1$$

Fig. 10 shows VPF results with K_V set to 5.5. Islanding was successfully detected within 2 seconds. Fig. 11 shows voltage variations for different values of K_V. The islanded system started being destabilized with K_V = 4.6, which was in good agreement with the calculated value. The *q*-axis current response due to a step change in grid voltage was shown in fig. 12. At the designed upper bound of 15.1, the resulting response was 4.03 A, corresponding to 9.4% of the rated current, which was in good agreement with the design criterion of 10%. It is reasonable to choose a medium gain with adequate margins from the two bounds.

Table IV shows the calculated and simulated results for the lower bound of K_V with different quality factors, by which the voltage shift gain was not significantly influenced.

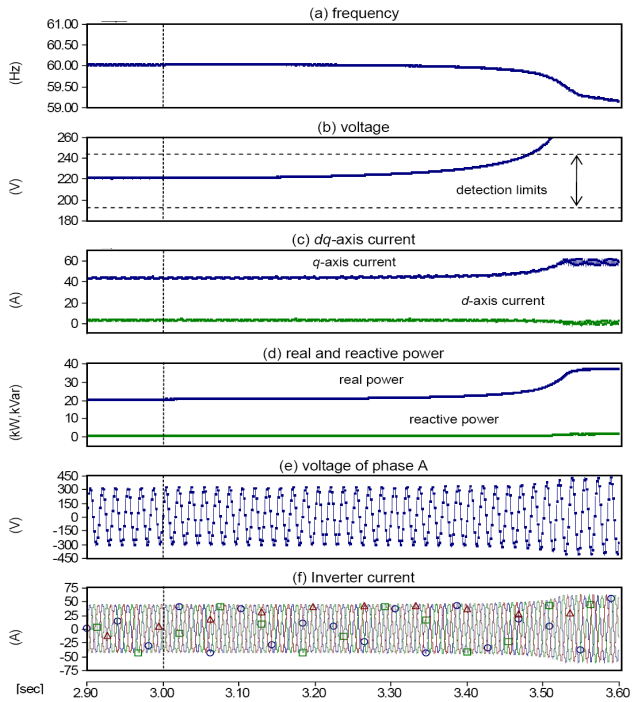

Fig. 10. VPF results for a CCCI with K_V =5.5

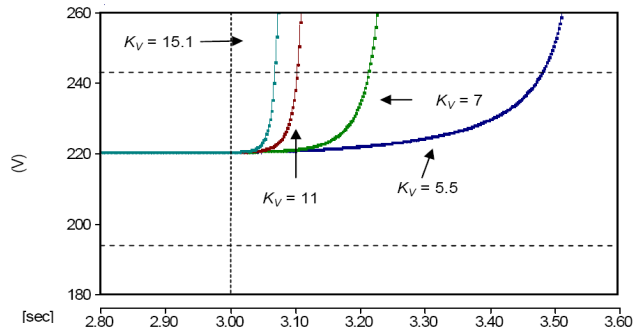

Fig. 11. Voltage variations of a CCCI for different K_V when islanded

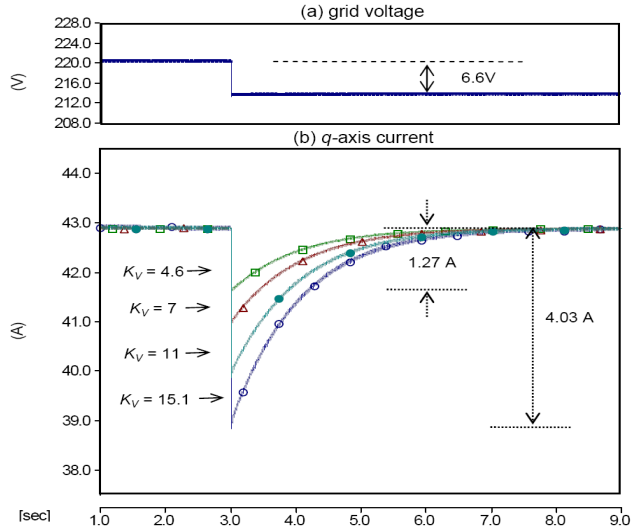

Fig. 12. q-axis current fluctuations of a CCCI for step change in grid voltage when grid-connected

Table IV. -Calculated and simulated lower bounds for different quality factors

Q_f	Simulated	Calculated
0.6	4.57	
1.0	4.58	
1.6	4.59	4.55
2.5	4.61	
3.0	4.62	

Figs. 13 and 14 show the results in cases that two methods were implemented into a constant-current controlled inverter. The q-axis current responses of the modified VPF were proportional to its output current level, whereas those of the conventional VPF were all the same irrespective of the current level. In a constant-current controlled inverter, the modified method is advantageous in mitigated output fluctuations to grid voltage changes.

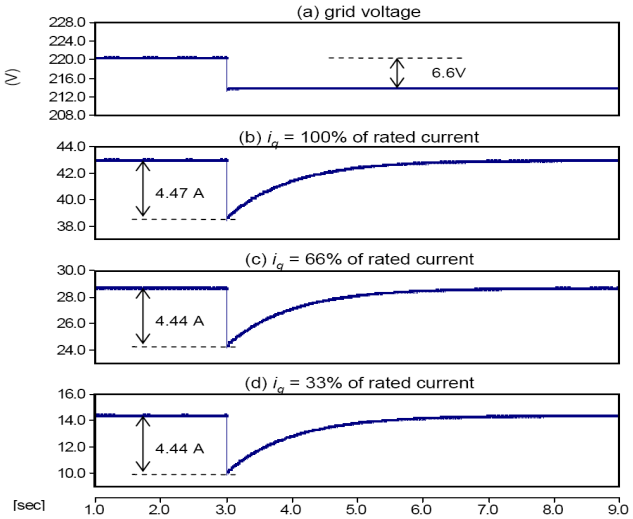

Fig. 13. q-axis current responses to a step change in grid voltage when the conventional VPF used (a CCCI)

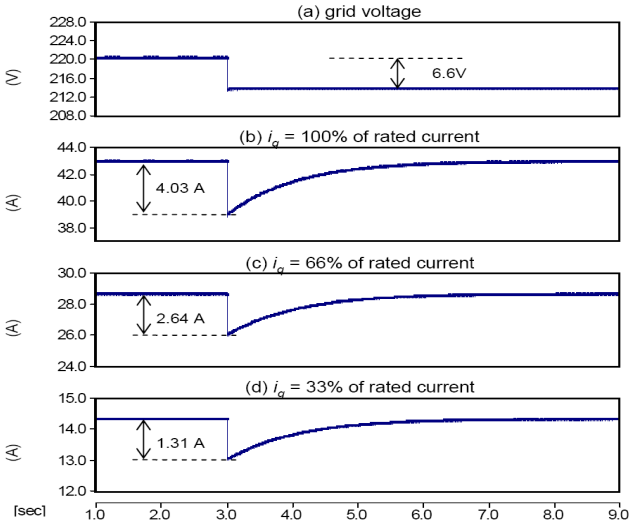

Fig. 14. q-axis current responses to a step change in grid voltage when the modified VPF used (a CCCI)

5. Conclusion

An analytical design method for dq-based voltage positive feedback scheme was proposed. Mathematical expressions for lower and upper bounds of VPF gains were presented for the purpose of implementing a constant-power controlled inverter. It was found that the conventional VPF scheme depended on output levels of DGs, which made its control performance variant with DG's output. The modified method incorporated real power component, q-axis current in this study, into its positive feedback gain so as to break the dependence. Simulation results verified that the proposed design and modified VPF was effective and reliable

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