International Conference on Renewable Energies and Power Quality (ICREPQ'13)
Bilbao (Spain), 20th to 22th March, 2013
Renewable Energy and Power Quality Journal (RE&PQJ)
ISSN 2172-038 X, No.11, March 2013

Development of a new mixed 5-level inverter for 3 kW household photovoltaic applications

A. Caldeira, S. Jacques, A. Schellmanns, J.-C. Lebunetel, N. Batut and L. Gonthier

GREMAN – UMR-CNRS 7347
University of Tours
7 avenue Marcel Dassault, 37200 Tours (France)
Phone number: +33 (0)2 47 36 13 38, e-mail: adelphe.caldeira@univ-tours.fr

Abstract. Multilevel inverters are well used in high power electronic applications (about 10 kW) because of their ability to generate a very good quality of waveforms, reducing switching frequency, and their low voltage stress across the power devices. However, inverter architecture must be modified in order to take into account the different photovoltaic (PV) problems in conventional installation. This paper presents a comparative study of 5-level Neutral Point Clamped (NPC) and a new mixed 5-level inverter. The theoretical study is validated using simulation with the LTspice environment. The output voltage and total harmonic distortion are particularly compared. An experimental 5-level inverter was realized in order to validate analytical results.

Key words

PV application, Capacity's reliability, Leakage current, 5 Level NPC inverter, Harmonic distortion,

1. Introduction

The energy efficiency of a photovoltaic installation depends mainly on two conversion stages: the PV module and the DC/AC converter. In this paper, the PV inverter is the point of focus of the study. Nowadays, H-Bridge inverters are well used because of their quite simple design and cost-effectiveness. However, the use of this kind of topology in PV applications can lead to some operating problems.
PV modules are composed of inherent stray capacitances and particularly between the silicon cell and aluminum structure. This capacitance value, that could be equal to 150 nF.kW^{-1}, [1], depends on the humidity level and the cell technology of the PV module, [2], [3].

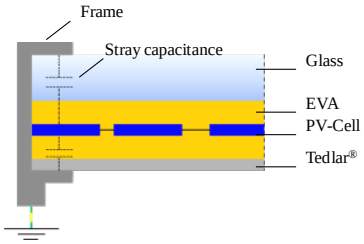


Fig. 1. Inherent stray capacitances of a PV module.

The mechanical PV structure is earthed. The positive or negative module polarity is connected to the DC/AC converter. This polarity level varies because of the switching of the devices. The variable voltage on parasite capacity leads to leakage current flowing to the earth.

The NFC 15-100 and UTE C 15-712 standards require the use of 30 mA differential circuit breaker inside the PV installation. However, the leakage current can increase over 30 mA that leads to the installation shut down. So, the limitation of earth leakage currents has become an important challenge.

One of well-known converter structure that is able to eliminate earth leakage currents is the NPC (Neutral Point Clamp converter) topology. Because the middle point of the DC source is fixed (clamped by diodes), no current can be generated.
In symmetrical configuration, the output voltage is divided by 2 for 3 levels NPC compared to the H-Bridge converter. To obtain an H-Bridge equivalent output voltage, it's therefore necessary to double the DC source level. Unfortunately, it requires an increase of the voltage stress on the semiconductor switches. One solution consists in using a five-level NPC topology. This converter improves the Total Harmonic Distortion (THD) of the output voltage and current and no leakage current can flow through the structure.

Regarding a NPC converter, the number of levels "N" is defined as:

$$N=k/2+1 \quad (1)$$

where, k is the number of semiconductor switches

For example, a 5-level inverter requires 8 semiconductor devices and the number of clamping diodes is multiplied by 3.compared to an H-bridge topology. Furthermore, the number of sources and decoupling capacitors is doubled. The increase of components number implies a cost increase that is the main drawback of this converter topology.

The Mean Time Between Failure (MTBF) of PV systems is estimated between 80,000 h to 100,000 h [4]. One of the major causes of breakdown is the gradual fatigue of the electrolytic condensers commonly used to smooth the DC bus voltage. Furthermore, their aging is accelerated by the increase of the ambient temperature inside the converter. Indeed, according to (2), the aluminum electrolytic condenser lifetime is divided by two for 10 °C temperature increase [5].

$$H = L_u \times 2^{(T_0 - T)/10} \quad (2)$$

where, H = lifetime; Lu = estimated lifetime for a T_0 temperature level; T = operating temperature

This article aims to develop and validate a new mixed 5-level inverter structure limiting the number of components, the use of decoupling capacitors compared to 5-level NPC topology and limiting the earth leakage current compared to H-Bridge one.

This new topology is particularly compared with a 5-level NPC one. A theoretical study is presented and validated using the LTspice simulation tool. The output voltage and THD are analyzed.

2. Theoretical analysis

A. 5-level NPC inverter reminder

Fig. 2 shows an operating phase of 5-level NPC inverter in symmetrical configuration [6]. This topology is composed of 8 bidirectional current and unidirectional voltage switches and 6 clamping diodes.

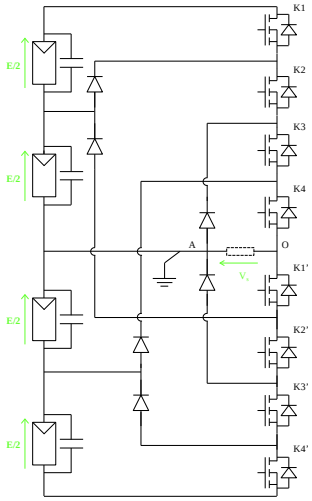


Fig. 2. Electrical schematic of 5-level NPC inverter.

Fig. 3 only describes the positive operating sequence (level 1 to 3) but the different steps are summarized in Table 1, where the output voltage ("Vs") is indicated.

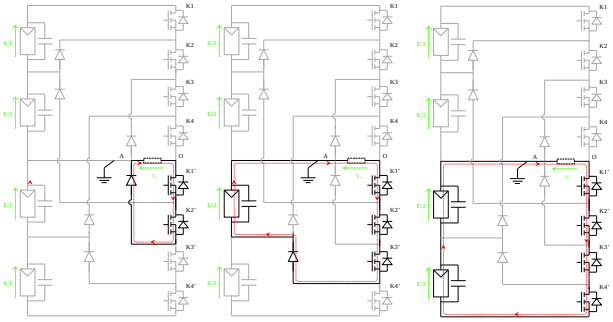


Fig. 3. Switching sequence of 5-level NPC: a) Vs = 0, b) Vs = E/2, c) Vs = E.

Table 1. State of switches and voltage of the 5 levels NPC converter.

Level	Switches controlled	Vs
Level 1	K3 ; K4 ; K1' ; K2'	0
Level 2	K1' ; K2' ; K3'	E/2
Level 3	K1' ; K2' ; K3' ; K4'	E
Level 4	K2 ; K3 ; K4	-E/2
Level 5	K1 ; K2 ; K3 ; K4	-E

B. Development of a new mixed 5-level inverter

The architecture proposed is shown on Fig. 4. This kind of structure is based on the mixture between a H-Bridge converter (composed of the K1, K4, K7 and K8 semiconductor switches) and a NPC (composed of the K1-K4 devices) one. The K5 and K6 power switches allow a bidirectional current and voltage operating mode because of the symmetrical configuration of the converter (one phase inverter).

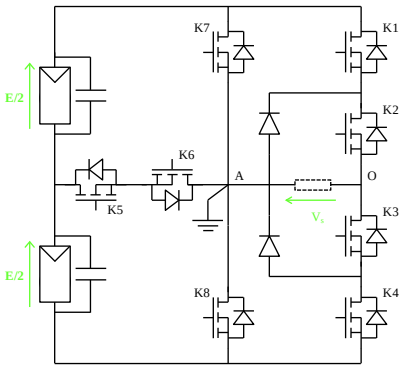


Fig. 4. Electrical schematic of the new mixed 5-level inverter proposed.

Fig. 5 shows the operating mode of this new converter and particularly for positive output voltage.

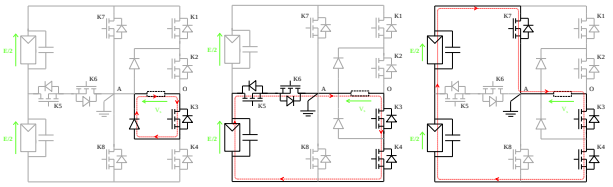


Fig. 5. Switching sequence of 5 level converter proposed: a) Vs = 0, b) Vs = E/2, c) Vs = E.

Table 2 synthesizes the different operating steps.

Table 2. State of switches and voltage of the 5-level converter proposed.

Level	Switches controlled	Vs
Level 1	K2 ; K3	0
Level 2	K3 ; K4 ; K5 ; K6	E/2
Level 3	K3 ; K4 ; K7	E
Level 4	K1 ; K2 ; K5 ; K6	-E/2
Level 5	K1 ; K2 ; K8	-E

Table 3 sums up the maximum voltage constraint of the two comparative topologies, the number of voltage sources needed to build the 5 voltage levels and the number of semiconductor switches.

Table 3. Operating mode of the mixed 5-level inverter proposed.

	5-level NPC inverter	**5-level inverter proposed**
V_{switch} max	E/2	E/2
Nb. of source	4 x E/2	2 x E/2
Nb. of switch	14	10

The proposed converter allows a lower design cost and the number of sources and capacitances are divided by two.
It is important to notice that the cost and energy conversion efficiency of the proposal topology could also be improved by replacing the K5 and K6 switches by a voltage and current bidirectional switch. An interesting switch called "ISIS" could be implemented [7]. This is a low heat dissipating integrated switch (0.7 W/A) design for houses application. However, its electrical characteristics do not correspond to our needs at this time (600 V / 5 A).

C. Principle of 5-level converter control

A widely used method to control inverter connected to the grid is the Pulse Width Modulation (PWM), and particularly, Sinusoidal Pulse Width Modulation (SPWM) [8]. This method is used for the output signal quality. Harmonics are shifting to higher values that improve the THD. So, the output filtering is easier and cheaper.

The principle is based on the comparison of a reference signal (i.e. signal to be synthesized, here a 50 Hz sinusoidal) with a carrier [9]. The carrier frequencies must be higher or equal to 20 times the modulating signal (typically, a centered triangle signal or a sawtooth signal) [10].
To generate PWM control for a multilevel converter with « N » levels, it is needed to compare the "N-1" triangular carriers to the reference signal (see Fig. 6).

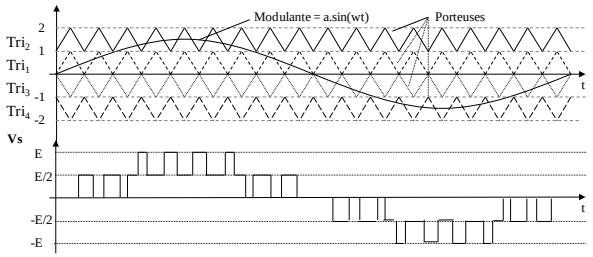


Fig. 6. Control signal for a 5-level converter.

Each comparison gives 1 if a carrier is higher or equal to the reference and 0 in the other case. The carrier « Tri_1 » determines level 1 and « Tri_2 » and « Tri_3 », respectively the level 2 and 3. The Table. 4. resume the control working.

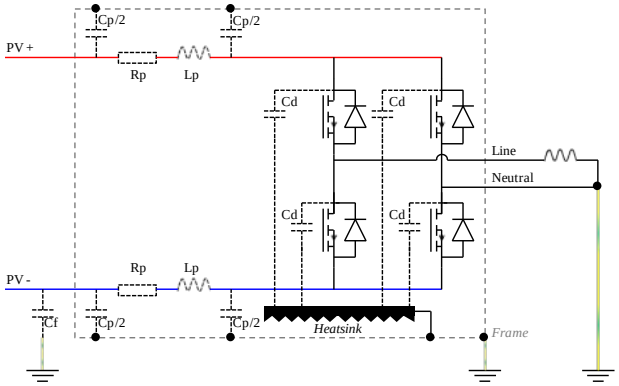
Table 4. PWM control states of the 5 levels converter.

State	Vs
Tri_3 < Sinus < Tri_1	0
Sinus > Tri_1	E/2
Sinus > Tri_2	E
Sinus < Tri_3	-E/2
Sinus < Tri_4	-E

3. New inverter topology validation using SPICE simulation

A. Foreword

Several electrical simulations were performed, using the LTspice environment, to validate the theoretical analysis described previously. In particular, the two last structures (5-level NPC inverter and new mixed 5-level inverter) were compared to the standard H-bridge converter. Fig. 7 shows the H-bridge simulation schematic taking into account all the parasitic elements (inductances and capacitances) that could also be found in the two 5-level topologies. The capacitance element (C_p) represents wire coupling with the ground plan. The resistance and inductance element (R_p and L_p) represents the wires resistive and inductive behavior of. "C_d" is the coupling capacitance between the switch rear faces and the thermal heat sink.
A 3 kW inverter is considered in this paper. The input voltage "E" and output current "I_s" are equal to 400 V and 13 A respectively. The load is a resistance to simplify the study. The SPWM switching frequency is equal to 16 kHz (frequency higher to 20 times the modulating signal and quite near to the limit audible song).



where: L_p*= 76 nH ;* C_p*=3,3 pF ;* R_p *= 10,4 mΩ*

Fig. 7. H-bridge converter parasitic elements.

B. 5-level NPC inverter simulation

Fig. 8 shows the output voltage (Vs) and the sinusoidal modulating signal.

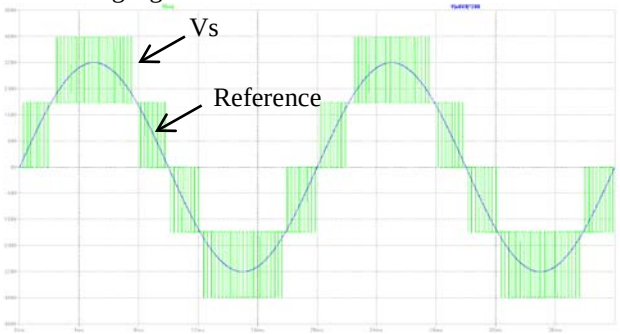


Fig. 8. Output voltage for the 5-level NPC converter.

Fig. 8 shows the five levels of the output voltage (0; E/2; E; -E/2; -E). The voltage waveform approach to a sine wave. Fig. 9. shows the output voltage spectrum harmonic for the NPC topology.

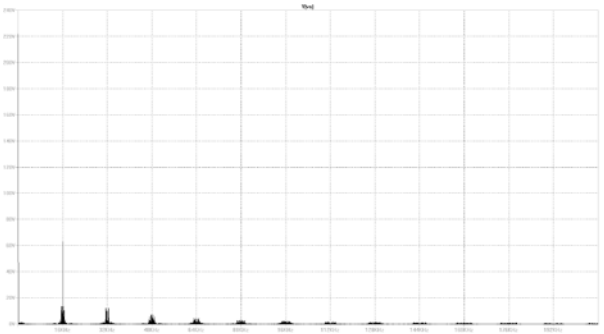


Fig. 9. Harmonic spectrum of the output voltage for the 5 level NPC converter.

The harmonic value number 2 (at switching frequencies) represents 27% of the fundamental one and the third, only 4.5%. The low harmonic value confirms the output sinusoidal behavior. The THD value is equal to 37%.

C. Simulation of the new mixed 5-level inverter

Fig. 10 shows the output voltage (Vs) and the sinusoidal modulating signal.

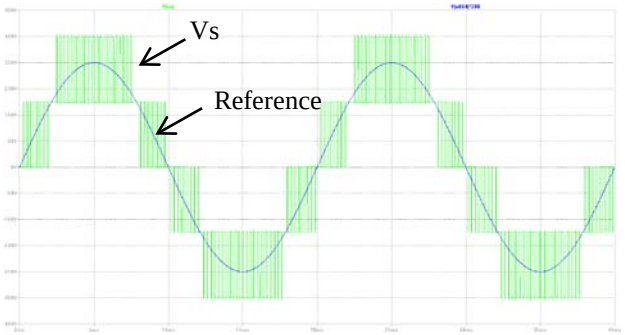


Fig. 10. Output voltage for the new 5-level inverter proposed.

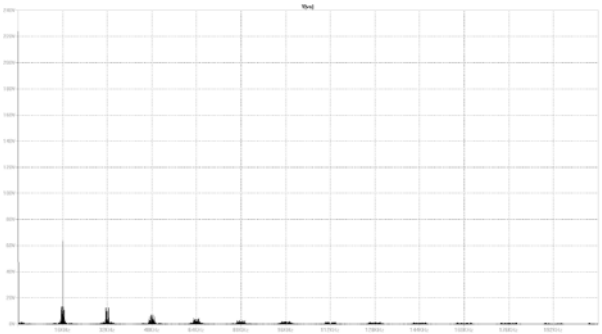


Fig. 11. Harmonic spectrum of the output voltage for the new 5-level inverter proposed.

Fig. 10 and 11 shows results quite identical than NPC ones because of the same control method is used.

Table 5 sums up the THD level for the H-bridge, 5-level NPC and new 5-level inverters. The leakage current and RMS output voltage are also taken into consideration.

Table 5. Simulation results of the two 5-level inverters and comparison with the H-bridge converter.

		H-Bridge	**NPC 5-level**	**Mixed 5-level**
THD [%]		139	37	35
I_{cf} [A]		9,09	0	4,64
V_{seff} [V]	**1-10MHz**	374	237	238
	1-06KHz	219	222	224
	Δ	155	15	14

The two 5 level converter reduce significantly the output voltage THD compare to the H-bridge topology. The value is divided by four (with bidirectional PWM).

The proposal converter improves the leakage current level. It's approximately divided by 2. This topology is so interesting because of the good output quality signal and a lower leakage current level. Moreover, the number of component is reduced compare the NPC topology.

4. Experimental validation

A test prototype of the new mixed 5-level inverter was designed. Fig. 13 to 15 show the results of experimental measurements under reduced voltage and power (in the following conditions: Vs = 220 V RMS; E = 300 V, Is = 2 A). In particular, Fig. 13 shows the four control signals resulting from the comparison of the sinusoidal reference

and the four carriers. Fig. 14 shows the output voltage and output current without any filtering.

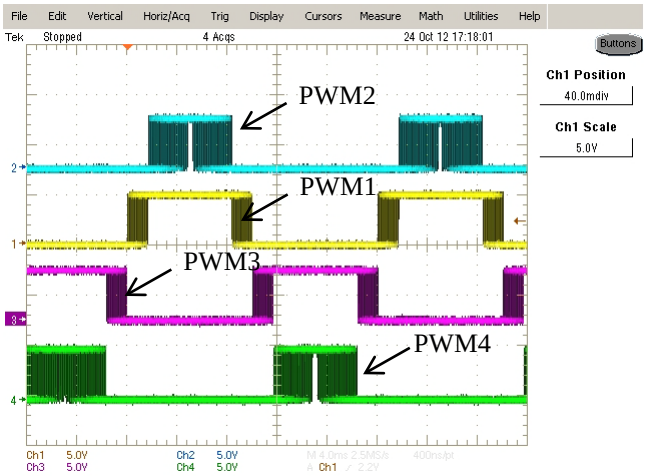


Fig. 13. PWM control signals of the new 5-level inverter proposed.

The switching frequency used by the TTL numerical control circuit (a Digital Signal Processor) is equal to 18 kHz (20 ms / 360 pts). Logical circuit controls the eight switches by means of opto-isolator.

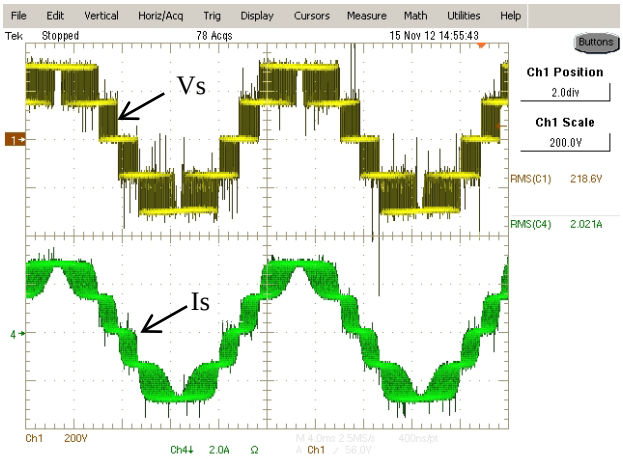


Fig. 14. Output voltage and output current for the new 5-level inverter proposed.

We can show that experimental results correspond to those waited, a modulated signal at five levels. Because of the inductive behavior of the resistive load (i.e. rheostat), the output current is filtered (≈ 0.5 mH). The current THD measured is shown on Fig. 15. The value at 18 kHz is about 37% as simulation results highlighted previously.

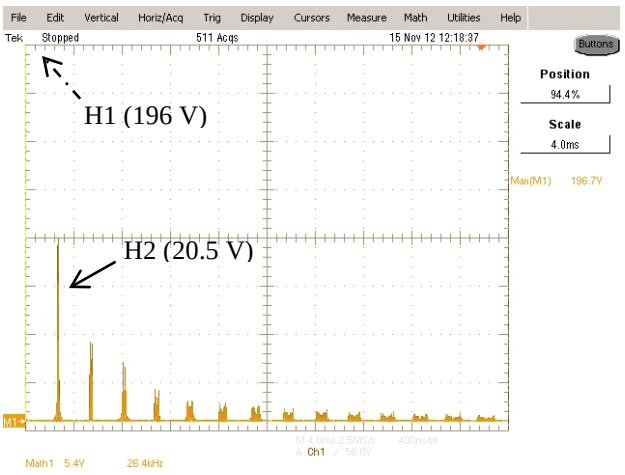


Fig. 15. Output voltage and harmonic spectrum for the new 5-level inverter proposed.

5. Conclusion

In this paper, a concept of a mixed 5-level inverter is proposed to improve the global solar energy conversion efficiency of household photovoltaic systems. In particular, this kind of inverter could be helpful to reduce earth leakage currents that are currently responsible for the shutdown of solar energy production.

The new inverter topology described in this paper is based on the mixture between a 2-level H-Bridge converter and a 3-level NPC structure. A 5-level NPC inverter might have been an approach to consider. However, this kind of topology does not fully satisfy the above-quoted objective. A comparative study between a 5-level NPC inverter and the new mixed 5-level converter is introduced to get a better understanding of the differences between the two topologies.

A complete simulation analysis highlighted that the new multi-level inverter proposed enables to reduce the voltage drop of the semiconductor switches and improve the output signal quality. The THD, which has approximately the same value as a 5-level NPC inverter, is divided by four compared to the well-known H-Bridge structure. The number of power components and input capacities are reduced compared to the NPC topology one (10 even 9 power switches and 2 input capacitances for the new mixed 5-level inverter compared to 14 power devices and 4 input capacitances for the 5-level NPC topology). Thus, the robustness of the converter could be improved.

The new mixed 5-level structure operation was validated by experimental measurements. The first results help to highlight the advantages of this kind of structure to address the problem of earth leakage currents limitation and robustness increase of the inverter to improve the energy efficiency of photovoltaic systems. However, additional measurements are required to complete the analysis.

References

[1] T. Kerekes, R. Teodorescu, M. Liserre. “Common mode voltage in case of transformerless PV inverters connected to the grid”. IEEE International Symposium on Industrial Electronics (ISIE’08), 2008, pp. 2390-2395.

[2] S.V. Araujo, P. Zacharias, B. Sachan. “Novel grid-connected non-isolated converters for photovoltaic systems with grounded generator”. Power Electronics Specialist Conference (PESC’08), 2008, pp. 58-65.

[3] T. Kerekes, R. Teodorescu, U. Borup. “Transformerless photovoltaic inverter connected to the grid”. Applied Power Electronics Conference (APEX’07). 2007, pp. 1733-1737.

[4] D.Violaine. “Inverters for photovoltaic systems’’, Hespul 2007.

[5] G. Sam, JR. Parler. “Selecting and Applying Aluminum Electrolytic Capacitors for Inverter Applications”. Cornell Dublier, 30/10/2007.

[6] M. Baldé, M. L. Doumbia, A. Chériti, C. Benachaiba, Comparative study of NPC and cascaded converters topologies, Renewable Energy & Power Quality Journal, No.9, 12th May 2011.

[7] L.-V. Phung, C. Benboujema, N. Batut, J.-B. Quoirin, A. Schellmanns, L. Jaouen, L. Ventura, “Modeling of a New SOI Bidirectional Bipolar Junction Transistor for Low-Loss Household Appliances”, IEEE Transactions on Electron Devices, 2011, pp. 1164-1169.

[8] L. Hassaine, E. Olías, M. Haddadi, A. Malek. Sam, JR. Parler. “Asymmetric SPWM used in inverter grid”. Revue des Energies Renouvelables,Vol. 10 N°3, 2007.

[9] Subhransu Sekhar Dash, P.Palanivel, S.Premalatha, Performance Analysis of Multilevel Inverters Using Variable Switching Frequency Carrier Based PWM Techniques, Renewable Energy & Power Quality Journal, No.10, 25th April 2012.

[10] H. Foch, F. Forest, T. Meynard. “Voltage inverter : processing’’. Techniques de l’ingénieur, 2000.