International Conference on Renewable Energies and Power Quality (ICREPQ'13)
Bilbao (Spain), 20th to 22th March, 2013
Renewable Energy and Power Quality Journal (RE&PQJ)
ISSN 2172-038 X, No.11, March 2013

A CASE STUDY ON HIGH POWER COMPENSATOR OF THE POWER GRID IRREGULARITIES FOR INDUSTRIAL APPLIANCES

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The paper presents a case study on development of the high power compensator of the power grid irregularities. The compensator is dedicated for sensitive industrial installations protection against dips, sags and short duration interruptions in public power network. The energy for compensation will be stored in bank of high voltage stacked supercapacitors. The development of the new high power medium voltage compensator will be based on experience gained during the realisation in The Electrotechnical Institute Gdansk Branch a similar medium power low voltage device. The study includes: main power converter topology considerations with some preliminary simulation results including harmonic components discussion, the solution to the problem of fast identification of the grid voltage disturbances, the solution to the problem of compensator waveforms synchronization with the grid and the description of the main operational algorithm of the compensator.

Key words – power quality, voltage interruptions, voltage dips and sags, power converter.

1. Introduction

The increasing number of non-linear devices connected to the public grid as well as increasing share of unstable renewable energy sources lead to deterioration of the energetic system reliability. To cope with this situation it is necessary to increase the number of switchover operations, generating voltage disturbances of short duration. These disturbances can be identified as: surges (1), flickers (2), voltage deviations (3), dips (4), interruptions (5) and wave shape disturbances (5). The typical disturbances in public supply grid are presented in fig. 1.

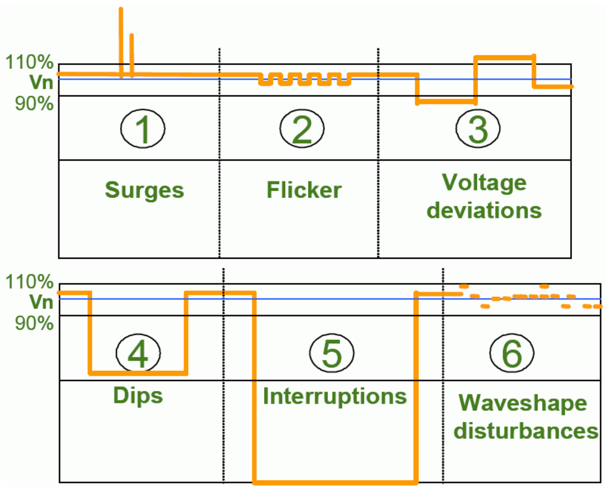

Fig. 1. The typical disturbances in public grid.

Even brief supply interruptions may cause the malfunctioning of the sensitive industrial installations, therefore arises the need for devices able to protect such receivers against the power outages. For low power, one phase devices like computers there is already established practice of using uninterruptible power supplies (UPS) with chemical batteries as energy sources. The standard computer type UPS device allows for maintaining the power during the interval of several minutes to several hours. This kind of solution is not suitable for high power, three phase industrial installations.

Because more than 90 % of public grid failures are short-time disturbances in a shape of voltage dips and short interruptions, it is reasonable to concentrate on compensating only this kind of irregularities, without setting-up the huge energy storage for long term supply. The idea of short duration disturbances industrial compensator has been developed in Gdansk Branch of The Electrotechnical Institute in the frame of COST Action 542: High Performance Energy Storages for Mobile and Stationary Applications. The energy storage for the proposed compensator is based on high voltage supercapacitors. This kind of energy storage do not need any service applied usually to energy storage devices based on batteries. The supercapacitors have also large number of charge/discharge cycles, high level of charge and discharge current and wide working temperature range.

Based on this idea a prototype of medium power (100 kW), low voltage (400 V) three phase compensator has been developed and tested in Gdansk Branch of The Electrotechnical Institute as a result of a special research project COST/255/2006 [1]. The experience gathered during designing and testing this prototype will now be used in new project of high power (1 MW) medium voltage (6 kV) three phase compensator.

2. Identification of voltage disturbances

In order to compensate the grid voltage disturbances effectively they must be immediately detected or even anticipated. The instant diagnostics of the failure state is the elementary condition of the effective compensator performance allowing for rebuilding the necessary voltage level and shape. However methods faster than depicted in [11] were not used because of independent controllers in each phase.

If detection of lower voltage states (dips) occurs when the network voltage and the time base generated by the control circuit are synchronized than it is possible to determine the current voltage amplitude of the first harmonic A_1 of the signal $u_s(t)$. The amplitude A_1 is given:

$$A_1 = \left| 2 \cdot \sum_{n=0}^{N-1} u_s(n) \cdot \sin(2\pi n / N) \right| \qquad (1)$$

where: $u_s(n)$ – n-th sample of the input signal,
n – input sample index,
N – number of input samples or frequency components of the discrete Fourier transform (DFT).

The idea of the actual and reference voltage comparison ("prediction") in an interval T is illustrated in Fig. 2. The reference voltage signal is created as a predictive alternating voltage synchronized with the fundamental harmonic of the mains voltage. The comparison process occurs only in selected intervals of the period T. Comparison results during short zero crossing intervals are not taken into consideration. These intervals have been adopted experimentally and set on the value of ± 1,25 ms. Analyzing deviations of the instantaneous voltage outside zero crossing intervals results in that, in the worst case, a delay compensator response to a dip will be in maximum $t_{opmax} = 2.5$ ms (2 • 0,125 • T/2, T = 20 ms). Nevertheless the likelihood of such events during process comparison is small and the delay will relatively be comparable with the assumed cycle of sampling (e.g. Tp = 80 µs typically). A parameter which better describes the possible delay of dip detections is the expected value. In the presented method this value could be estimated at approximately 0.7 ms as the average delay time course of variability shown in Figure 2b.

In the case of strong deformation of voltage waveform in the network the above described method may result in detection of dips even though the root-mean-square (rms) voltage is acceptable. In this case the predicted signal should take into account the most likely form of the forecast. Inclusion of an appropriate reference signal distortion can be obtained taking into account the higher harmonic components. The amplitudes of these components can be calculated using the conversion formula (1).

Effective dips detection, fast and highly immune to noise, requires the use of specialized algorithms, including the synchronization mechanism (described below) by FFT or wavelet transform. The main difference between the wavelet transform described in [8] and DFT is that the first one operates in the time domain while the FFT in the frequency domain and uses variable window sizes to capture voltage changes. But practical implementation to the detection process is still difficult [11].

In [5] the dip detection mechanism was performing in two ways: exploring patterns of instantaneous value deviation and the r-m-s value of the measured waveform.

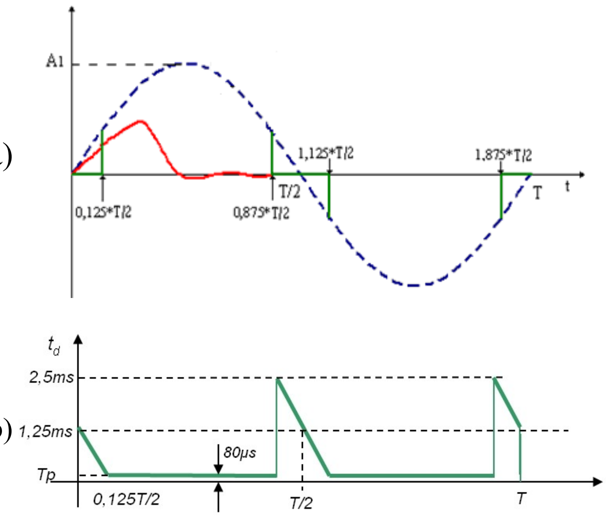

Fig. 2. The detection mechanism: a) comparison of the real and predicted signals in the interval T (one period) and marked zones of measurement insensitivities; b) a way to estimation of average delay of the dip detection.

3. Synchronization with the mains voltage

In order to minimize transients after power outage of the main supply a replacement supply source (loss compensated) must have an amplitude and phase of the voltage compatible with pre-distortion waveform. Compensator controller provides synchronization of the internal reference voltage signal generator with voltage occurring during proper operation of the main power supply by means of phase locked loop (PLL). The applied software method of synchronization with the mains voltage is based on the use of DFT transforms signal us(t) into two orthogonal components of the formula:

$$Us(m) = \sum_{n=0}^{N-1} u_s(n) \cdot [\cos(2\pi nm / N) - j\sin(2\pi nm / N)] = \mathrm{Re}Us(m) + j\,\mathrm{Im}Us(m) \qquad (2)$$

where: $U_s(m)$ – m-th component of the DFT,
m – output component index in frequency domain,
$u_s(n)$ – n-th sample of the input signal,
n – input sample index,
N – number of input samples or frequency components in the DFT.

If the signal $u_s(t)$ is an odd function of time and the period of input signal is T = Tp • N (Tp – sampling period, N – constant) then the real components of DFT will be zeroes:

$$Us(m) = -j\sum_{n=0}^{N-1} u_s(n) \cdot \sin(2\pi nm / N) \qquad (3)$$

In case of no synchronization, when $T \neq Tp \cdot N$, where T is the period of the signal $u_s(t)$, the real component $\mathrm{Re}(U_s(m))$ and imaginary component $\mathrm{Im}(U_s(m))$ have nonzero values. The equation (3) describes the synchronization state of the odd components of the signal $u_s(t)$ with the sampling system.

The compensator should synchronize the sampling system with the first harmonic of grid voltage for $m = 1$. The angle between the vector us(1) and the real axis is described by the formula:

$$\varphi(1) = \arctan \frac{\mathrm{Im}Us(1)}{\mathrm{Re}Us(1)} \quad (4)$$

The synchronization state can be obtained by changing the sampling period Tp in such a way that $(T - Tp \cdot N) \rightarrow 0$. Then the angle defined by formula (4) tends toward $\pi/2$. A simplified angle control system is shown in figure 3. Only the real component of DFT is calculated and in this way the time-consuming calculation of the function arctan(φ) is omitted.

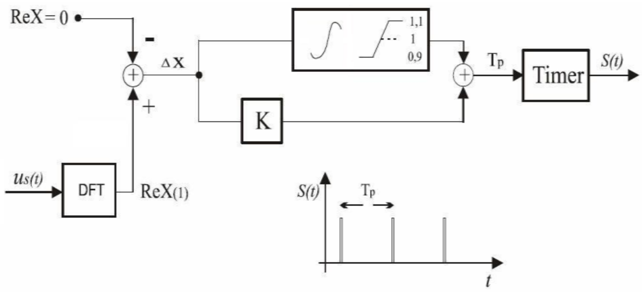

Fig. 3. A simplified synchronization circuit.

The output signal $S(t)$ is a synchronized time base common to all signal processing blocks in the digital controller.

4. Power converter topology

Already built prototype compensator consisted of the three independent one-phase multilevel cascaded inverters and its energy storage is based on high voltage stacked supercapacitors. There are three identical single phase compensators connected in a star as shown in figure 4.

Each single phase compensator is formed as a cascaded multilevel inverter built from two H- bridges units which are independently supplied. Simplified diagram of a single phase circuit is shown in Figure 5.

The energy exchange between the network and the supercapacitor is accomplished by the cascade inverter consisting of two H-bridge inverters connected in series and supplied by two DC/DC intermediary circuit converters (P1 and P2). The key K denotes a very fast switch placed between phase line and protected network. The switch is able to disconnect the load from the mains. Symbols C and RL denote parameters of the load. Most of time the switch K is closed allowing energy flow from the mains to load and to the compensator. It must be disconnected at the specific instant of voltage interruption or dip when the compensator takes over to power sensitive loads.

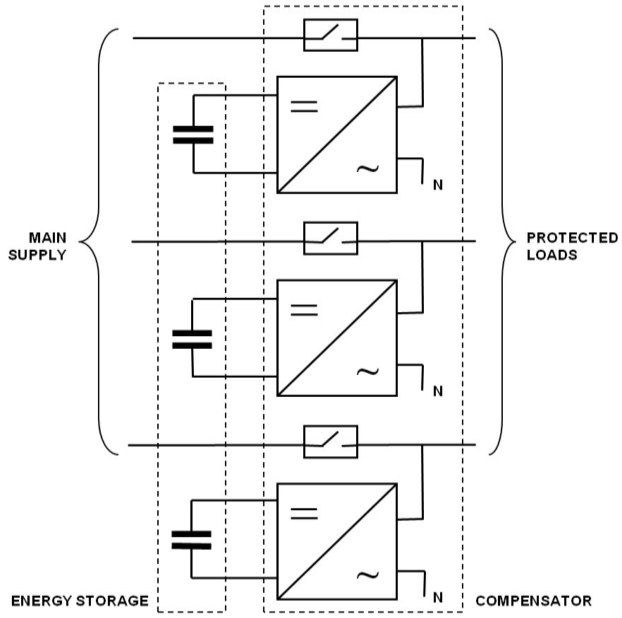

Fig. 4. Block diagram of the three-phase voltage outages compensator.

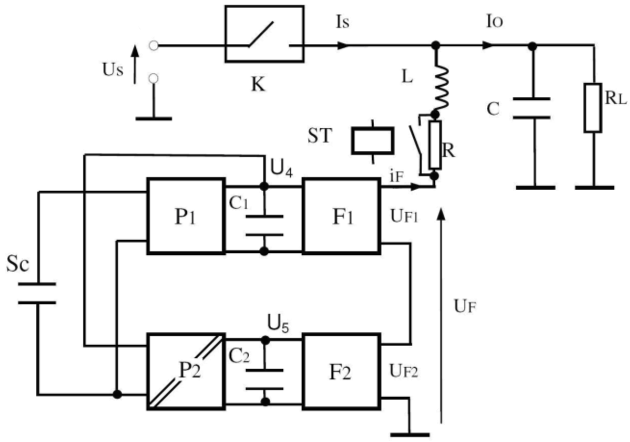

Fig. 5. A simplified diagram of the one phase of the three-phase voltage outages compensator.

The cascaded multilevel converter allows for low level THD factor in generated waveforms. When the supplying voltages ratio $U_1/U_2 = 1/3$ the available step voltage levels are as following:

$$\begin{cases} U = U_1 = \frac{1}{4} \\ U = U_2 - U_1 = \frac{1}{2} \\ U = U_2 = \frac{3}{4} \\ U = U_2 + U_1 = 1 \end{cases}$$

The output waveforms (phase and line-to-line) and their harmonic spectra are presented in fig. 6.

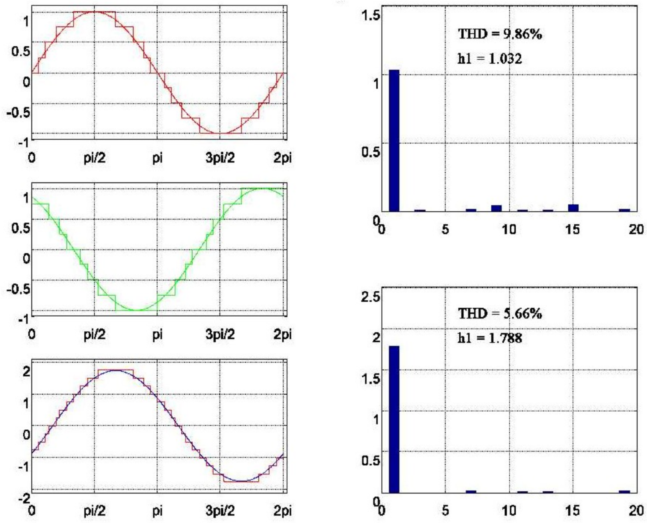

Fig. 6. Phase and line-to-line voltages and their spectral analysis.

The experimental results, presented in fig. 7 and 8 are in agreement with the predicted properties of the used multilevel cascade converter.

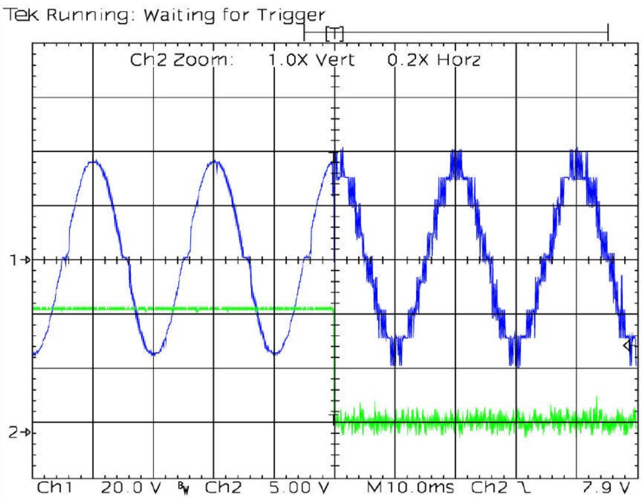

Fig. 7. Experimental waveforms showing the start of the voltage generation by the cascade inverter.

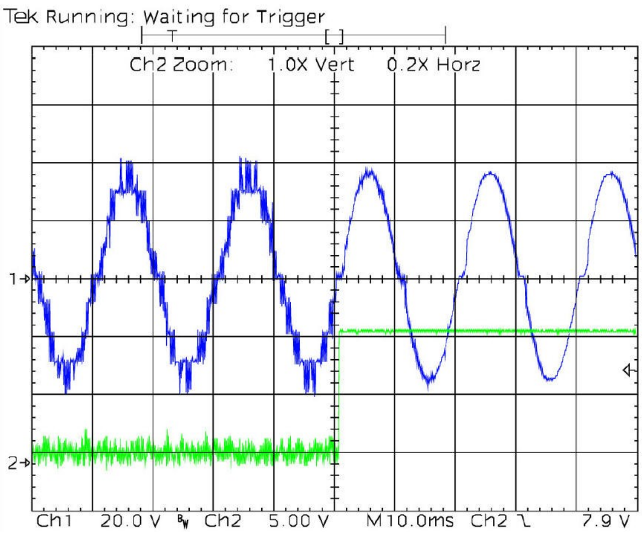

Fig. 8. Experimental waveforms showing the end of the voltage generation by the cascade inverter.

The figures above show the operation of the compensator in response to grid voltage disturbances. The fast switching from network to supercapacitor storage supply is shown in fig. 7 and back switching after restoring the network voltage is shown in fig. 8. The slight deformation of the obtained voltage around zero crossing points is caused by the properties of thyristor switch K at low voltage.

The multilevel cascade architecture used in medium power compensator is not the optimal topology for the developed high power compensator, due to the high price of the power switching components. So it is necessary to consideration somewhat simpler topology of the converter with lesser number of the active switching components. On this power level there are serious limitations on the switching frequency for the switching components and output waveforms of the typical two level PWM converter inevitably include high level of harmonic components, as presented in fig. 9.

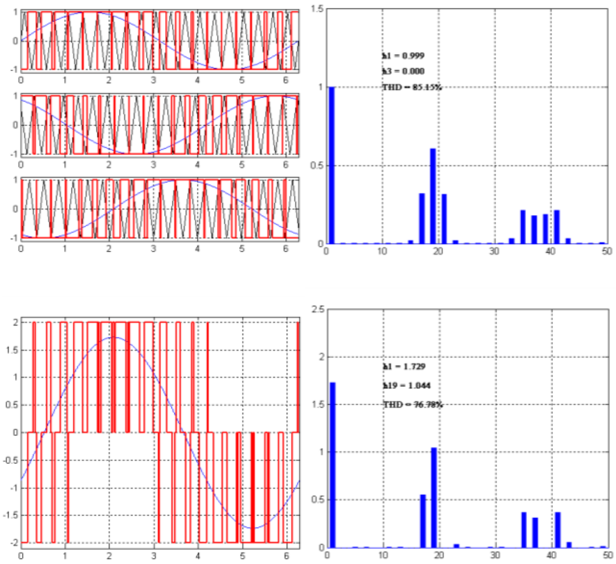

Fig. 9. Phase and line-to-line voltages and their spectral analysis for two level PWM converter with 1 kHz switching frequency.

Much better results can be obtained using three level converter. For this kind of converter the harmonic distortion is approximately two times lower. The simulation results are presented in fig. 10.

The three level PWM converter can be considered as the most suitable solution for high power compensator from technical as well as economical point of view. It consists of 12 switching transistors and 6 clamping diodes, while the H bridges of the previously used two stage cascade converter consist of 24 switching transistors.

The number of the switching components is in the middle between simple two level converter (6 transistors) and two stage cascade one (24 transistors).

Additional disadvantage of the considered solution with three level converter is that in this topology even if the voltage interruption appeared in only one phase it is necessary to generate all three phase voltages. There is no possibility to operate the phases independently – as was possible using the cascade converter.

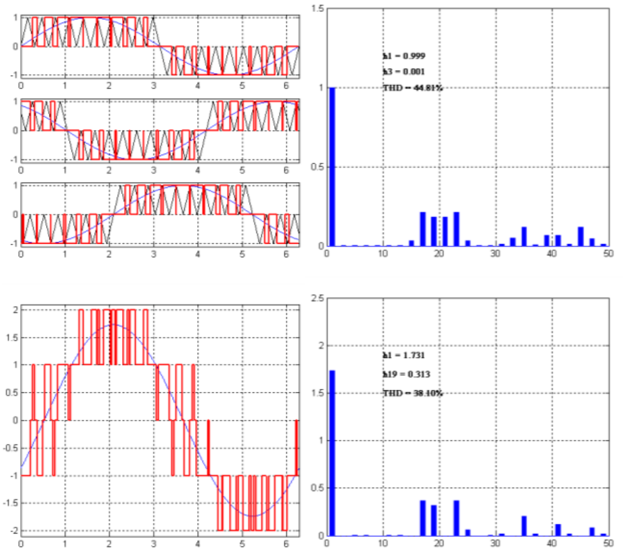

Fig. 10. Phase and line-to-line voltages and their spectral analysis for three level PWM converter with 1 kHz switching frequency.

Two different configuration versions have been considered for the new compensator. In the first version – presented in fig. 11 there are two additional DC/DC converters stabilizing the DC link voltages of the converter when the supercapacitors' voltage decreases during discharge in the active state of the compensator.

The second configuration without stabilizing converters is presented in fig. 12. In this version the appropriate level of the generated voltage will be obtained using the PWM modulation. The simulation works on using PWM technique for first harmonic stabilization have been carried out and the obtained results are highly promising assuming that the allowed discharge of the supercapacitors is in the range from nominal voltage to 0.5 nominal value. This discharge level means usage of 75 % of the stored energy:

$$E_{full} = \frac{U^2}{2}$$

and

$$E_{usable} = \frac{U^2 - \left(\frac{U}{2}\right)^2}{2} = \frac{\frac{3U^2}{4}}{2}$$

Anyhow the full discharge of the supercapacitors is not recommended by their manufacturers because it affects their life span.

The carried out tests proved that for modulation changing the amplitude of first harmonic in the range from 0.4 to 1.25 the level of the higher harmonic components is an the similar level, which means that properly adjusted low-pass filter can cope with the output waveforms quality within this range of PWM.

The version without additional DC/DC stabilizing converters is very interesting from economical and energy conversion efficiency point of view.

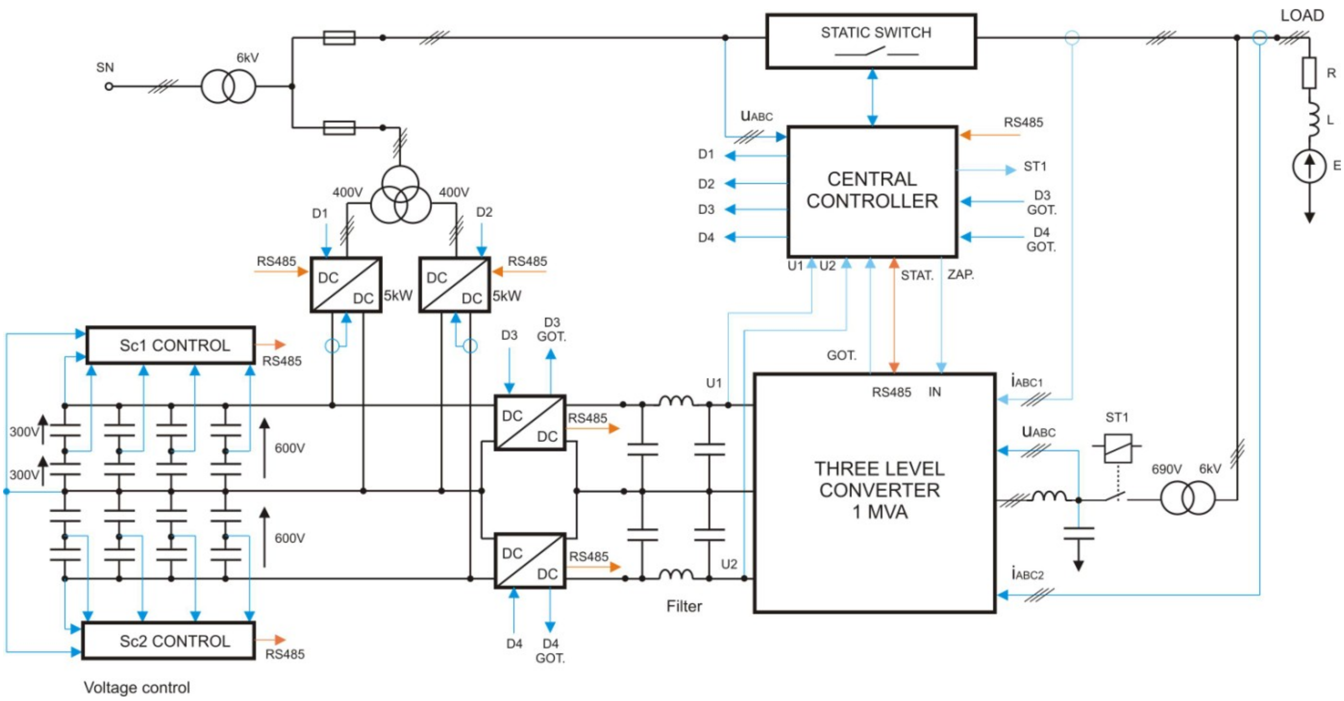

Fig. 11. Proposed structure of the high power compensator – version with stabilizing DC/DC converters.

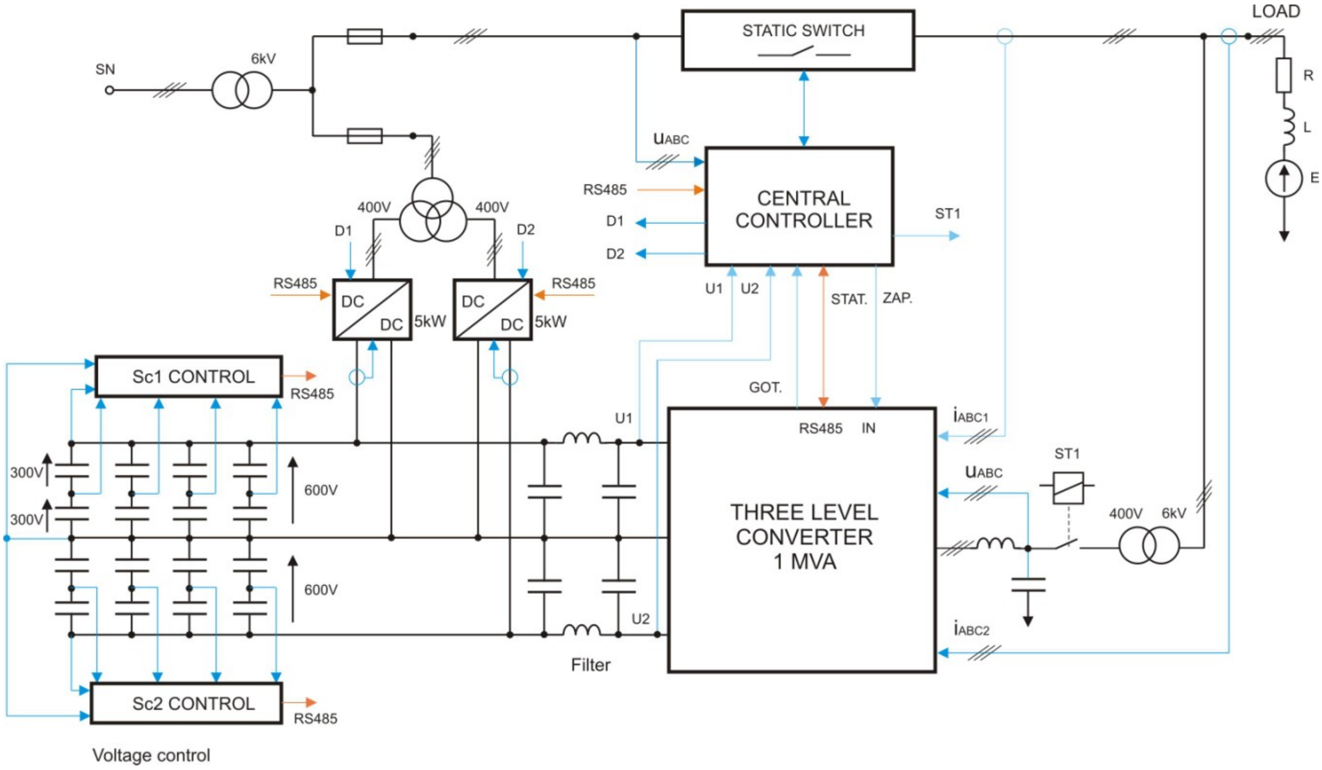

Fig. 12. Proposed structure of the high power compensator – version without stabilizing DC/DC converters.

The resulting output phase and line-to-line waveforms and their spectral analysis for U = 0.8 U_n are presented in fig. 13.

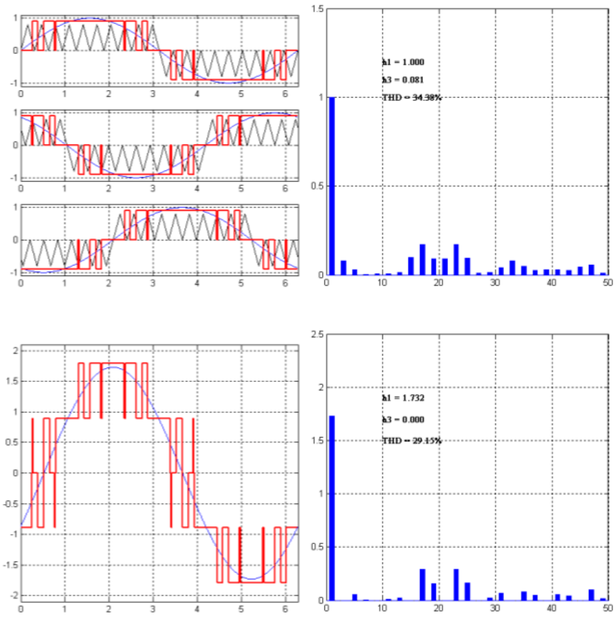

Fig. 13. Phase and line-to-line voltages and their spectral analysis for U = 0,8 U_n.

The resulting output phase and line-to-line waveforms and their spectral analysis for U = 2.5 U_n are presented in fig. 14.

The final choice of the version will be taken on the basis of the experimental results.

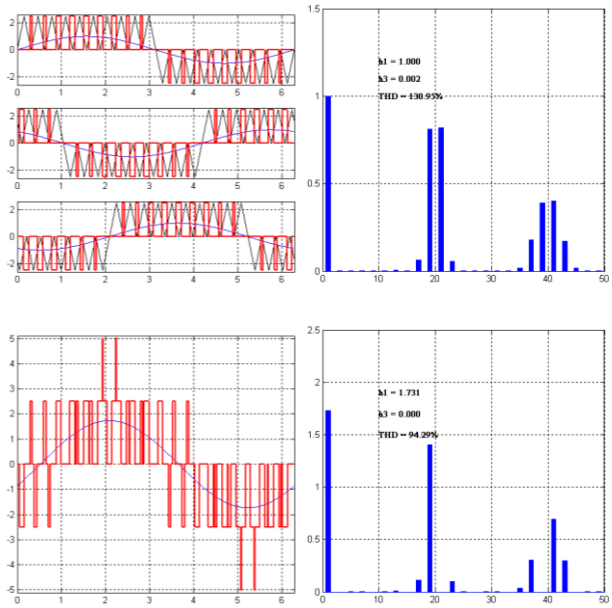

Fig. 14. Phase and line-to-line voltages and their spectral analysis for U = 2,5 U_n.

5. Operational algorithm of the compensator

The operation of the compensator requires realization of multiple concurrent real-time control tasks. In order to solve the complexity of these issues the finite-state machine (called a finite automaton) has been created in the controller of the compensator.

Six basic states of operation have been distinguished in the control algorithm:

STOP	off – no mains power.
CHARGE C2	device is powered and supply voltage (Us) is normal. Capacitor C_2 is charged to the nominal voltage.
CHARGE C1	device is powered and supply voltage (Us) is normal. Capacitor C_1 is charged to the nominal voltage.
WAIT	standby – waiting for dip or voltage outage
CHARGE Sc	charging the supercapacitor Sc in given compensator's phase. The charger raises and maintains the level of the supercapacitor voltage at U_{sc} = 300 V.
INVERTER	based on the energy stored in supercapacitor Sc phase voltage is generated using the cascade inverter. The device enters this state after the identification of voltage dip or power failure.

A simplified operating graph for the created finite-state machine with the conditions for transitions between states is presented in fig. 15.

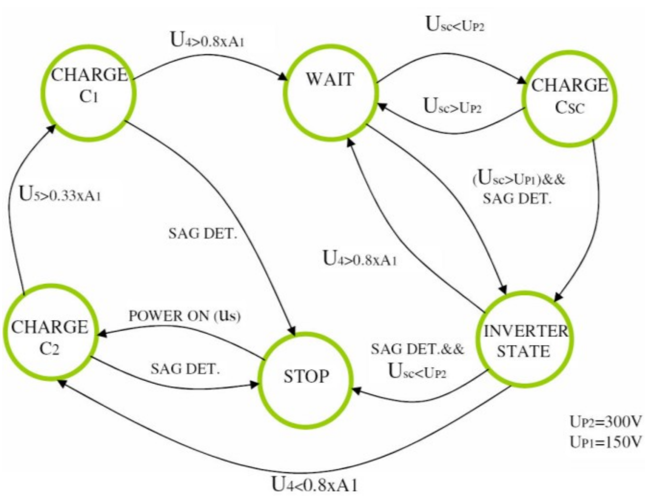

Fig. 14. A simplified graph of the operating states of the voltage compensator.

These conditions are discrete variables (logical states 0 or 1), obtained by simple comparisons or as the result of more complex calculations (dip detection – SAG_DET). Threshold values UP1 and UP2 determine supercapacitor working voltage range.

In addition to the grid voltage measurement, waveforms synchronization, compensating voltage generation and regulation of energy flows between the grid, energy storage and load, the controller also supports communication with higher level control system using local or wide area network.

6. Conclusions

A great and still escalating number of non-linear loads and growing share of energy from distributed resources result in decreasing the reliability of the public power grids. Therefore the issues related to the improvement of the quality and reliability of the electrical energy supply are particularly important.

The presented high power compensator proposal allows for compensating dips and short-term interruptions in medium voltage three-phase four-wire grid. The three level three phase converter with PWM modulation is considered as the most suitable power converter topology for the designed compensator. Using this technique it is probably possible to eliminate the additional DC/DC converters stabilizing the DC-link voltages in the main converter. The experimental tests will be carried out to proof this idea. The compensator energy storage is accomplished using the high voltage stacked supercapacitors. Their usage as energy storage devices in such application is very advantageous. Till now they are not practically implemented in energetic supply systems, mainly because this technology is not widely known yet and secondly because high voltage supercapacitors are still very expensive.

The observed rapid progress in supercapacitors' technology will undoubtedly lead to mass production of these components with better parameters and much lower price, which will allow the wide usage of supercapacitor based compensators for protection of the sensitive processes and devices against interruptions or voltage dips in supply networks or for suppressing disturbances in networks with disruptive sources.

Acknowledgement

The work was carried out under the Project INNOTECH-K1/IN1/56/158978/NCBR/12.

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https://doi.org/10.24084/repqj11.439

RE&PQJ, Vol.1, No.11, March 2013