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Software phase lock loops for pulse width modulated rectifiers

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Abstract. Simulation and experimental results of the use of three SPLL (Software PLL) that differ by the method of the detection of symmetrical grid voltage sequences (positive and negative ones) in case of an unsymmetrical grid voltage system with harmonics and under usual disturbances and parameter changes of the grid are presented. The function of the DSC (Delayed Signal Cancellation) based SPLL with $f_S = 1600$ Hz was experimentally verified under different grid voltage disturbances with satisfactory results.

Key words

Phase Lock Loop, unsymmetrical voltage system, PWM rectifier, Delayed Signal Cancellation, 56F807 development kit

1. Introduction

An effective synchronization of the control system of an electronic power converter to the grid voltage is a necessary condition of a reliable behaviour of the converter. The PLL (Phase-Lock Loop) should assure a good synchronization even in case of an unsymmetrical grid and/or presence of harmonics. It should assure also good transient responses in case of some grid disturbances. That is why a great attention has been focused on different PLL strategies in the last years.

Synchronization techniques can be sorted into two groups: those working in the open loop and other working in the closed loop. Generally, the open loop techniques are more sensitive to the disturbances mentioned above. The simplest example of these techniques is the ZCD (Zero-Crossing Detection). A basic closed look technique is SF-PLL (Synchronous Frame PLL) where the reference frame is synchronized by the vector of the grid three-phase voltage. In case of presence of some voltage harmonics the method works satisfactory only if band width is reduced that leads to increased settling times of transients. Undesirable effects of a negative grid voltage sequence (a pulsation of the dc capacitor voltage) can not be eliminated as well. Thus, the basic principle of more sophisticated methods is the synchronization of the reference frame with the positive grid voltage sequence of the fundamental frequency. Different methods differ in tools used for reaching this goal.

Four different basic techniques of the positive and negative grid voltage sequences detection and three grid current control strategies are theoretically and experimentally compared in [1]. The current control strategies differ in how they respect negative voltage sequences in the control structure. It has been found that from the point of view of precision, band width, and respective settling time the method DSC (Delayed Signal Cancellation) [2], [3] of the voltage symmetrical sequences separation provides the best results.

We will present here simulation and experimental results of the use of the SPLL (Software PLL) with DSC in case of an unsymmetrical grid voltage system with harmonics under usual disturbances and parameter changes of the grid. The discrete operation of the SPLL with DSC is considered for two different sampling periods (50 μs and 0.5 ms). So an IGBT- or IGCT- based MV (Medium Voltage) PWM rectifier with low switching frequency is supposed to be used.

Functions of other two feedback SPLL techniques that differ by the method of symmetrical grid voltage

sequences (positive and negative ones) detection are analyzed as well. From many methods published recently only those were selected which are suitable for three phase systems and do not need tuning of many parameters (like e.g. those with varying switching periods, with adaptive parameter tuning, with many low- or high-pass filters, etc.). Both the selected techniques have been more or less verified by simulations or experiments not only by their authors too.

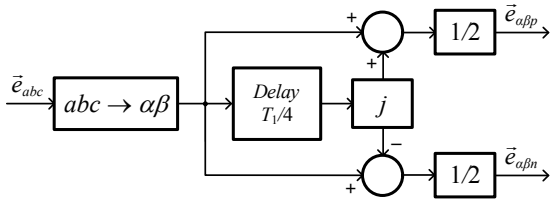


Fig.1 Block diagram of DSC (Delay Signal Cancellation)

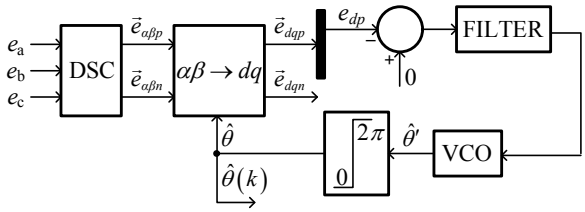


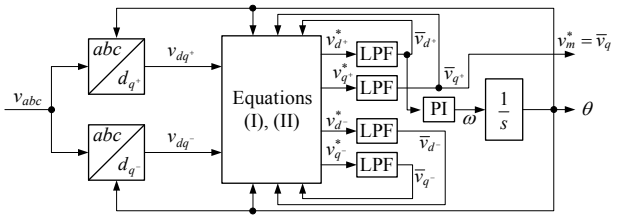
Fig.2 Block diagram of DSC-SPLL

2. Method DSC-PLL

The block diagram of the DSC is shown in Fig. 1 [3]. The block diagram of the DSC-PLL is presented in Fig. 2 [3].

3. Method DDSRF-PLL

The block diagram is in Fig. 3 [4] where the equations (I), (II) are presented too. The scheme is in line with the notation introduced in [1] where the axis q of the reference system oriented by the grid voltage vector.



$$\begin{bmatrix} v^*_{d^+} \\ v^*_{q^+} \end{bmatrix} = \begin{bmatrix} v_{d^+} \\ v_{q^+} \end{bmatrix} - \begin{bmatrix} \cos 2\theta & \sin 2\theta \\ -\sin 2\theta & \cos 2\theta \end{bmatrix} \begin{bmatrix} \bar{v}_{d^-} \\ \bar{v}_{q^-} \end{bmatrix} \quad \text{(I)}$$

$$\begin{bmatrix} v^*_{d^-} \\ v^*_{q^-} \end{bmatrix} = \begin{bmatrix} v_{d^-} \\ v_{q^-} \end{bmatrix} - \begin{bmatrix} \cos(-2\theta) & \sin(-2\theta) \\ -\sin(-2\theta) & \cos(-2\theta) \end{bmatrix} \begin{bmatrix} \bar{v}_{d^+} \\ \bar{v}_{q^+} \end{bmatrix} \quad \text{(II)}$$

Fig.3 Block diagram of DDSFR-PLL

4. Method VAVGF-PLL

The block diagram of the Variable Average Frequency-PLL (VAVGF-PLL) method is in Fig. 4 [5]. The scheme is a modified method SF-PLL with the addition of the block of the digital average value DAVG (in the interval of the fundamental period $\bar{f}$).

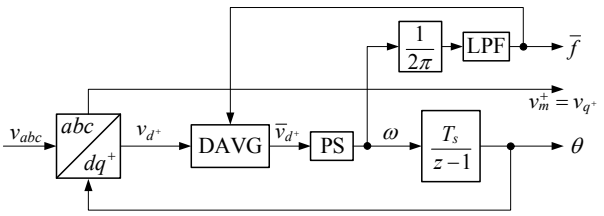


Fig.4 Block diagram of VAVGF-PLL

5. SPLL simulation

The behaviour of all three PLL methods (DSC, DDSFR, and VAVGF) under different states of the grid voltage three phase system was simulated in the Matlab/SimulinkTM environment.

The following transients were simulated:

1) voltage magnitude change by 20 % (in all three phases)
2) presence of the negative voltage component of the magnitude 10%
3) step change of the frequency by 2 Hz
4) step change of the voltage vector phase by 30 %
5) presence of the 5th and 7th voltage harmonics of the magnitude of 10 %
6) start of the PLL for 0º and 180º initial phase error between real and expected grid voltage vector.

All these simulations were done for $T_S = 0.05$ ms and $T_S = 0.5$ ms, which corresponds to the sampling periods of the discrete PLL $f_S = 20$ kHz and 2 kHz, respectively.

For the VAVGF method the function of the algorithm without the block DAVG was simulated as well. Without this block the method VAVGF is actually the basic variant SF-PLL (see introduction) that does not respect and does not rectify at all the negative sequence and/or harmonics in the grid voltage system. The simulations were done for the following parameters of the PI type compensator: $K_P = 0.006$, $K_I = 0.15$ ($T_I = K_P / K_I = 0.04$ s) when all free methods are working (e.g. Fig. 5) and for higher values of $K_P = 0.05$, $K_I = 25$ ($T_I = 0.002$ s) when the method VAVGF fails and thus only the DSC and DDSFR methods are compared (e.g. Fig. 6).

Applying the negative voltage sequence, the least phase error $\Delta\Theta$ between the real and estimated grid voltage vector is obtained by using the method DSC, while the remaining two methods DDSFR and VAVGF yield comparable results with approximately two times higher amplitudes and settling times. It stands to reason that the VAVGF strategy without the DAVG block does not filtrate the negative voltage sequence at all. The system behaviour is not practically influenced by the magnitude of the sampling period (in the mention ranges), while an

increasing gain of the PI compensator leads to shorter settling times with higher frequencies of pulsation.

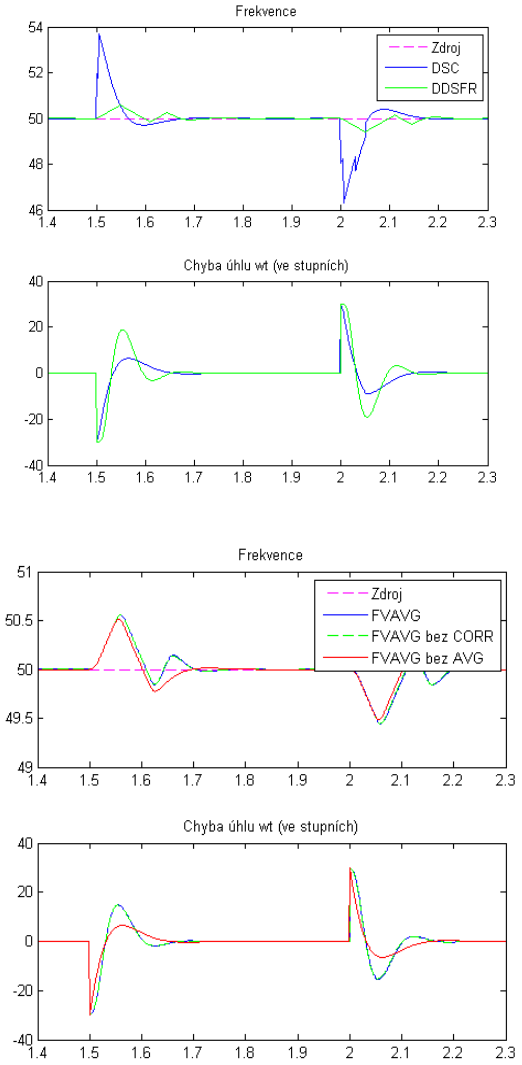


Fig. 5 Estimated frequency (Hz) and phase angle error (deg) for phase change by 30° (sampling period $T_S = 0.05$ ms);
$K_P = 0.006$, $K_I = 0.15$ ($T_I = K_P / K_I = 0.04$ s);
{Grid-pink dashed, DSC-blue, DDSFR-green
VAVGF-green dashed, VAVGF without DAVG-red}

If the grid voltage system contains some harmonics, all the methods yield similar results for lower gains of the PI compensator of the PLL, but for higher gains some un-dumped low amplitude oscillations of $\Delta\Theta$ (circa 1º) appear if the DDSFR method is used. This is not the case of the DSC method.

The most difficult task for the SPLL is a phase change of the grid voltage vector (Figs. 5, 6). All the methods provide similar results. But, for high gains of the PI compensator of the PLL the error $\Delta\Theta$ reaches its steady state faster for the DSC method then for the DDSFR method and this effect is more profound with longer sampling intervals (Fig. 6).

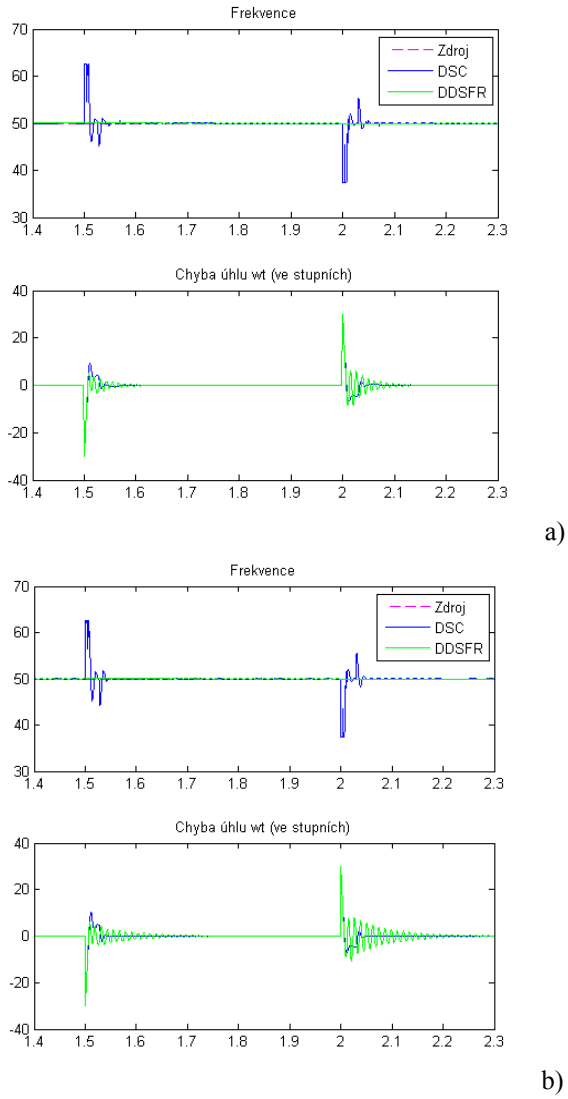


Fig. 6 Estimated frequency (Hz) and phase angle error (deg) for phase change by 30°; $T_S = 0.05$ ms (a), 0.5 ms (b);
$K_P = 0.05$, $K_I = 25$ ($T_I = 0.002$ s);
{Grid-pink dashed, DSC-blue, DDSFR-green}

6. PWM rectifier simulation and measurement

The detailed model of a 4-level Capacitor Clamped Inverter (CCI) based MV PWM rectifier has been developed in the Matlab/Simulink™ environment. The laboratory model of the same PWM rectifier has been realized as well (3×230V/400V, 4 kVA, IGBTs IXYS with $I_c = 100$ A and $U_{ces} = 1200$ V , CT-Concept Technologie AG, switching frequency $f_S = 1600$ Hz).

A control algorithm has been realized by using the 56F807 development kit with the Code Varior environment and program Freemaster.

Some tests of the DSC-SPLL implemented are presented in Figs. 7-12 (contrary to the theory and simulation results presented up to now, q voltage component was nullified to put the grid voltage vector in the line with the d axis here).

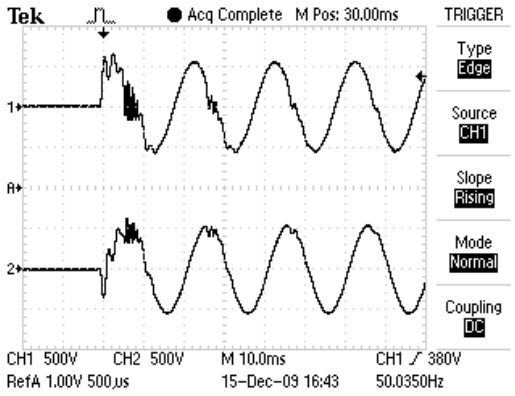


Fig. 7 Captured time responses of switched grid line-to-line voltages on: v_{ab}, v_{ca} (500 V/div), 10 ms/div

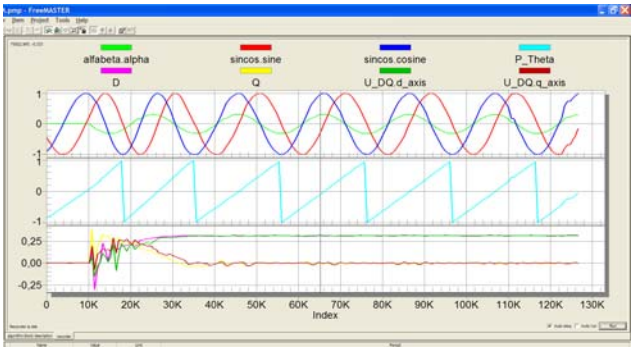


Fig. 8 Captured time responses after switching grid voltage on: a) upper part: grid voltage component v_a (1000 V/div), sinΘ, cosΘ; b) middle part: angle Θ (π /div); c) lower part: grid voltage components v_d , v_q (250 V/div) - time scale 10 ms/div

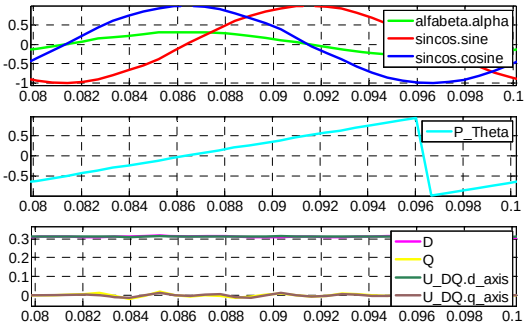


Fig. 9 Zoom of Fig. 8 in steady-state: a) upper part: grid voltage component v_a (500 V/div), sinΘ, cosΘ; b) middle part: angle Θ (π /2/div); c) lower part: grid voltage components v_d , v_q (100 V/div) - time scale 2 ms/div

First, the behaviour of the DSC-SPLL after the grid voltage switched on has been studied. Fig. 7 shows captured time responses of switched grid line-to-line voltages v_{ab}, v_{ca} on. Note that the first two voltage periods are substantially deformed due to the switching process. So, some unfavourable impact of these high frequency transients on the DSC-SPLL function can be expected.

Fig 8 presents captured time responses of some characteristic variables of the DSC-SPLL after switching grid voltage on. Fig. 9 shows the zoom of Fig. 8 in the steady-state. The DSC-SPLL algorithm ran before the voltage switching with the generation of the angle Θ (and the respective functions sinΘ, cosΘ) independently to the real grid voltage vector. We see that synchronization of the DSC-SPLL (v_d is constant, $v_q = 0$) to this grid voltage vector is reached in 1.5-2 fundamental periods, although the generated function cosΘ of the non-synchronized DSC-SPLL at the instant of switching grid voltage on was at its maximum, while the voltage component v_a was at zero and headed to negative values.

The next Figs. 10-12 show some time responses after changing the grid voltage in an unbalanced form: negative sequence = 35% of the positive one was applied (in the opposite phase) and positive sequence was decreased also by 35% at the same time.

Figs. 10 and 11 present simulated time responses. In Fig. 10, lower part, two pairs of d, q grid voltage components are depicted: v_d, v_q of the real grid voltage and v_d^+ , v_q^+ of the extracted positive symmetrical voltage sequence only, which are used in the DSC-SPLL algorithm to synchronize the controller to the grid.

Fig. 11 shows the respective simulated time responses of the 4-level CCI based MV PWM rectifier: the dc voltage component v_{dc}, grid currents i_{sa}, i_{sb}, i_{sc}, and the PWM rectifier phase voltage v_a and current i_a.

Fig. 12 presents captured time responses of the DSC-SPLL variables under the same conditions as those in Fig. 10. Again, similar high frequency disturbances at the instant of a voltage system change as those shown in Fig. 7 influenced the time responses of the DSC-SPLL. Nevertheless, even by this dramatic voltage change, the synchronization was reached in circa half of fundamental period (that is, the components v_d^+ , v_q^+ were again constant).

7. Conclusion

Generally speaking, if the magnitude of the three phase grid voltage is changing and/or the system contains a negative voltage sequence or voltage harmonics, then the DSC method provides the best results. The most difficult task for the SPLL is a phase change of the grid voltage vector. Here, all the methods provide similar results.

For such changes in the frequency when $T_1/T_S = 1/(f_1 T_S)$ is not an integer the DSC method leads to a permanent steady state error of $\Delta\Theta$ that increases with an increasing sampling period (for $T_S = 0.5$ ms , that is $f_S = 2000$ Hz , the error reaches $\Delta\Theta \approx 2°$). It is due to the discrete delay block (Fig. 1) where the real delay $T_1/4$ is only approximated by an integer amount of T_S.

Nevertheless, from all three methods analyzed here the DSC method can be recommended as the best one.

The function of the DSC-SPLL with $f_S = 1600$ Hz was experimentally verified under different grid voltage disturbances with satisfactory results.

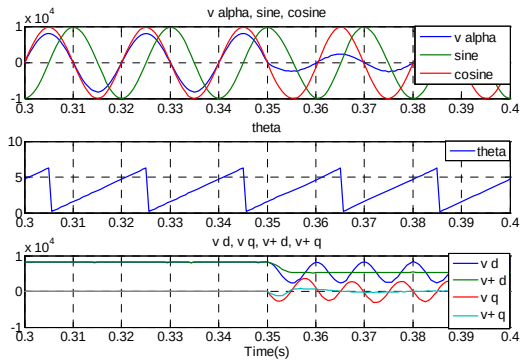


Fig. 10 Simulated time responses after changing grid voltage in unbalanced form: a) upper part: grid voltage component v_a (10000 V/div), $10^4 \sin\Theta$, $10^4 \cos\Theta$; b) middle part: angle Θ (5rad/div); c) lower part: grid voltage components v_d, v_q (10000 V/div) – time scale 10 ms/div

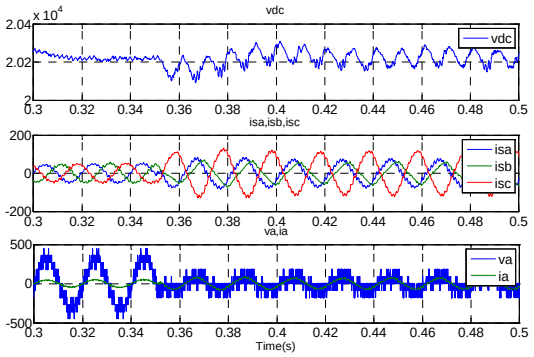


Fig. 11 Simulated time responses after changing grid voltage in unbalanced form: a) upper part: dc voltage component v_{dc} (200 V/div); b) middle part: grid currents i_{sa}, i_{sb}, i_{sc} (200 A/div); c) lower part: PWM rectifier phase voltage v_a and current i_a (10000 V/div, 500 A/div) – time scale 20 ms/div

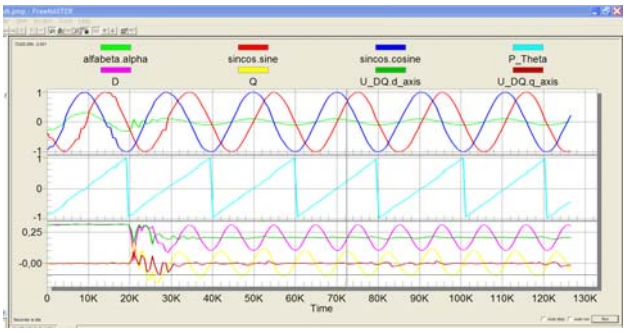


Fig. 12 Captured time responses after changing grid voltage in unbalanced form: a) upper part: grid voltage component v_a (1000 V/div), $\sin\Theta$, $\cos\Theta$; b) middle part: angle Θ (π/div); c) lower part: grid voltage components v_d, v_q (250 V/div) – time scale 10 ms/div

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