20th International Conference on Renewable Energies and Power Quality (ICREPQ'22)
Vigo (Spain), 27th to 29th July 2022
Renewable Energy and Power Quality Journal (RE&PQJ)
ISSN 2172-038 X, Volume No.20, September 2022

Adaptive Dead Time Compensation for Continuous Cross-Period Single Phase-Shift Control of Dual Active Bridge Converters

Szabolcs Veréb, András Futó, Zoltán Sütő, Attila Balogh and István Varjasi

Department of Automation and Applied Informatics
Faculty of Electrical Engineering and Informatics
Budapest University of Technology and Economics
Műegyetem rkp. 3., H-1111 Budapest, Hungary
Phone number: +36 (1) 463-1552, e-mail: szabolcs.vereb@edu.bme.hu

Abstract. The load transient response of a power converter is an important property, especially in a test equipment application. The dynamic behavior of a dual active bridge converter mainly depends on the switching frequency, the transformer leakage inductance, and the capacitor bank size. Using the Continuous Cross-Period Single Phase-Shift control, an excellent load transient response can be achieved without the need for expensive hardware components. However, in practical applications, the switch delay and the required inserted dead time distort the current waveform, increasing the electromagnetic noise and reducing the effectiveness of the regulation. In this paper, an adaptive dead time compensation technique is presented, which eliminates such phenomenon. The effects of dead time are analyzed, and mathematical formulas are derived, from which the adaptive compensation technique is formalized. The algorithm is implemented on a TMS320F28075 DSP and tested in a HIL environment. The study revealed that the proposed adaptive technique could mitigate the current waveform distortions.

Key words. control, dead time, DAB converter, power conversion

1. Introduction

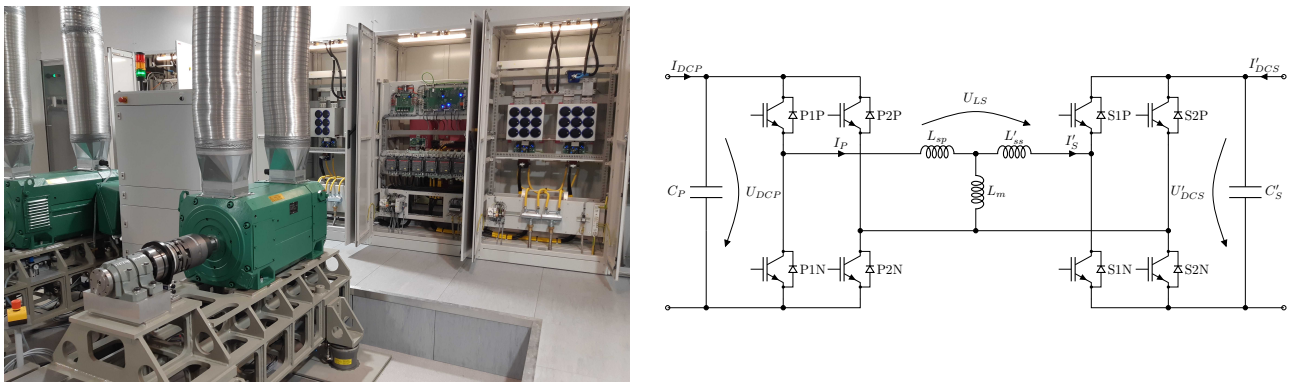
Nowadays, automobile manufacturers are shifting their focus on electric drivetrain to allow more environmentally friendly private transportation around the world. The design process of such systems can be challenging. New automotive standards are emerging, which require complex test procedures. The Modular Hybrid Drive System (MHDS) Laboratory was built at the Budapest University of Technology and Economics to allow electric drivetrain signal and power level testing. This laboratory includes various built-in high power converters, one of them is a 360 kW nominal power dual-active-bridge (DAB) converter (Fig. 1).

The DAB topology is a bidirectional, isolated DC-to-DC converter, which was proposed [1] and patented [2] in 1991. The power circuit is built up from a two-coil transformer driven by full-bridges, as shown in Fig. 1b. The leakage inductance of the transformer plays a key role in the converter operation [3].

Various control methods have been introduced for the DAB converter topology recently. The commonly used single phase-shift (SPS) control is the simplest. The full-bridges are driving the transformer with 50% duty cycle square waves [1], and the required power flow can be regulated through the phase-shift between them [3]. The converter efficiency can be increased by reducing the circulating power and by having a wider ZVS region [4]. Further improvements could be achieved with more advanced techniques, such as the double phase-shift (DPS) [5] and triple phase-shift (TPS) [6] control. However, these have more degrees of freedom in the regulation parameters, which may complicate the practical implementation.

In a high-power electric drivetrain test facility, galvanic isolation is essential, which can be implemented with the DAB topology. The most recent publications are focusing on physical size reduction by increased switching frequency [7] [8] and on efficiency enhancement [9] [10] [11]. In a test equipment application, the transient response is an important property seldom considered in papers.

A good transient behavior can be characterized by a fast, voltage overshoot, and overcurrent free disturbance response. The required characteristics can be achieved by utilizing a large capacitor bank, a higher switching frequency, and a transformer with low leakage inductance. High-frequency transformer cores, which are suitable for high-power applications, are expensive and hard to manufacture.



(a) (b)

Fig. 1. The $360kW$ DAB converter in the MHDS laboratory and its power circuit diagram.

In the MHDS laboratory, as a cost-effective solution, a laminated steel core transformer was chosen, which operates at 400 Hz. Lowering the switching frequency to this extent would result in a large and expensive capacitor bank if an excellent dynamic behavior is required.

To improve the transient behavior, the authors have researched the Continuous Cross-Period Single Phase Shift (CCP-SPS) control technique [12]. It is suitable for such low-frequency applications. A good transient behavior can be achieved without the need for large capacitor banks. However, the effective switch delay has a great impact on the operation, which is inevitable in practice. In this paper, the effects of switch delay and inserted dead time are analyzed, and an adaptive compensation method is presented, which can mitigate the unwanted phenomena.

In Section 2 the main equations of the dead time effects are formalized. The adaptive compensation technique is presented in Section 3. The HIL simulation results of the proposed control algorithm are shown in Section 4.

2. Dead time effects

The following analysis is based on a few assumptions to simplify the complex nature of half-bridge switching waveforms. First, each half-bridge output voltage is assumed to be an ideal square wave with zero rise and fall time. Second, the timing of the output voltage edge depends on the top and bottom semiconductor gate signal, the half-bridge output current direction, the semiconductor switch on-delay (t_{on}) and off-delay (t_{off}), and the inserted dead time (t_d). Third, the t_{on} and t_{off} delays are considered equal among all semiconductor switches.

The CCP-SPS control improves the DAB converter dynamic behavior (compared to the SPS control) by introducing four additional switching actions during a switching period without increasing the transformer magnetizing current fundamental frequency [12]. The possible switching actions and the resulting waveforms are shown in Fig. 2. The fundamental switching time period (T_{SPS}) is divided into six T_{CCP} long durations, so-called phases, marked with PH1-PH6.

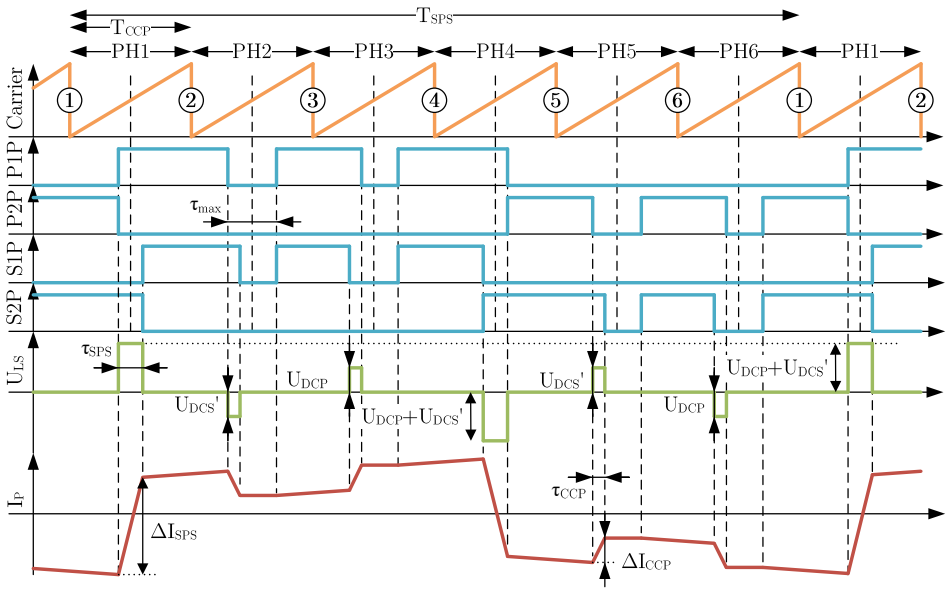
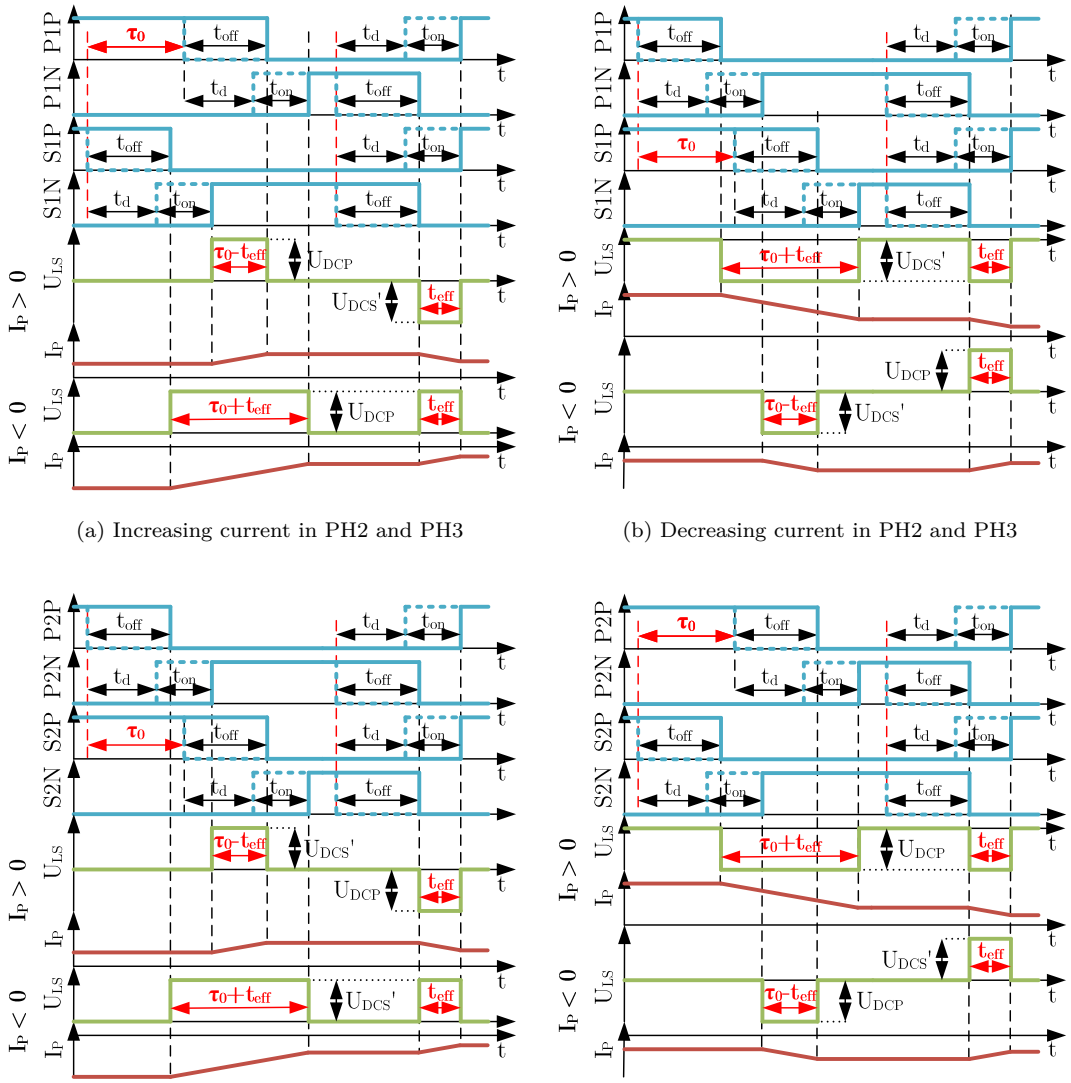


Fig. 2. CCP-SPS control resulting waveform illustrating possible in-period transformer current modifications.



(a) Increasing current in PH2 and PH3

(b) Decreasing current in PH2 and PH3

(c) Increasing current in PH5 and PH6

(d) Decreasing current in PH5 and PH6

Fig. 3. Effects of dead time during CCP-SPS control in various circumstances.

The switching actions in PH1 and PH4 are creating the single phase-shift between the transformer primary and secondary side square wave voltages. In such events, the effects of dead time depend on the current level as described in [13]. In continuous current conduction mode (CCM), the original voltage-time product on the transformer leakage inductance does not change but shifts with t_{off} in time. Discontinuous current conduction mode (DCM) may occur during light load conditions. In such a case, the voltage-time product of U_{LS} depends on the switch delays, inserted dead time, and other system parameters. As DCM may be present in steady-state operation, the adaptive dead time compensation is necessary for PH1 and PH4 phases.

In-period switching actions in PH2, PH3, PH5, and PH6 are used to change the current by shorting both coils for different amounts of time. The shorting-time difference (τ_{CCP}) defines the length of the voltage pulse on the leakage inductance. In PH2 and PH3 the current can be increased or decreased by switching the P1 and S1 half-bridges as shown in Fig. 3a and Fig. 3b respectively. Similarly, the current can be increased or decreased in PH5 and PH6 by switching the P2 and S2 half-bridges, Fig. 3c and Fig. 3d shows examples of such actions.

The effects of the dead time depend on the actual phase, the current polarity, and the direction of change. We can observe patterns in the voltage across the transformer leakage inductance (U_{LS}). During switching actions, two voltage pulses are created. The first one can be longer or shorter by t_{eff} than the intended pulse length (τ_0). The length of the second one is always t_{eff}. This time duration is called the effective dead time. It is the result of the switch delays and inserted dead time. It can be calculated as shown in equation (1).

$$t_{eff} = t_d + t_{on} - t_{off} \tag{1}$$

If the first pulse is the longer, then the second one's voltage amplitude always matches the first one's. If the first pulse is the shorter, then the second one's voltage amplitude has an opposite polarity, and its absolute value equals to the DC voltage on the other side of the transformer. Considering that the DC voltages are balanced during steady state operation ($U_{DCP} = U'_{DCS} = U_{DC}$), the voltage-time product (VT) of the leakage inductance can be summarized in equations (2) and (3) for all possible switching actions. The value of p can be 1 or -1 depending on the switching phase, current polarity, and change direction.

$$VT_U = p \cdot U_{DC} \cdot (\tau_0 + 2 \cdot t_{eff}) \quad (2)$$

$$VT_D = p \cdot U_{DC} \cdot (\tau_0 - 2 \cdot t_{eff}) \quad (3)$$

It is clear that due to the $\pm 2 \cdot t_{eff}$ components the transformer current change will be higher or lower, which results with issues during the CCP-SPS control operation.

3. Adaptive compensation

One could argue that if the right amount of inserted dead time is used ($t_d = t_{off} - t_{on}$), then the effective deadtime would become zero. The inserted dead time is needed to prevent shoot-through switching events. The switch delays are not constant parameters. Their values depend on the temperature, the current and voltage level, the age of the converter, etc. Thus, the inserted dead time must be high enough to compensate for these effects.

The proposed compensation technique is based on a simple idea. The pulse length reference can be shortened or lengthened by a τ_c duration to cancel out the effective dead time.

$$VT = p \cdot U_{DC} \cdot ((\tau_0 \mp \tau_c) \pm 2 \cdot t_{eff}) \quad (4)$$

The required compensation time (τ_c) is the sum of two separate components.

$$VT = p \cdot U_{DC} \cdot ((\tau_0 \mp (2 \cdot \tilde{t}_{eff} + \tau_a)) \pm 2 \cdot t_{eff}) \quad (5)$$

The first one is the estimated effective dead time ($\tilde{t}_{eff}$), which is a constant and represents an initial guess. The other one (τ_a) implements the adaptability of the method as the following.

In each phase, the transformer primary and secondary side current is sampled before and after a switching action as shown in Fig. 4. From that, the measured average transformer current change (ΔI_{meas}) is calculated.

$$\Delta I_{meas} = \frac{I_P(A) + I'_S(A)}{2} - \frac{I_P(B) + I'_S(B)}{2} \quad (6)$$

This value is compared to the output of the current change requested by the voltage controller (ΔI_{ref}) [12]. The average current error (ΔI_{err}) is calculated and stored for each phase separately.

Before the next switching action, in the same phase, this calculated error value is multiplied with a constant

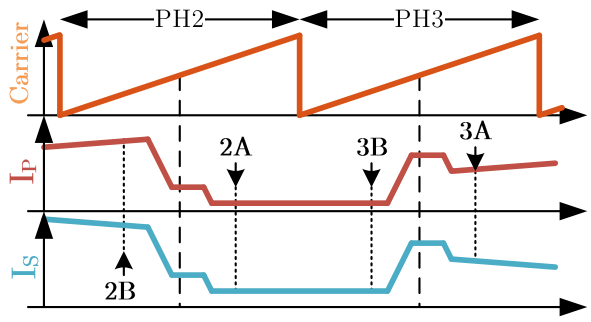


Fig. 4. The transformer current sampling points for the adaptive controller, in the PH2 and PH3 phases before (2B, 3B) and after (2A, 3A) the switching action.

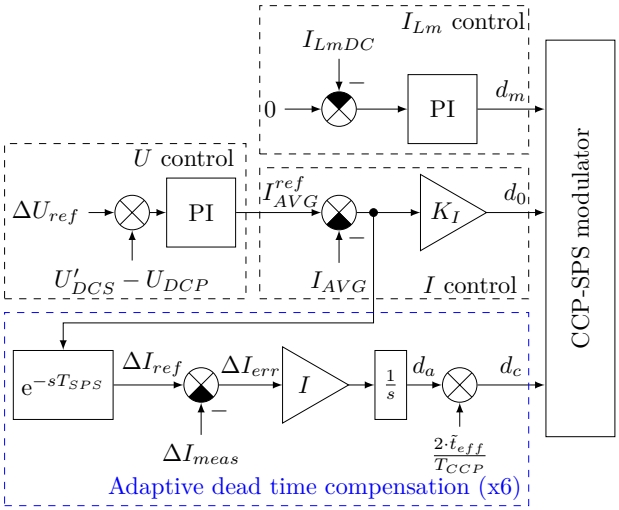


Fig. 5. The control diagram of the Continuous Cross-Period Single Phase Shift algorithm with adaptive dead time compenastion.

(I) and fed into an integrator, of which output is used as the τ_a value for the respective phase. In other words, the six integrators are learning how much longer or shorter pulses are necessary in each phase to have no difference between the requested and the measured average transformer current.

The control diagram of the CCP-SPS algorithm, extended with the adaptive dead time compensation logic, is shown in Fig. 5. Note that the controller output (d_c) has no unit. This can be interpreted as if τ_c would be divided by the time period of the PWM carrier signal. Similar logic could be applied to the integrator output (d_a).

Due to the τ_c compensation time, the CCP-SPS modulator switching table has to be changed accordingly. The required modifications are shown in Tab. I, which is based on the original CCP-SPS switching table published in [12]. Note that d_{cx} appears multiple times in one column, thus it has an effect on the switching behavior at the beginning and at the end of each switching action. This is required to get rid of the second U_{LS} pulse (see in Fig. 3).

Table I - The switching table of the CCP-SPS modulator with dead time compensation. d_{cx} is the adaptive controller output (d_c) for the respective phase (d_{c1} for PH1, d_{c2} for PH2, etc.). The compare values are suitable for a unity amplitude sawtooth carrier signal based PWM generator.

Switching action	PH1	PH2 and PH3		PH5 and PH6		PH4
		$I_{err} > 0$	$I_{err} \leq 0$	$I_{err} > 0$	$I_{err} \leq 0$	
P1 to U_{DCP}	$\frac{1-d_0-\mathbf{d_{cx}}}{2} - d_m$	$\frac{1+d_{max}-\mathbf{d_{cx}}}{2}$	$\frac{1+d_{max}-\mathbf{d_{cx}}}{2}$	x	x	x
P1 to 0	x	$\frac{1-d_{max}+\mathbf{d_{cx}}}{2} + d_0$	$\frac{1-d_{max}}{2}$	x	x	$\frac{1-d_0-\mathbf{d_{cx}}}{2} + d_m$
P2 to U_{DCP}	x	x	x	$\frac{1+d_{max}-\mathbf{d_{cx}}}{2}$	$\frac{1+d_{max}-\mathbf{d_{cx}}}{2}$	$\frac{1-d_0-\mathbf{d_{cx}}}{2} + d_m$
P2 to 0	$\frac{1-d_0-\mathbf{d_{cx}}}{2} - d_m$	x	x	$\frac{1-d_{max}+\mathbf{d_{cx}}}{2} + d_0$	$\frac{1-d_{max}}{2}$	x
S1 to U_{DCS}	$\frac{1+d_0+\mathbf{d_{cx}}}{2} - d_m$	$\frac{1+d_{max}}{2}$	$\frac{1+d_{max}}{2}$	x	x	x
S1 to 0	x	$\frac{1-d_{max}}{2}$	$\frac{1-d_{max}-\mathbf{d_{cx}}}{2} + d_0$	x	x	$\frac{1+d_0+\mathbf{d_{cx}}}{2} + d_m$
S2 to U_{DCS}	x	x	x	$\frac{1+d_{max}}{2}$	$\frac{1+d_{max}}{2}$	$\frac{1+d_0+\mathbf{d_{cx}}}{2} + d_m$
S2 to 0	$\frac{1+d_0+\mathbf{d_{cx}}}{2} - d_m$	x	x	$\frac{1-d_{max}}{2}$	$\frac{1-d_{max}-\mathbf{d_{cx}}}{2} + d_0$	x

4. HIL simulation

A HIL simulation system was utilized to test the proposed adaptive dead time compensation logic.

The control loops were implemented on a Texas Instruments TMS320F28075 DSP. The transformer currents and DC voltages are sampled multiple times in a switching period. For the adaptive control, the transformer current sampling points are dynamically calculated as shown in Fig. 4. For the voltage and current regulators, the required analog measurements are triggered at the start of each control phase (PHx), in other words, when the PWM carrier signal is reset to zero (see the numbered circles on Fig. 2). The control logic is running after the completion of these ADC conversions, and the new switching actions are actuated in the same phase. The tuning and implementation of the digital control loop were done as described in [12]. The I parameter of the adaptive dead time compensation integrators was set to 4 %/kAs, which gave a good balance between settling time and measurement noise sensitivity.

An extended model of the power circuit (as shown in Fig. 6) was created in MATLAB Simulink and compiled to a Xilinx Zynq-7000 SoC powered development board. The half-bridges were implemented with the switching function model as described in [14]. The switch delay were taken into account with a simple delay in the input PWM signals with a turn-off time of $t_{off} = 3\,\mu s$ and with a turn-on time of $t_{on} = 2\,\mu s$. These values are adjustable during runtime. The rest of the model was implemented based on the differential equations of the circuit. The discrete-time integrators were realized based on the forward Euler method.

The goal of the simulation is to verify the adaptability of the proposed control technique. To verify its behavior, the turn-off time was changed from the nominal $t_{off} = 3\,\mu s$ to $t_{off} = 40\,ns$ while the converter was running with the applied 300 A load.

The adaptive controller was configured with a specific $\tilde{t}_{eff}$ value to assume the 3 µs turn-off time. Therefore, the integrator output (d_a) is expected to be around zero when the turn-off time is set to 3 µs. When it is changed to 40 ns, the output of the integrator should change as well. The expected d_a value can be estimated with the following equation, based on (5).

$$d_a = \pm 2 \cdot \frac{\tilde{t}_{off} - t_{off}}{T_{CCP}} = 1.42\,\% \tag{7}$$

During the transient, debugging tools were used to record the transformer current and the PH2 adaptive controller variables. No analog measurements were necessary to collect the simulation data. The respective digital values were read directly from the SoC and DSP memory. This method was chosen deliberately to avoid measurement errors.

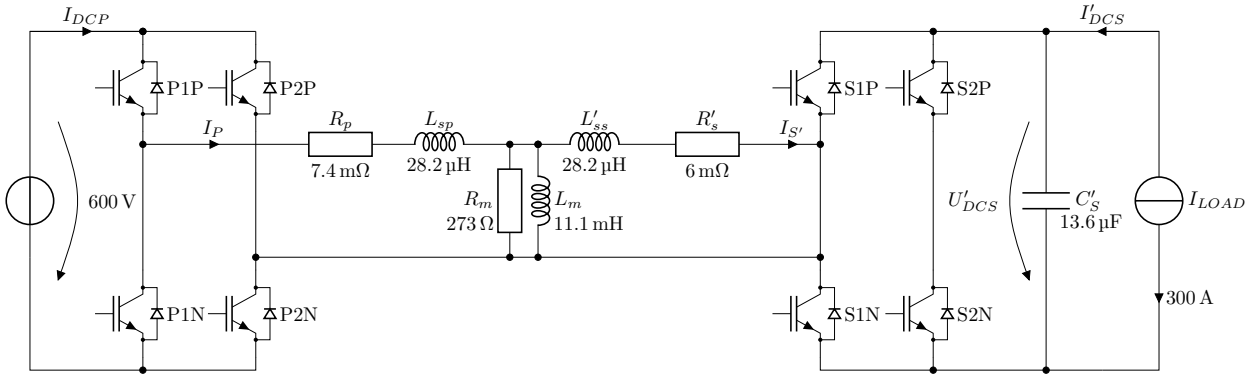


Fig. 6. Power circuit schematic diagram used in the HIL simulation.

5. Results

The simulation results are shown in Fig. 7 and Fig. 8. The figures are only focusing on the PH2 phase to limit the number of plotted waveforms. The turn-off time was changed at 0 s.

Before that, the PH2 adaptive controller's error input (ΔI_{err}) and it's output (d_a) are around zero (see in Fig. 7). This means that the $\tilde{t}_{eff}$ value was configured correctly. It is clear in Fig. 8 that the dead time effects are compensated out by $\tilde{t}_{eff}$ as the transformer current waveform is nearly straight between the PH1 and PH4 edges.

After the turn-off time change, the first switching action happens at around 0.3 ms. The hard-coded $\tilde{t}_{eff}$ is no longer adequate to compensate for the effective dead time, as t_{off} was reduced close to zero in the simulation model. Thus, the switching action reduced the transformer current by approximately 60 A. The transformer current was intended to be reduced by a small amount. Therefore, the voltage impulse across the leakage inductance was longer than intended due to the changed turn-off time (see in Fig. 3b). Based on (5), the expected current error should be approximately

$$\Delta I_{AVG} = p \cdot \frac{U_{DC}}{L_{sp} + L'_{ss}} \cdot 2\left(\tilde{t}_{off} - t_{off}\right) \approx -63\,\text{A} \quad (8)$$

which matches the measured value.

In each consecutive PH2 phase, the controller output is increasing gradually, and the current error is reduced. After approximately 40 switching periods, the transient ends, and the transformer current waveform becomes normal again (see at the bottom of Fig. 8). The final d_a value is approximately 1.4 %, which matches the expected value calculated in (7).

Based on the simulation results, the proposed control technique is capable of compensating for the effective dead time variation. In reality, the turn-on and turn-off time does not change within seconds but in minutes. Therefore, the observed 100 ms settling time is acceptable.

6. Conclusion

In this paper, a novel adaptive dead time compensation technique was presented. It is an extension of the Continuous Cross-Period Single Phase Shift control for DAB converters, which improves the load transient response of the topology.

The effects of dead time were analyzed based on the switching waveforms of the DAB converter. The necessity of the dead time compensation was demonstrated by mathematical formulas, from which the theory of operation was derived.

The proposed control was implemented and tested in a HIL environment. It was shown that the regulator is able to compensate for a sudden change in the system's delay parameters in a few switching periods. The results prove that the technique behaves as intended and successfully mitigates the effects of dead time.

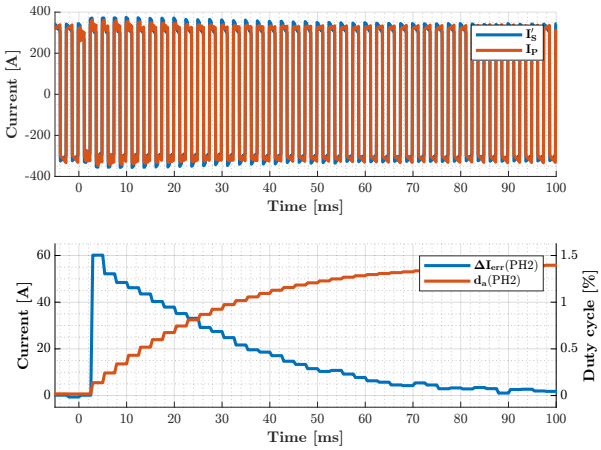


Fig. 7. The transformer currents and the adaptive controller variables when t_{off} is changed from 3 µs to 40 ns.

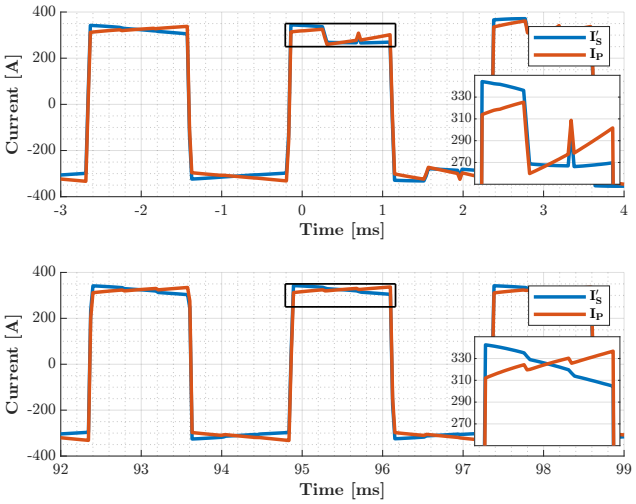


Fig. 8. The transformer currents when t_{off} is changed from 3 µs to 40 ns at 0 s. Top: the transients when the change happens. Bottom: the converter operation once the adaptive controller has settled.

The adaptive controller learns the converter's effective dead time with integrators. It can be implemented on a DSP with minimal memory footprint and computational time, making the technique suitable for embedded systems.

Further improvement could be to store the integrator output in non-volatile memory during operation. The stored value would be used as the integrator's initial value upon the startup of the converter. That would reduce the length of the adaptive controller's initial transient.

Acknowledgement

This work was performed in the frame of FIEK 16-1-2016-0007 project, implemented with the support provided from the National Research, Development and Innovation Fund of Hungary, financed under the FIEK 16 funding scheme.

References

[1] R. W. A. A. DeDoncker, D. M. Divan and M. H. Kheraluwala (1991) "A three-phase soft-switched high-power-density DC/DC converter for high-power applications". IEEE Transactions on Industry Applications, vol. 27(1), pp. 63–73. ISSN 1939-9367. doi: 10.1109/28.67533.

[2] R. W. DeDoncker, M. H. Kheraluwala and D. M. Divan (1991). "Power Conversion Apparatus For DC/DC Conversion Using Dual Active Bridges".

[3] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan and E. D. Baumann (1992) "Performance characterization of a high-power dual active bridge DC-to-DC converter". IEEE Transactions on Industry Applications, vol. 28(6), pp. 1294–1301. doi: 10.1109/28.175280.

[4] B. Zhao, Q. Yu and W. Sun (2012) "Extended-Phase-Shift Control of Isolated Bidirectional DC–DC Converter for Power Distribution in Microgrid". IEEE Transactions on Power Electronics, vol. 27(11), pp. 4667–4680. ISSN 0885-8993. doi: 10.1109/TPEL.2011.2180928.

[5] T. Hirose and H. Matsuo (2010) "A consideration of bidirectional superposed dual active bridge dc-dc converter". Proc. 2nd Int. Symp. Power Electronics for Distributed Generation Systems. ISSN 2329-5759, pp. 39–46. doi: 10.1109/PEDG.2010.5545929.

[6] F. Krismer and J. W. Kolar (2012) "Closed Form Solution for Minimum Conduction Loss Modulation of DAB Converters". IEEE Transactions on Power Electronics, vol. 27(1), pp. 174–188. ISSN 0885-8993. doi: 10.1109/TPEL.2011.2157976.

[7] H. Beiranvand, E. Rokrok and M. Liserre (2019) "Volume Optimization in Si IGBT based Dual-Active-Bridge Converters". 2019 10th International Power Electronics, Drive Systems and Technologies Conference (PEDSTC). doi: 10.1109/PEDSTC.2019.8697785.

[8] E. Laporta, G. Fernández, E. García, J. M. Perié, M. A. Alonso and J. Berges (2020) "Multi-technology battery storage system for optimal demand-side management". Renewable Energy and Power Quality Journal (RE&PQJ), vol. 18, pp. 287–291. doi: 10.24084/repqj18.301.

[9] W. Han and L. Corradini (2018) "Control Technique for Wide-Range ZVS of Bidirectional Dual-bridge Series Resonant dc-dc Converters". IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL). doi: 10.1109/COMPEL.2018.8460141.

[10] W. Han and L. Corradini (2019) "Wide-Range ZVS Control Technique for Bidirectional Dual-Bridge Series Resonant dc-dc Converters". IEEE Transactions on Power Electronics. doi: 10.1109/TPEL.2019.2893282.

[11] T. Liu, X. Yang, W. Chen, Y. Li, Y. Xuan, L. Huang and X. Hao (2019) "Design and Implementation of High Efficiency Control Scheme of Dual Active Bridge Based 10 kV/1 MW Solid State Transformer for PV Application". IEEE Transactions on Power Electronics, vol. 34(5), pp. 4223–4238. ISSN 0885-8993. doi: 10.1109/TPEL.2018.2864657.

[12] S. Veréb, A. Futó, Z. Sütő, A. Balogh and I. Varjasi (2021) "Continuous cross-period single phase shift control for dual active bridge converters". Renewable Energy & Power Quality Journal (RE&PQJ), vol. 19, pp. 222–228. ISSN 2172-038X. doi: 10.24084/repqj19.262.

[13] S. Veréb, A. Futó, Z. Sütő, A. Balogh and I. Varjasi (2020) "Adaptive Dead Time Compensation for Cross-Period Single Phase Shift Control of Dual Active Bridge Converters". Renewable Energy & Power Quality Journal (RE&PQJ), vol. 18, pp. 327–332. ISSN 2172-038X. doi: 10.24084/repqj18.318.

[14] C. Batard, F. Poitiers, C. Millet and N. Ginot (2012) MATLAB - A Fundamental Tool for Scientific Computing and Engineering Applications, IntechOpen, vol. 1, chap. 3. pp. 43–68.