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Proposed New Structure for Fault Current Limiting and Power Quality Improving Functions

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Abstract- **This paper presents the combination of the bridge type fault current limiter and power converter for voltage quality improvement. Common diode bridge fault current limiter and power converter injected together by a common dc link in new structure system. The proposed system can be connected between the beginning and end of feeder connected to critical loads and point of common coupling (PCC) in distribution network. The proposed FCL has been Simulated and Studied by PSCAD/EMTDC.**

Keywords: Fault Current Limiter (FCL), Power Converter, Sensitive loads, Power quality

I. INTRODUCTION

Power quality problems are becoming more and more important for utilities due to growing number of sensitive loads. Among all the problems, voltage sage and momentary outage are the most serious ones. Furthermore, voltage sag is mainly caused by short circuits in distribution network. The large fault currents flow may damage the series equipment, such as circuit breaker and other system components [1]. This current will also cause voltage of point of common coupling (PCC) to drop and affect most other loads which are connected to PCC. Sensitive loads often drop off-line due to voltage sag. As a result, some industrial facilities experience production outage that results in economic losses [2]-[3]. Therefore, utilities are currently exploring mitigation techniques that eliminate large fault current, increase the reliability of the power supply and improve the reliability and the system power quality [4]. The most common ways to limit fault currents are the costly replacement of substation equipments or imposition of changes in the configuration splitting power system that may lead to decreased operational flexibility and lower reliability. A novel idea is to use Fault Current Limiters (FCLs) to reduce the fault current to lower, acceptable level so that the existing switchgear can still be used to protect the power grid. An ideal FCL should have the following characteristics [5]-[6]:

- Low impedance at normal operation,
- Have a very short recovery time,
- Large impedance in fault conditions,
- Limit fault current before the first peak,
- Properly respond to any fault magnitude and/or phase combinations,
- High reliability
- Low cost.

Superconducting Fault Current Limiter (SFCL) offers a solution to these problems with many significant advantages. The application of the SFCL would not only decrease the stress on device but also it is very effective means to the system reliability and power quality in terms of availability and voltage drop. There are various types of SFCLs which are based on different superconducting material and designs such as, flux-lock, transformer, resistive, bridge types SFCL, and so on [5]. Bridge types SFCL is a kind of superconducting fault current limiter which has zero impedance under the normal condition and large impedance under the fault condition. But its advantage is fault current limitation without delay and fault current does not have any surge current, because DC reactor prevents a sudden increasing of current. The disadvantage of bridge SFCL is that can not limit the steady fault current and the fault current increase gradually [6]-[7]. Unfortunately, because of the technical and economic limitations superconducting coil has been replaced with nonsuperconducting coil, to make it simpler and much cheaper. It should be noted that the main drawback of nonsuperconductor fault current limiter (NSFCL) is power losses that is negligible in comparison with the total distribution feeder losses [8]. In this paper, the bridge type fault current limiter based on nonsuperconducting coil have been integrated with a current regulator in order to absorb the energy of inductance and transfer it to the faulted load through PWM converter by fault occurring. The proposed FCL is shown in Fig.1. Absorbing the energy of the dc reactor will result in the reduction of cause to reduce size and current rating of the inductance of dc reactor

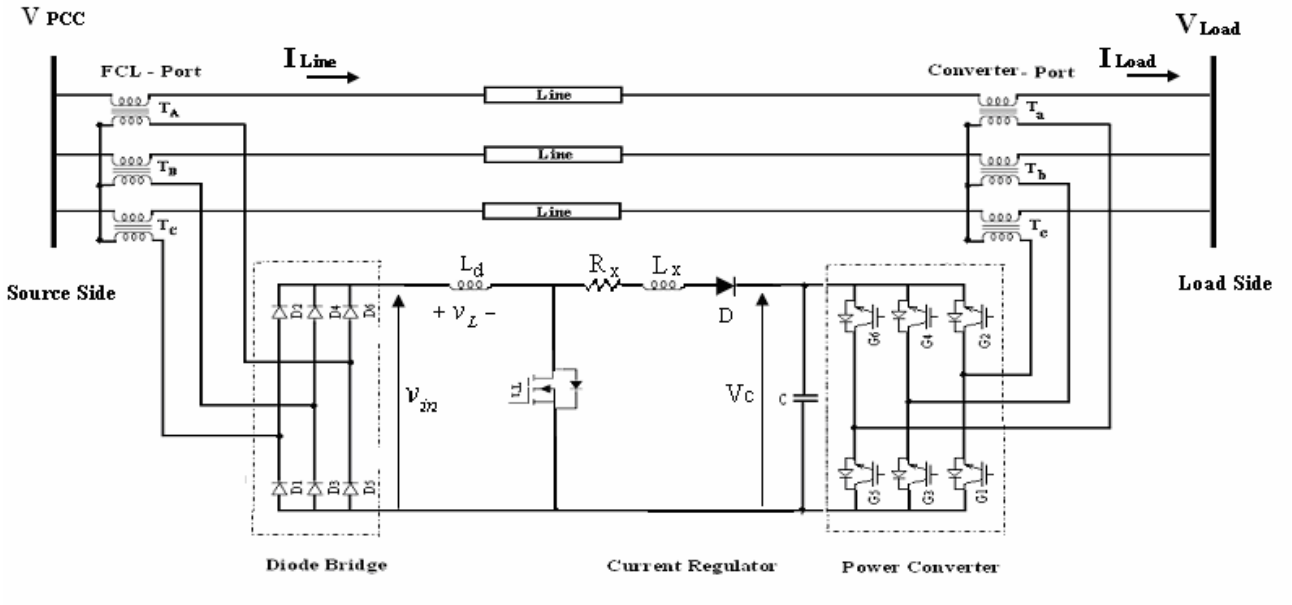

Fig.1. Proposed fault current limiter and power converter

II. PROPOSED FCL

Fig.2 shows the three-phase bridge type FCL, which consists of an inductor (L_d), series transformer bridge circuit. The diode bridge converts three-phase AC to DC current which

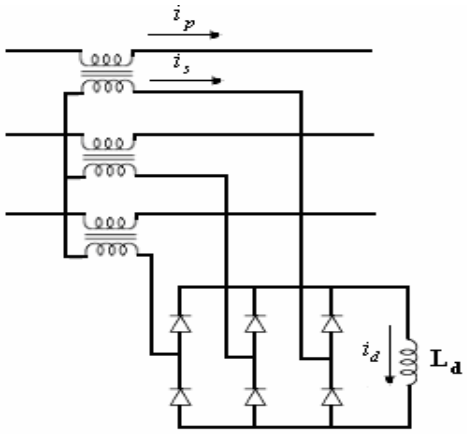

Fig.2. Bridge type fault current limiter

flows through the DC rector.

The current through the primary and secondary winding of transformer are Presented by I_P and I_S, respectively, and the ratio of transformer is N. The DC reactor current (I_d) through the DC reactor is approximately equal to the peak value of the secondary current, as follows [9]-[11]:

$$I_d = \sqrt{2} I_S = \sqrt{2}\, N\, I_P \qquad (1)$$

After charging the DC reactor and in the steady state condition, the current of L_d is approximately constant, so dI_d/dt is equal to zero and the impedance seen by the primary side of the coupling transformer is very low. Under the fault conditions, the current increases with a constant rate. One advantage of this type of FCL is that the fault current does not have any surge current. The DC reactor prevents a sudden increase of fault current. But increasing the fault current will increase voltage sag in PCC. In the proposed FCL the boost chopper is working as controlled resistor, absorbing the energy from the DC reactor and providing constant voltage for the capacitor. Then the DC voltage is converted to AC voltage, in series and synchronism with the load voltage. As a result, the load voltage can be restored to pre-fault value like a DVR (Dynamic Voltage Restorer).

A. *Principles of new structure system*

As shown in Fig. 1 The proposed FCL consist of a power converter (IGBT G1-G6), a boost regulator (MOSFET T1 and diode D), an inductor (Ld) and three phase diode bridge rectifier (D1-D6). A DC capacitor(C) is located between inverter and boost regulator. The power converter is connected in to the feeder at load side via three phase boost transformer (Ta, Tb, Tc) and DC link voltage is connected to the chopper (boost regulator) and DC reactor.

In the steady state condition, the T1 is switched on and the power converter is in standby mode. By choosing appropriate value for Ld, results in a near constant current through the DC reactor. Then proposed FCL has no effect on utility voltage and load current in the steady state condition. The circuit has

two modes in the fault condition. The first mode is shown in Fig 3-a. Turning on the T1 applies the input voltage across the inductor such that v_L is equal to v_{in} and i_L linearly ramps up, increasing the energy stored in the inductor.

In the second mode, turning off the T1 forces the inductor current to flow through the diode as shown in Fig 3-b, and a part of stored energy is transferred to the out-put capacitor. Controlling the turn-on and turn off duration, it is possible to provide constant voltage for the capacitor. The DC voltage of capacitor is converted by voltage source inverter, to AC voltage which is connected in series with line through boosting transformer at load side.

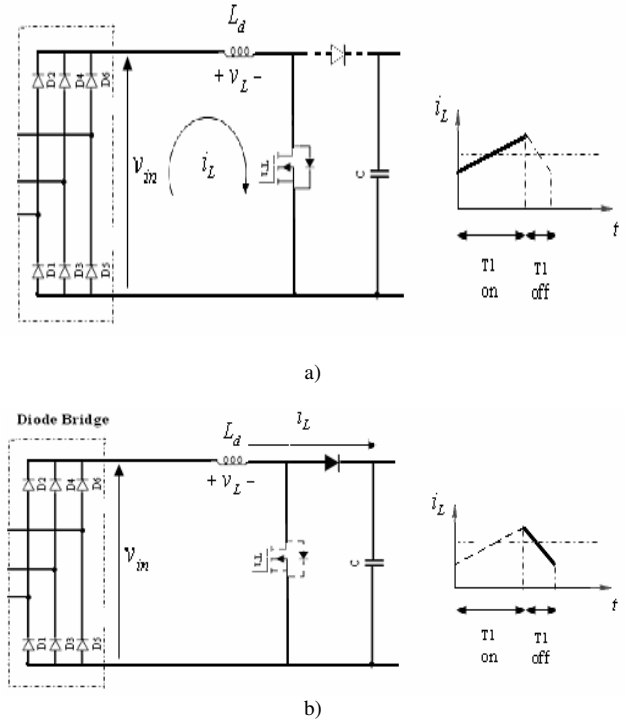

Fig 3. Operation modes of chopper during fault for charging capacitor
a) T1 is on – b) T1 is off

B. *Control System*

The main function of proposed FCL is to limit the fault current and compensate the load voltage by injecting an appropriate voltage in series and synchron with the load voltage, so that the load voltage can be restored to its desired level. As shown in Fig.4, the voltage at load side should be measured. In case a fault, the converter is controlled by a reference voltage, of *Vref=Vload_ref-Vload*, where *Vload_ref* is obtained by a PLL locked at the pre-sag load voltage. Therefore the magnitude and phase of *VLoad* is unchanged during fault. The drawback is the capacity limitation of energy storage device for the injection of real power. In the proposed FCL the chopper provides constant DC voltage for the capacitor. Fig. 5 shows the control scheme of the chopper regulator.

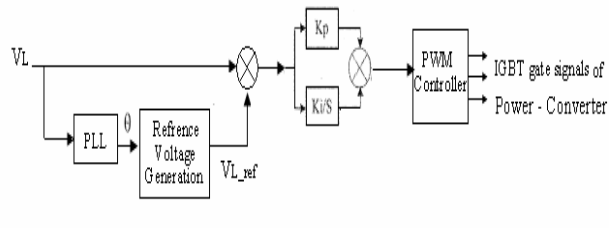

Fig 4. Control system of converter

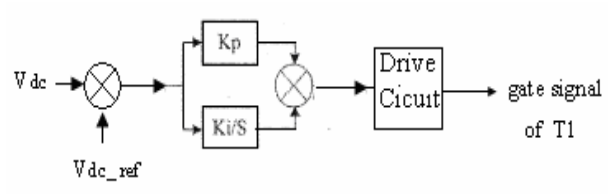

Fig 5. Control system of chopper

III. SIMULATION RESULTS

Simulations were carried out by the PSCAD/EMTDC. The modeled system is shown in Fig.6. The parameters are given in Table1. A carrier wave PWM controller is used to generate signals of IGBTs used in the power converter.

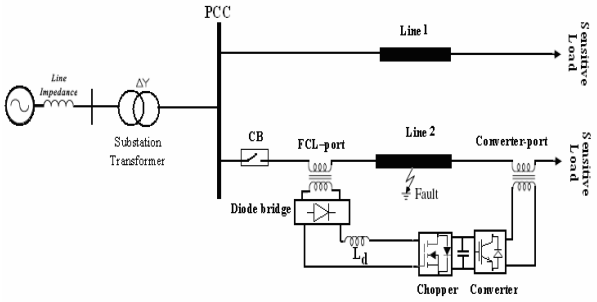

Fig.6. Simulated system

TABLE I. SYSTEM PARAMETERS

Parameter		Value
Grid	Supply voltage	20kV
	frequency	50Hz
	X/R ratio	8
	Step down transformer	20kV/8kV 10MVA
Line	R	0.1(Ω/km)
	X	0.2(Ω/km)
	Length of F1	12km
	Length of F2	8km
Load	Sensitive load 1	1MVA,pf=0.8lag
	Sensitive load 2	1MVA,pf=0.9lag
Proposed FCL	Transformers	8KV/4kV,5MVA
	DC link capacitance	3kV,1000uF
	Superconducting Coil	0.1H
	Switching frequency of chopper	5kHz

In the first simulation three phases of the load at low voltage side have been short-circuited from 500 ms to 650 ms (for 7.5 cycles). If there is no FCL, then Plot1 and plot2 of Fig.7 show the line current and voltage of PCC respectively. It is obvious that the downstream short circuit causes extremely high currents. The short circuit currents in plot1 of Fig.7 comprise of a dc component and symmetrical ac components. The dc component causes the short circuit current to be asymmetrical and the decay of the dc component depends on the X/R ratio of the circuit between the source and the fault. The PCC voltage is shown in plot2 of Fig.7 drop to about 50%.

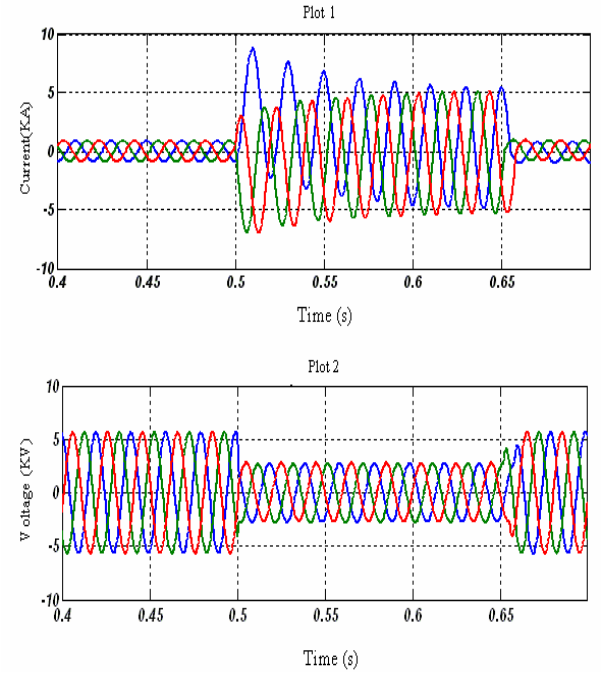

Fig.7. Line current and PCC voltage (without using FCL)

Plot1, plot2 of Fig. 8 show line current and PCC voltage in the case of using the FCL without power converter, respectively. It can be seen that the fault current does not have surge currents and was limited. Fig.9 shows DC reactor current. As shown in Fig.9, the coil current is increased by the absorb energy in to the current limiter and affect on the fault current and voltage drop. Therefore fault current and voltage sag in PCC gradually increases during the fault. Therefore the sensitive loads on other feeder connected in PCC will be affected, which this voltage sag in sensitive loads is more than acceptable level and power quality standard. On other hand, the sensitive loads on faulted feeder outage during fault. Plot1 and plot2 of Fig.10 show waveforms of DC reactor current and capacitor voltage in the case of using the proposed FCL. At t= 300ms the capacitor voltage reaches to its set point value. At the same instant T1 is turned on and DC reactor current is limited to the peak value of the secondary current.

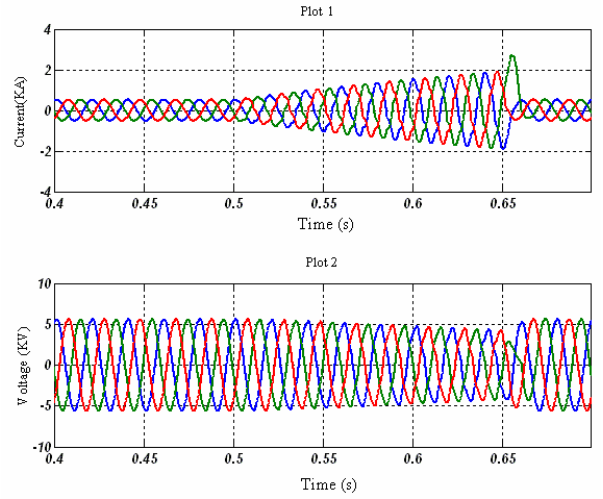

Fig.8. Line current and PCC voltage (with using FCL)

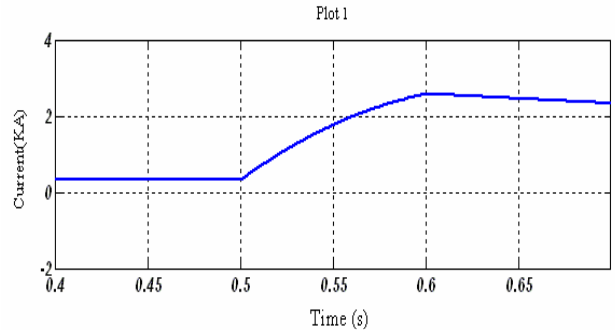

Fig.9. DC reactor current

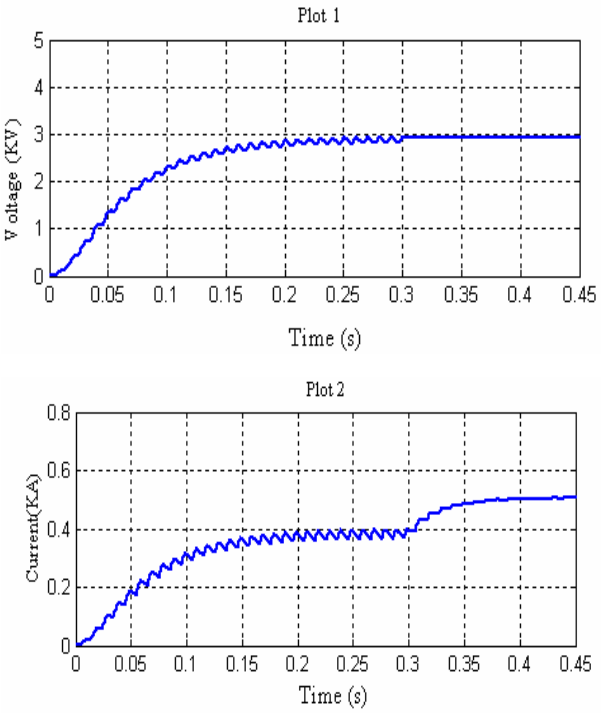

Fig.10. Capacitor voltage and DC reactor current (by using proposed

By using proposed FCL, as shown in plot1 of Fig.11, faulted load voltage is compensated completely in pre-fault and the faulted line current effectively limited by FCL port, as shown in plot2. Plot3 of Fig.11 shows the current of faulted loads. Plot 1 and plot 2 of Fig.12 shows the current of other loads connected to PCC and PCC voltage. It can be observed that the PCC voltage and the loads on other feeders would not affected by fault occurring.

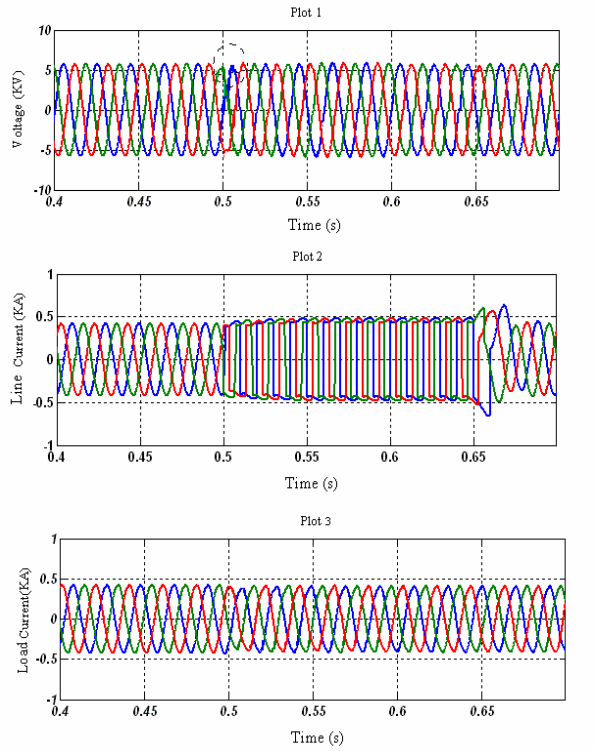

Fig. 11. Load voltage of faulted feeder (V_{Load}), fault current (I_{Line}) and load current (I_{Load})-(Proposed FCL has been used)

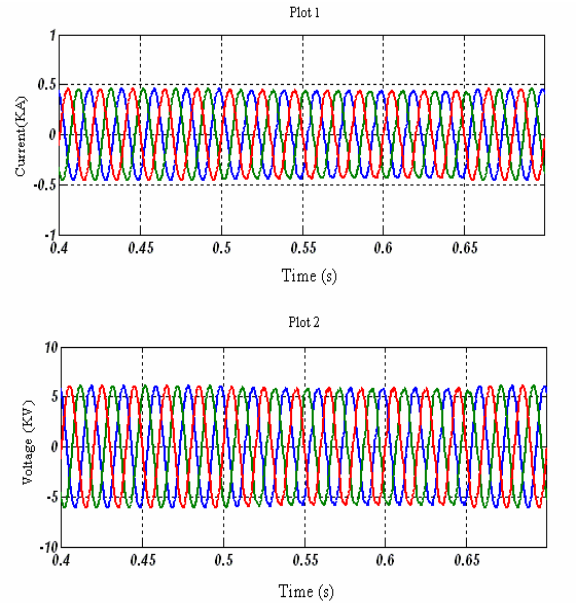

Fig.12. Current of other load connected to PCC and PCC voltage (Proposed FCL has been used)

Plot1– plot3 from Fig.13 show the real and reactive power injected by the converter port, the injected voltage to compensate the load voltage and capacitor voltage respectively. Plot1 and plot2 of Fig.14 show the DC reactor current and an enlargement of DC reactor current during fault, respectively.

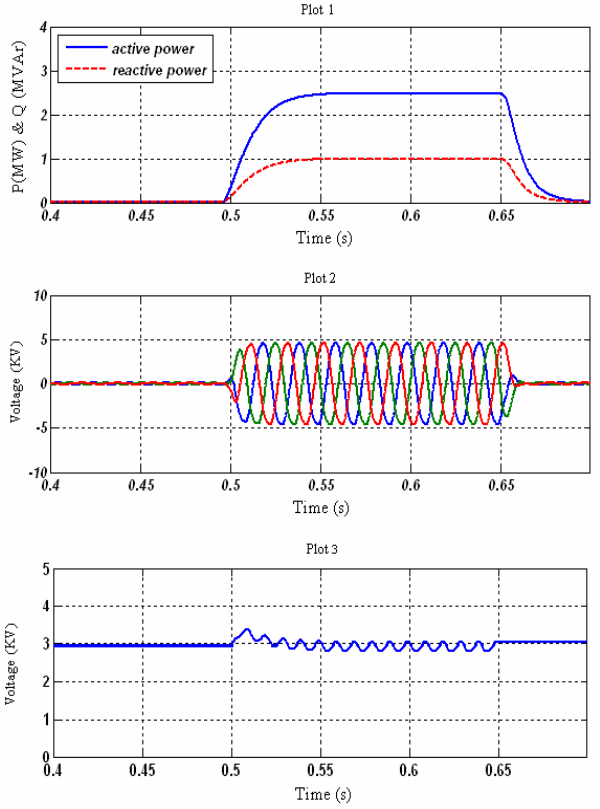

Fig.13. From top to bottom real and reactive power injected by converter, injected voltage by converter and capacitor voltage

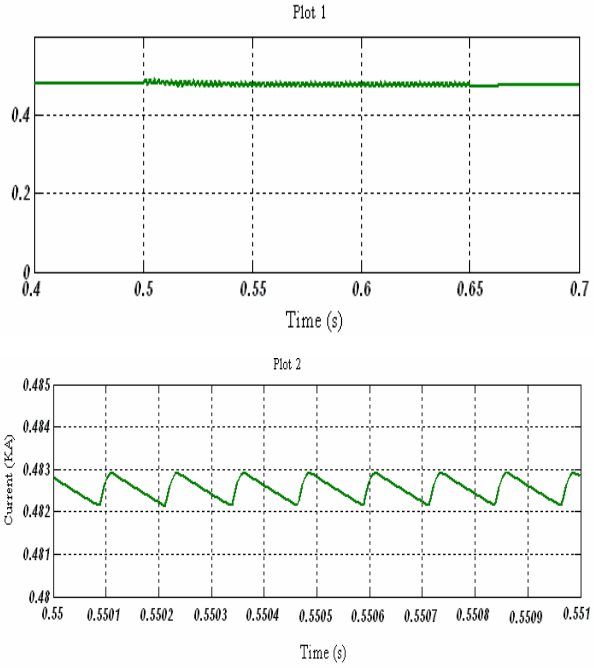

Fig.14. DC reactor and enlargement of DC reactor current

IV. Conclusion

In this paper, a new FCL has been presented. The proposed FCL can limit the fault current and improve the power quality of sensitive loads simultaneously. The simulation results show that the proposed FCL can limit faulted line current and PCC voltage, too.

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