International Conference on Renewable Energies and Power Quality (ICREPQ'13)
Bilbao (Spain), 20th to 22th March, 2013
Renewable Energy and Power Quality Journal (RE&PQJ)
ISSN 2172-038 X, No.11, March 2013

Review of Modulation Algorithms for Neutral-Point-Clamped Multilevel Converter

I. López[1], S. Ceballos[2], J. Andreu[1], I. Martínez de Alegría[1] and I. Kortabarria[1]

[1] Department of Electronic Technology
University of the Basque Country UPV/EHU, 48013 Bilbao (Spain)
Phone/Fax number:+0034 946 017243, e-mail: **iraide.lopez@ehu.es**, **jon.andreu@ehu.es**

[2] Energy Unit, Tecnalia, Parque Tecnológico de Bizkaia, 48160 Derio (Spain)
e-mail: **salvador.ceballos@tecnalia.com**

Abstract. Many modulation techniques have been developed along the years to provide in medium and high-voltage converters a high power quality and minimum switching frequency. This paper introduces some popular modulation techniques for multilevel converters, whose major challenges are obtain the previous two features. The modulation strategies that are presented are specially focused in the three-phase three-level Neutral-Point-Clamped convert (NPC), which is one of the most used topology in industry and in renewable applications.

Key words

Modulation techniques, neutral-point-clamped converter (NPC), voltage balancing.

1. Introduction

Multilevel converters are receiving special attention in industry due their meaningful advantages in high voltage and high power applications such as reactive power compensation, marine propulsion, railway traction, wind power systems, and high-voltage direct-current transmission (HVDC) among others [1]-[6].

This technology has not stopped to be deeply researched and developed since its start in order to improve power quality, power range, modularity, and other characteristics. In [4] is shown an extensive review over of the recent advances in the topologies of this technology. Among other topologies, the following ones are analyzed: five-level H-Bridge neutral-point-clamped (5L-HNPC) topology [7]-[8], three-level active NPC (3L-ANPC) [9]-[10], and the modular multilevel converter (MMC) [11]-[13] which is focused in HVDC applications. A large number of them are variations of the classic multilevel converters or a mixture of them.

The traditional or classic multilevel converter topologies are: the three-level three-phase neutral-point-clamped (3L-NPC) topology, introduced by Nabae in 1981 [14]; flying capacitor (FC) topology, introduced by Meynard in 1992 [15]; and cascaded H-bridge topology (CHB) which was used for plasma stabilization in 1990 [16], later it was extended to include three-phase systems. All of them are well-established and commercialized topologies. There are many studies in the literature comparing the three technologies in terms of losses, output voltage quality, structure and modularity [1], [17]-[18]. To summarize, could be drawn the following conclusions:

- Three-level NPC (3L-NPC) converter is the most popular topology, due its simple circuit structure and less number of capacitors and isolated DC sources.
- CHB converter is very suitable for high-power applications due its modularity achieving higher voltage levels. The main problem of this topology is that it uses a large number of isolated DC (Direct Current) sources.
- FC converter has modular structure, is not quite used compared with the previous two, due the high switching frequencies and, hence, the switching losses.

As indicated, the 3L-NPC topology has become more popular and extended topology, mainly in renewable applications. The main problem of NPC converter is how to keep the neutral point (NP) voltage stable with equal distribution of voltage in the two capacitors as shows Fig. 1. If the NP potential is not under control, the output voltage would move from the reference value, and in consequence the components will be damaged.

The traditional modulations are able to maintain the NP voltage in balance and achieve a good output voltage spectrum, but under certain operating conditions low-frequency (three times the fundamental frequency of the output voltage) voltage oscillation appears in the NP [19]-[20]. This derives in the rise of the voltage stress on

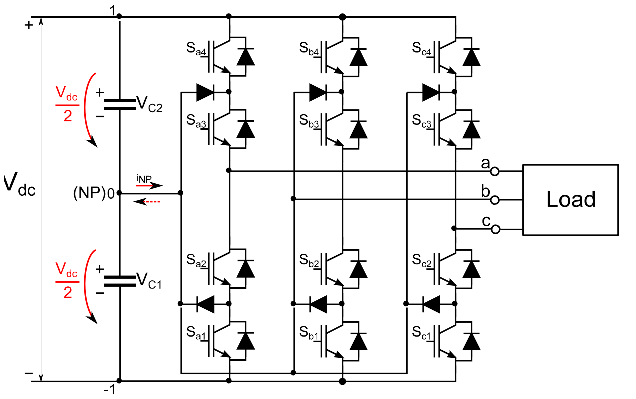

Fig. 1. Three-level three-phase NPC inverter

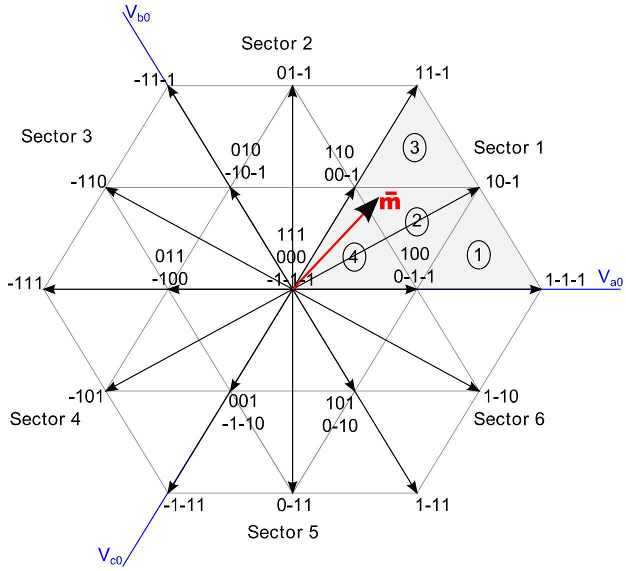

Fig. 2. SV diagram for 3L-NPC inverter.

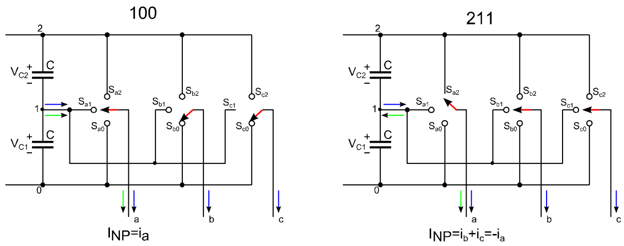

Fig. 3. Example of control of the NPC current by the proper selection of redundant vector.

the semiconductor devices and, therefore, the DC-link capacitors must be increased. There are modulation approaches that are able to remove completely this problem [21]-[22], but are incapable to achieve by themselves, or naturally, the NP voltage balance, a control loop is necessary.

In this paper the following three modulation techniques for the NPC converter are analyzed:

- Space-Vector Modulation (SVM): the most extended modulation strategy in three-phase multilevel converters, because it allows larger amplitudes of the output voltages than standard Pulse Width Modulation (PWM) strategy.
- CB-PWM with zero-sequence injection: compared with the standard sinusoidal PWM can be achieved 15% larger amplitudes of the output voltage fundamentals, better voltage-balancing performance, and lower switching frequencies. The injection of zero-sequence is related to SVM technique.
- DS-PWM: is based on CB-PWM but it can completely remove the low-frequency voltage oscillations.

2. Modulation techniques

The target of the modulation algorithms is determining in which state each power semiconductor should be, and how long, in order to generate the required output voltages and currents. In the following section the modulation strategies outlined above applied to the 3L-NPC inverter are described.

A. *Nearest three-vector space vector modulation (NTV-SVN)*

The NTV modulation uses only three of the nearest vectors from the reference vector $\overline{m}$ per modulation cycle [23]. The space-vector diagram (SV diagram) of 3L-NPC inverter has 27 different switching states (Fig. 2). Each vector defines which DC-link point (-1, 0, 1; which denote the corresponding voltage levels -Vdc/2, 0, and Vdc/2 respect to the NP) is connected each phase. The vector choice and its application time (duty cycle) are done to achieve the balance in DC-bus capacitors, and therefore, obtain the correct signal output.

In order to select the proper vectors, it is necessary to know the instantaneous NP voltage imbalance and the direction of the output currents. So, it is possible to choose the correct redundant vector of each couple to keep NP voltage balanced (Fig. 3).

Figure 3 details how the redundant vectors can be used to maintain the NP voltage under control. On the one hand vector 0-1-1 produces $I_{NP}=i_a$, and, on the other hand, vector 100, produces $I_{NP}=i_b+i_c=-i_a$. Therefore, using the appropriate redundant vector the direction of the NP current can be controlled, allowing some control degree over the NP voltage.

Once the redundant vector is selected it is necessary to order the vector sequence in order to minimize the switching frequency. Table 1 shows the vector sequences for the first sextant that minimize the switching frequency of the devices. The worst cases are in region 2 (0-1-1/110) and in region 4 (0-1-1/110) both with four switching steps. This example references to first sextant, for the rest of sextants the procedure is similar.

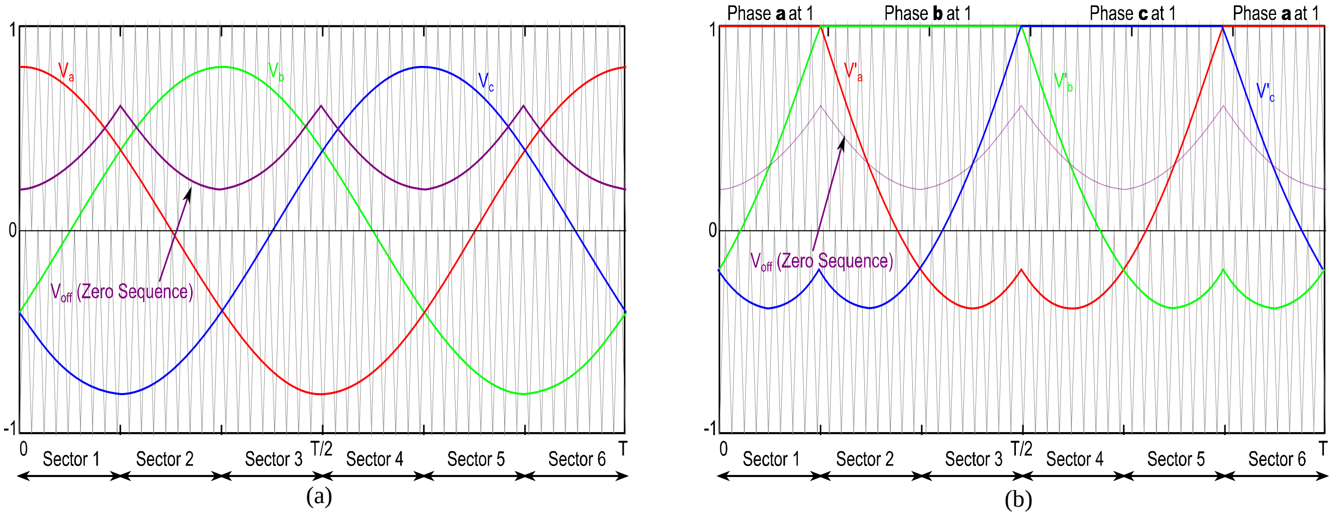

Fig. 4. Modulation signals: (a) sinusoidal references, and (b) addition of a positive zero-sequence signal.

Table 1. Vector sequences in sextant 1.

Region	Short vectors	Sequences	Steps
1	0-1-1	0-1-1/1-1-1/10-1 // 10-1/1-1-1/0-1-1	2 // 2
	100	1-1-1/10-1/100 // 100/10-1/1-1-1	2 // 2
2	0-1-1 / 00-1	0-1-1/00-1/10-1 // 10-1/00-1/0-1-1	2 // 2
	0-1-1 / 110	0-1-1/10-1/110 // 110/10-1/0-1-1	4 // 4
	100 / 00-1	00-1/10-1/100 // 100/10-1/00-1	2 // 2
	100 / 110	10-1/100/110 // 110/100/10-1	2 // 2
3	00-1	00-1/10-1/11-1 // 11-1/10-1/00-1	2 // 2
	110	10-1/11-1/110 // 110/11-1/10-1	2 // 2
4	0-1-1 / 00-1	0-1-1/00-1/000 // 000/00-1/0-1-1	2 // 2
	0-1-1 / 110	0-1-1/000/110 // 110/000/0-1-1	4 // 4
	100 / 00-1	00-1/000/100 // 100/000/00-1	2 // 2
	100 / 110	000/100/110 // 110/100/000	2 // 2

This modulation technique is simple and allows the control of the NP voltage. However some drawbacks also exist: the low-frequency NP voltage oscillation still remains, and when sequence changes due the reference vector lies into a new region, or different selection of short vectors, two switching steps (two legs must switch one level) can be produced. Adding this to the fact that some sequences need four steps (Table 1), the switching frequencies will not be constant.

B. *Carrier-Based PWM with zero-sequence voltage injection (CB-PWM).*

In the literature, there are many studies about CB-PWM modulation [24]-[25], which compared with the SPWM [26], the injection of the zero-sequence voltage signal into the original modulation signals provide the SVM same patterns and, extends the linear modulation range of the converter. But, it is not obtained the natural NP voltage balancing.

However, [27] proposes an algorithm which has the theoretical base of CB-PWM with zero-sequence voltage injection, and the analytical base of the NTV strategy. This algorithm achieves:

- Less processing time for digital implementation compared with NTV, due that the computational cost of the last one is higher.
- The switching losses are reduced because the four-step switching sequence is removed (Table 1).
- Compared with the classics CB-PWM strategies, the switching losses are reduced and also it has superior capability to balance the NP voltage.

A salient feature of NPV strategy is shown in the Table 1. In the all cases, except the four-step cases, one phase does not change its switching state. So, in comparison with other SVM strategies, NTV reduces the switching frequency of the switching devices. In a Fig. 4 (a) is shown the CB-PWM technique with two carrier signals which are compared with the modulation signals to generate the switching signals. When, in NTV strategy one phase does not switch along the cycle, is equivalent to maintain the corresponding modulation signal clamped to -1, 0 or 1. To achieve it, a zero-sequence signal (v_{off}) must be added to the modulation reference signals (Fig. 4 (b) [27]), and thus, the modulation signals are clamped to 1 (in this case). However NP current is affect by the injection of zero-sequence voltage and, could destabilize the NP voltage balance. The relationship between the NP average current and the modified modulation signals is:

$$\bar{i}_{NP} = \left(1-\left|v_a'\right|\right)\cdot i_a + \left(1-\left|v_b'\right|\right)\cdot i_b + \left(1-\left|v_c'\right|\right)\cdot i_c \qquad (1),$$

where v_x' for $x=\{a, b, c\}$are $v_x' = v_x + v_{off}$, and v_x is the modulation signal and v_{off} is a common signal to the three phases and ensures that the maximum range is achieved for the linear operation mode; its value is:

$$v_{off} = \frac{\max(v_a, v_b, v_c) + \min(v_a, v_b, v_c)}{2} \qquad (2)$$

To solve this problem, is resorted to the NTV strategy that achieves the balanced choosing the appropriate redundant vector in each situation. But, the region 2 (0-1-

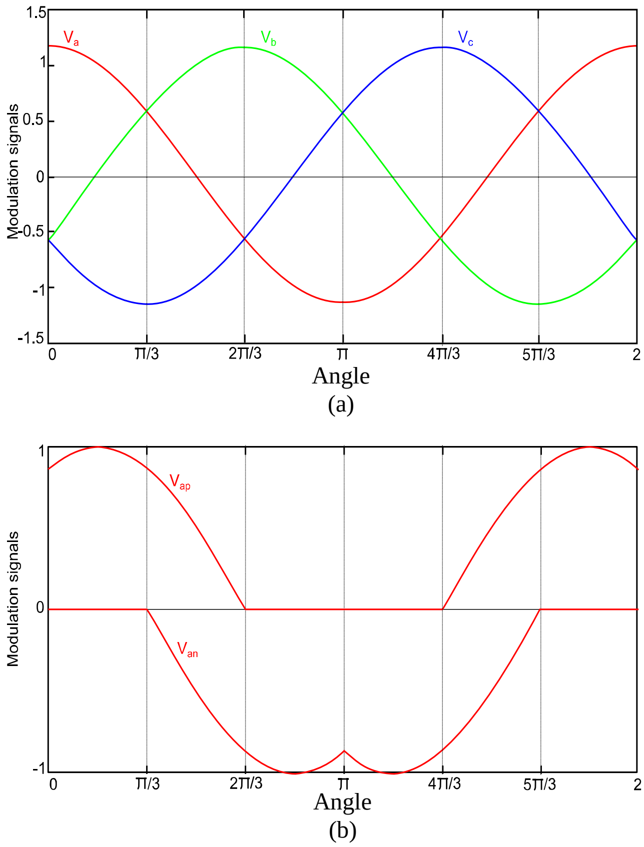

Fig. 5. Example for sinusoidal modulation signals: (a) Original signals. (b) Modified signals for phase *a*.

1/10-1/110) is a special case, in which none of the phases is clamped. Therefore, some considerations are made:

- Only a maximal-modulation signal (v_{max}) can be clamped to +1. In the same way, to -1 only a minimal-modulation signal (v_{min}) can be clamped and; to 0 median-modulation signal (v_{mid}). Always the generated signal must be into range [+1, −1].
- If the sign of one ac-side current is not appropriate to achieve the voltage balancing, this signal not must be clamped to 0, therefore it only can be clamped to +1 or -1, if the phase corresponds to v_{max} or v_{min} respectively.
- If one output phase current has the proper direction to assist voltage balancing, the corresponding modulation signal should be clamped to 0 if it is v_{mid}, but not to +1 or −1 if it is v_{max} or v_{min}, respectively.
- In the case of having two ac-side currents corresponding to the modulation signals v_{max} and v_{min} and being appropriate to keep the voltage balancing, the third one (associated to v_{mid}) is not adequate to assist the balance. Hence, v_{mid} should be shifted to the farthest possible from zero. This is usually achieved by clamping v_{max} to +1or v_{min} to −1, for $v_{mid} > 0$ or $v_{mid} \leq 0$, respectively. This is the only resolution different to NTV. Due this fact, the sequences that require four switching steps are avoided.

All of those conclusions are summarized mathematically in the Table 2 where ΔV_{NP} is the V_{C1}-V_{C2}.

Table 2. Actions to assist voltage balancing.

Sextant 1 and [sextant 4]

$\Delta V_{NP} \cdot i_a > 0$	$\Delta V_{NP} \cdot i_c > 0$	Action	v_{off}
0	0	*b* clamped to 0	$-v_b$
0	1	*a* clamped to +1 [-1]	$+1-v_a$ $[-1-v_a]$
1	0	*c* clamped to -1 [+1]	$-1-v_c$ $[+1-v_c]$
1	1	For $v_b>0$: *a* clamped to +1 [*c* clamped to +1] For $v_b\leq0$: *c* clamped to -1 [*a* clamped to -1]	For $v_b>0$: $+1-v_a$ $[+1-v_c]$ For $v_b\leq0$: $-1-v_c$ $[-1-v_a]$

Sextant 2 and [sextant 5]

$\Delta V_{NP} \cdot i_b > 0$	$\Delta V_{NP} \cdot i_c > 0$	Action	v_{off}
0	0	*a* clamped to 0	$-v_a$
0	1	*b* clamped to +1 [-1]	$+1-v_b$ $[-1-v_b]$
1	0	*c* clamped to -1 [+1]	$-1-v_c$ $[+1-v_c]$
1	1	For $v_a>0$: *b* clamped to +1 [*c* clamped to +1] For $v_a\leq0$: *c* clamped to -1 [*a* clamped to -1]	For $v_a>0$: $+1-v_b$ $[+1-v_c]$ For $v_a\leq0$: $-1-v_c$ $[-1-v_b]$

Sextant 3 and [sextant 6]

$\Delta V_{NP} \cdot i_b > 0$	$\Delta V_{NP} \cdot i_a > 0$	Action	v_{off}
0	0	*c* clamped to 0	$-v_c$
0	1	*b* clamped to +1 [-1]	$+1-v_b$ $[-1-v_b]$
1	0	*a* clamped to -1 [+1]	$-1-v_a$ $[+1-v_a]$
1	1	For $v_c>0$: *b* clamped to +1 [*a* clamped to +1] For $v_c\leq0$: *a* clamped to -1 [*b* clamped to -1]	For $v_c>0$: $+1-v_b$ $[+1-v_a]$ For $v_c\leq0$: $-1-v_a$ $[-1-v_b]$

In the case of region 4 (0-1-1/000/110), this criterion is not adopted, due as shown in the Table 1. Only the NP voltage is considering for clamping. The amplitude of the modulation signals is small (from CB-PWM point of view), and this means that clamping the modulation signal to zero requires less zero-sequence voltage amplitude. To determine which signal should be clamped to the NP, all of the three phase's contribution $\Delta v_{NP} \cdot i_x, x = \{a, b, c\}$ is calculated and evaluated. The maximum value indicates the modulation signal that has to be clamped to the NP, because this phase carries the best balancing current. In this strategy, the four-step switching-transition sequences are also avoided.

To finalize, to know in which sector lies the reference vector is only need the maximum and minimum value of modulation signals (Table 3.)

Table 3. Determination of the sector.

v_{max}	v_{min}	Sextant
v_a	v_c	1
v_b	v_c	2
v_b	v_a	3
v_c	v_a	4
v_c	v_b	5
v_a	v_b	6

C. Double-Signal PWM (DS-PWM).

One of the main problems in the NPC converter is the low-frequency voltage oscillation in NP under some operating conditions. With DS-PWM strategy [22], [28]-[29] that problem is completely removed for all operating conditions, even with unbalanced and nonlinear loads. Nevertheless, it presents any drawbacks also: the switching-frequencies of the devices are 1/3 higher than

SPWM, this is, higher than the strategies that have been analyzed; and that it does not provide a natural voltage balance; hence, is necessary to include a control or compensator.

This strategy employs two modulation signals for each phase. To obtain these signals, firstly it is necessary to add a zero-sequence to the original modulation signals to obtain the maximum range of linear operation mode:

$$\begin{cases} v_a^{'} = v_a - v_{off} \\ v_b^{'} = v_b - v_{off} \\ v_c^{'} = v_c - v_{off} \end{cases} \quad (3),$$

where v_{off} (zero-sequence) has the same expression that shows equation (2).

The two modulation signals should satisfy the following expression:

$$\begin{cases} v_a^{'} = v_{ap} + v_{an} \\ v_b^{'} = v_{bp} + v_{bn} \\ v_c^{'} = v_{cp} + v_{cn} \end{cases} \quad (4),$$

where $v_{xp} \geq 0$ and $v_{xn} \leq 0$ and $x=\{a,b,c\}$. The signals with the subscript *'p'* will only cross the upper carrier $v^p_{carrier} \in [0,1]$, and with subscript *'n'* will only cross the lower $v^n_{carrier} \in [-1,0]$. It can be demonstrated that the locally-average NP current when this modulation strategy is used is given by (5).

$$\bar{i}_{NP} = \left|v_{an}^{+1} - v_{ap}\right|\bar{i}_a + \left|v_{bn}^{+1} - v_{bp}\right|\bar{i}_b + \left|v_{cn}^{+1} - v_{cp}\right|\bar{i}_c \quad (5)$$

Where $v_{xn}^{+1} = v_{xn} + 1$ are the duty cycles of NP connection. In order to keep the NP voltage balanced $\bar{i}_{NP}$ should be zero, there are a large number of solutions to achieve $\bar{i}_{NP} = 0$; a good one that minimizes the switching-frequencies is given by the following expression:

$$\begin{cases} v_{xp} = \dfrac{v_x - \min(v_a, v_b, v_c)}{2} \\ v_{xn} = \dfrac{v_x - \max(v_a, v_b, v_c)}{2} \end{cases} \text{, for } x = \{a, b, c\} \quad (6)$$

In this way the variables v_{xp} and v_{xn} are forced to be zero for the maximum time possible, and in these intervals some of the transistors do not switch. An example of the application of the expression (6) to phase *a*, is shown in Fig. 5 (a). The modified modulation signal are within the range [-1, 1], this is, under linear modulation and with the maximum modulation index (v_a, v_b, and v_c equal to 1.547). In addition the NP voltage is controlled.

However, sometimes, due to the non-ideal performance of the converter it is necessary to produce $\bar{i}_{NP} \neq 0$ in order to maintain the NP voltage completely balanced. Otherwise if, for instance, the initial voltages in the capacitors were slightly different, the modulation strategy would tend to maintain the imbalance because the locally-averaged NP current is zero. Therefore, sometimes the modulation signals should be shifted up or down to carry out a proper compensation; this can only be accomplished when the modulating signal is not set to zero. Otherwise the switching frequency increases considerably. Hence, for the phase *a* in the Fig. 5 (b), the proper interval to shift the signal are $\pi/3 \leq \omega t \leq 2\pi/3$ and $4\pi/3 \leq \omega t \leq 5\pi/3$.

In the same way, the relationship shown in (4) must be satisfied to prevent the distortion of the output voltages. This can achieved with an external control which applies the magnitude of the offset to the modified modulation signals but with the opposite sign. This is widely analyzed in [29].

In order to finalize, the Table 4 is presented, where the main characteristics of the studied modulation techniques are summarized. Similar behavior is achieved with the first two techniques (NTV-SVM and CB-PWM), but when the number of phases need to be extended, the PWM algorithms are preferred due their feasibility of extension.

Table 4. Features of modulation techniques.

Strategy	(1)	(2)	(3)	(4)	(5)
NTV-SVM	Medium	Good	Medium	No	Yes
CB_PWM	Low	Good	Low	No	Yes
DS_PWM	High	Medium	Low	Yes	No

- (1). Switching-frecuency.
- (2). THD.
- (3). Computational complexity
- (4). Remove low-frequency ripple.
- (5). Achieve natural NP voltage balance.

3. Conclusions

Three modulation techniques for the NPC inverter have been analyzed. It has been highlighted that with the use of PWM techniques is possible to control the NP voltage. In addition PWM strategies have advantages in terms of simplicity and computational complexity than their SVM counterparts.

Acknowledgement

This work has been carried out inside de Research and Education Unit UFI11/16 of the UPV/EHU and supported by the Department of Education, Universities and Research of the Basque Government within the fund for research groups of the Basque university system IT394-10, the University of Basque Country UPV/EHU, and the Department of Education, Universities and Research of the Basque Government on the basis of support for training of researchers RBFI-2011-167.

References

[1]. J. Rodriguez, S. Bernet, B. Wu, J. Pontt, S. Kouro, “Multilevel voltaje-source-converter topologies for industrial médium-voltage drives”, IEEE Transactions on Industrial Electronics 2007, Vol., 54, pp 2930-2945.

[2]. J. Rodriguez, L. Franquelo, S. Kouro, J. Leon, R. Portillo, M. Prats, M. Perez, “Multilevel converters: an enabling technology for high-power applications”, in Proc. IEEE2009, Vol. 97, pp. 1786-1817.

[3]. G. Adam, K. Ahmed, S. Finney, B. Williams, “Modular multilevel converter for medium-voltage applications”, Proc. IEMDC2011, pp.1013-1018.

[4]. S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Pérez, J. Leon, “Recent asvances and industrial applications of multilevel converters”, IEEE Transactions on Industrial Electronics 2010, Vol. 58, pp. 2553-2580.

[5]. M. Chaves, E. Margato, J. Silva, S. Pinto, J. Santana, “HVDC transmission systems: bipolar back-to-back diode clamped multilevel converter with fast optimum-predictive control and capacitor balancing strategy”, Electric Power Systems Research 2011, Vol. 81, pp. 1436-1445.

[6]. Z. chen, X. Xiao, H. Wang, M. Liu, “Analysis of converter topological structure for direct-drive wind power systems with PMSG”, Proc. POWERCON2010, pp.1-5.

[7]. C. Wu, W. Lau, h. Chung, “A five-level neutral-point-clamped H-Bridge PWM inverter with superior harmonics suppression: a theoretical analysis”, Proc. ISCAS1999, Vol.5, pp 198-201.

[8]. K. Ma, F. Blaabjerg, “Multilevel converters for 10 MW wind turbines”, Proc. EPE2011, pp. 1-10.

[9]. C. Attaianese, M. Di Monaco, G. Tomasso, “Three-phase three-level active NPC converters for high power systems”, Proc. SPEEDAM2010, pp.204-209.

[10]. J. Li, A. Huang, Z, Liang, S. Bhattacharya, “Analysis and design of active NPC (ANPC) incverters for fault-tolerant operation of high-power electrical-drives”, IEEE Transactions on Power Electronics 2012, Vol. 27, pp. 519-533.

[11]. A. Lesnicar, R. Marquardt, “An innovative modular multilevel converter topology suitable for wide power range”, IEEE Bologna Power Tech Conference, 2003.

[12]. S. Allebrod, R. Hamerski, R. Marquardt, “New transformerless, scalable modular multilevel converters for HVDC-transmission”, Proc. PESC2008, pp. 174-179.

[13]. J. Zhao, C. Gao, K. Cao, X. Yang, W. Mao, J. Jiang, “Research on high-voltage large-capacity modular multilevel converter (MMC) system”, ISDEA2012, pp. 1470-1474.

[14]. A. NAbae, I. Takahashi, H. Akagi, “A new neutral-point-clamped PWM inverter”, IEEE Transactions on Industrial Electronics 1981, pp. 518-523.

[15]. T. Meynard, H. Foch, “Multilevel conversion: high voltage choppers and voltage-source inverters”, PESC1992, Vol. 1, pp. 397-403.

[16]. M. Marchesoni, M. Mazzucchelli, S. Tenconi, “A nonconventional power converter for plasma stabilization”, IEEE Tansactions on Power Electronics 1990, Vol. 5, pp. 212-219.

[17]. T. Prathiba, P. Renuga, “A comparative study of Total Harmonic Distortion in Multilevel inverter topologies”, Proc. IISTE2012, Vol. 2, pp. 26-36.

[18]. A. Sanchez, M. Mazuela, S. Alvarez, G. Abad, I. Baraia, “Medium voltaje-high power converter topologies comparison procedure, for 6.6 kV drive application using 4.5 kV IGBT modules”, IEEE Transactions on Industrial Electronics 2012, Vol. 59, pp. 1462-1476.

[19]. J. Pou, D. Boroyevich, R. Pindado, “Effects of imbalances and nonlinear loads on the voltage balance of a neutral-point-clamped inverter”, IEEE Transactions on Power Electronics 2005, Vol. 20, pp. 123-131.

[20]. J. Pou, R. Pindado, D. Boroyevich, P. Rodríguez, “Evaluation of low-frequency neutral-point voltaje oscillations in the three-level invertir”, IEEE Transactions on Industrial Electronics 2005, Vol. 52, pp. 1582-1588.

[21]. S. Busquets-Monge, J. Bordonau, D. Boroyevich, S. Somavilla, “the nearest three virtual space vector PWM-A modulation for the comprehensive neutral-point balancing in three-level NPC”, IEEE Power Electron 2004, Vol. 2, pp. 11-15.

[22]. J. Pou, J. Zaragoza, P. Rodríguez, S. Ceballos, v. Sala, R.Burgos, D. Boroyevich, “Fast-proccesing modulation strategy for the neutral-point-clamped converter with total elimination of the low-frequency voltaje oscillatons in the neutral point”, IEEE Transactions on Industrial Electronics 2007, Vol. 54, pp. 2288-2299.

[23]. N. Celanovic, D. Boroyevich, “A fast space-vector modulation algorithm for multilevel three-phase converters,” IEEE Transactions on Industrial Applications 2001, Vol. 37, pp. 637-641.

[24]. M. Carpita, M. Marchesoni, M. Pellerin, D. Moser, “Multilevel Converter for Traction Applications: Small-Scale Prototype Tests Results”, IEEE Transactions on Industrial Electronics 2008, Vol 55, pp. 2203-2212.

[25]. L.G. Franquelo, J. Rodriguez, J.I. Leon, S. Kouro, R. Portillo, “The age of multilevel converters arrives”, Industrial Electronics Magazine, IEEE, Vol 2, pp. 28-29.

[26]. N. Mohan, T. Undeland, Robbins W. 2003. Power Electronics: Converters, Applications and Design.

[27]. J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, D. Boroyevich, “A carried-based PWM strategy with zero-sequence voltaje injection for a three-level neutral-point-clamped converter”, IEEE Transactions on Power Electronics 2012, Vol. 27, pp. 642-651.

[28]. J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, M. Corbalán, “VOltage-balance compensator for a carrier-based modulation in the neutral-point-clamped-converter”, IEEE Transactions on Industrial Electronics 2009, Vol. 56, pp. 305-314.

[29]. J. Pou, P. Rodríguez, V. Sala, J. Zaragoza, R. Burgos, D. Boroyevich, “Fast-processing modulation strategy for the neutral-point-converter with total elimination of the low-frequency voltage oscillations in the neutral point”, IECON2005, pp. 1054-1059.