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Synchronization of a single-phase wind energy generator with the low-voltage utility grid

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Abstract. This paper presents a new circuit topology of a phase-locked loop that can be used for synchronising a single-phase wind turbine generator (WTG) with the low voltage utility grid. The circuit is based on the time-delay digital tanlock loop (TDTL) architecture and was modelled and simulated using Simulink/MATLAB. The results presented demonstrate the ability of the circuit not only to synchronise a WTG with the grid, but also to re-gain synchronization following a sudden disturbance in the grid voltage. The simulated disturbances included a ramp and a multi-step change in the phase of the grid voltage waveform.

Key words

Wind-turbine generator, renewable energy, grid synchronization, time-delay digital tanlock loop.

1. Introduction

Recent years have seen interest in renewable energy utilization increasing at a record rate [1-2]. Due to the intermittent nature of renewable energy sources (RES), its utilization has, mainly, taken one of two forms: using a standalone system in which the ac load is connected to a "standalone" inverter energised from a battery bank, or by integrating the renewable energy into the low voltage grid using a "grid-tie" inverter [3,4]. However, connecting a renewable energy (RE) generator such as a wind turbine generator (WTG) to the grid may induce unwanted effects on the grid voltage such as harmonic distortion. In order to regulate the connection and integration of an RE generator with the grid, certain regulations have been put forward by regulatory bodies such as the IEC (International Electrotechnical Commission) and the IEEE [5,6]. Prior to connecting an RE generator, or any generator for that matter, the generator voltage must be synchronised with the grid voltage. To achieve such synchronization, circuits based on the implementation of some form of the ubiquitous phase-locked loop technique have been reported in the literature [7-9]. Generally, these are analogue circuits and therefore, their working life and functionality are fairly dependent upon component tolerances and aging. In this paper, a new digital circuit topology for synchronising a single-phase wind turbine generator with the grid is presented. The circuit which is based on the time delay digital tanlock loop (TDTL) [10,11] not only synchronises a WTG to the grid, but also re-establishes synchronization whenever it is lost such as after a sudden perturbation in the phase of the grid voltage. Essentially, the circuit consists of two TDTL loops as depicted in Fig. 1. The upper loop is a second order loop through which synchronization is achieved and is used to drive the lower first order TDTL loop. Therefore, the system will be referred to as TDTL with dual input (TDTL-DI). The lower arctan phase detector produces an error signal that is proportional to the phase difference between the DCO (digital controlled oscillator) output and the grid voltage. This error is corrected by the upper loop.
Mathematical analysis and modelling of the proposed circuit along with results of its testing are presented.

2. System Analysis

A continuous sinusoidal signal $y(t)$ with a frequency offset

$$\Delta\omega = (\omega - \omega_o)$$

is received by the proposed design. This is also translated as a phase shift, from the free running frequency $\omega_o\ (rad/s)$ of the DCO as follows

$$y(t) = A\sin\left[\omega_o t + \theta(t)\right] \tag{1}$$

where A is the input signal amplitude and

$$\theta(t) = \Delta\omega t + \theta_o$$

is the phase process of the incoming signal, where $\theta_o \ (rad)$ is constant. The incoming signal is passed through a time delay unit τ that introduces a variable phase shift of $\psi = \omega\tau, (rad)$ depending on incoming signal frequency value. Consequently, a phase shifted signal $x(t)$ of the input "incoming" signal which is generated due to the delay may be expressed as

$$x(t) = A\sin\left[\omega_o t + \theta(t) - \psi\right] \tag{2}$$

As both signals; the incoming signal and the phase shifted version pass through sample and hold blocks, as illustrated in Fig. 1, sampled versions of both continuous signals (1) and (2) may be expressed as in (3) and (4) respectively

$$y(k) = A\sin\left[\omega_o t(k) + \theta(k)\right] \tag{3}$$

and

$$x(k) = A\sin\left[\omega_o t(k) + \theta(k) - \psi\right] \tag{4}$$

where

$$\theta(k) = \theta\left[t(k)\right]$$

where t(k) is the elapsed time up to the k[th] sampling instant.

The sampling interval between the sampling instants $t(k)$ and $t(k-1)$ is given by

$$T(k) = T_o - c(k-1) \tag{5}$$

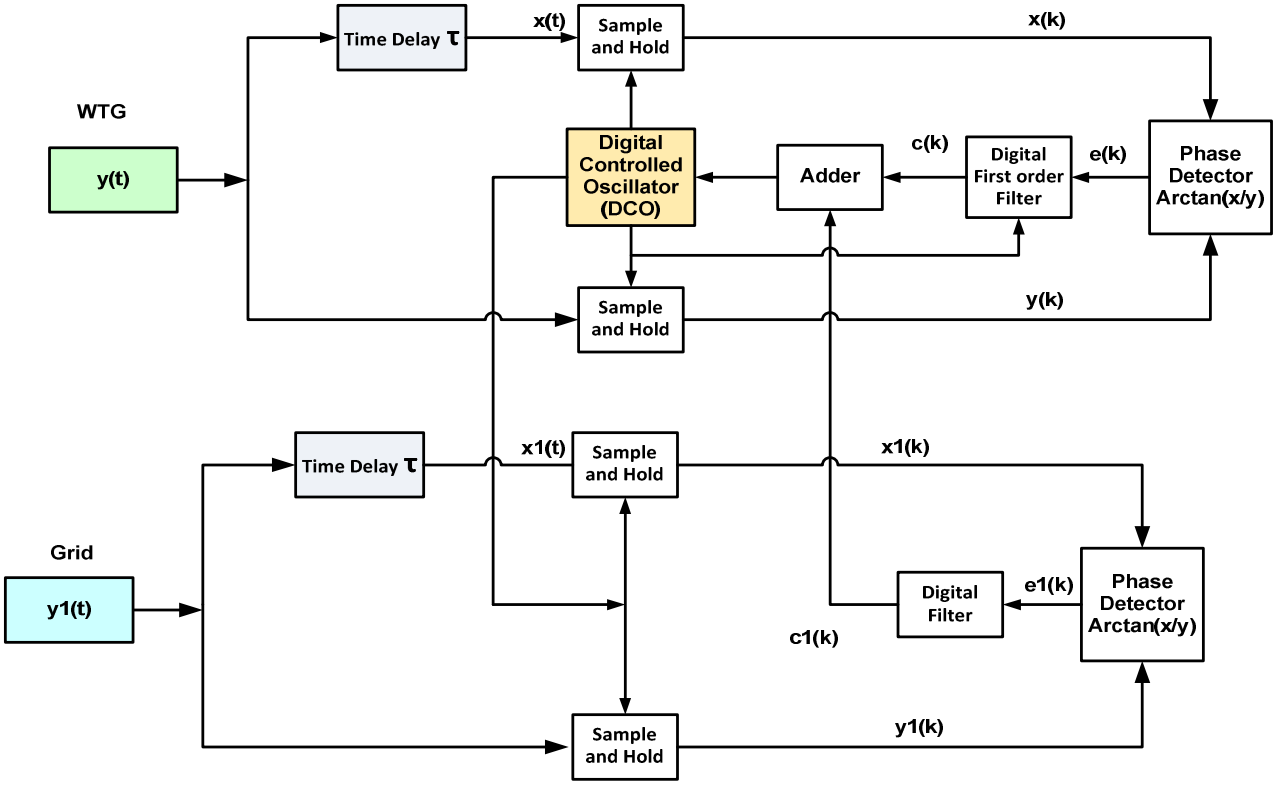

Fig. 1 Block diagram of the proposed system TDTL-DI.

where $T_o = 2\pi / \omega_o$ is the nominal period of the DCO and $c(i)$ the output of the digital loop filter at the i[th] sampling instant. By assuming $t(0) = 0$, the elapsed time to reach the k[th] sampling instant is

$$t(k) = \sum_{i=1}^{k} T(i) = kT_o - \sum_{i=0}^{k-1} c(i) \tag{6}$$

As a result both $y(k)$ and $x(k)$ can be written as

$$y(k) = A\sin\left[\theta(k) - \omega_o \sum_{i=0}^{k-1} c(i)\right] \tag{7}$$

and

$$x(k) = A\sin\left[\theta(k) - \omega_o \sum_{i=0}^{k-1} c(i) - \psi\right] \tag{8}$$

Therefore, the phase error between the incoming signal and the DCO output signal can be defined as

$$\phi(k) = \theta(k) - \omega_o \sum_{i=0}^{k-1} c(i) - \psi \tag{9}$$

Both (7) and (8) can be expressed in terms of the above phase error as

$$y(k) = A\sin\left[\phi(k) + \psi\right] \tag{10}$$

and

$$x(k) = A\sin\left[\phi(k)\right] \tag{11}$$

Hence, the loop error signal $e(k)$ produced by the phase detector can be expressed as

$$e(k) = f\left[\tan^{-1}\left(\frac{\sin\left[\phi(k)\right]}{\sin\left[\phi(k) + \psi\right]}\right)\right] \tag{12}$$

where $f(\gamma) = -\pi + [(\gamma + \pi) \bmod 2\pi]$. This error signal $e(k)$ represents the non-linear phase error version whose effect on the nonlinearity of the system worsens as the phase shift ψ moves away from $\pi/2$. The digital loop filter with a transfer function $D(k)$ receives the error signal $e(k)$ and produces the signal $c(k)$ that drives the DCO to the required frequency. Consequently, the system difference equation can be derived from (6) and (9) as

$$\phi(k+1) = \phi(k) - \omega c(k) + \Lambda_o \tag{13}$$

where

$$\Lambda_o = 2\pi(\Delta\omega / \omega_o)$$

Due to the nonlinearity produced by the variation in the phase shift ψ which depends on the incoming signal frequency, the system difference equation cannot be solved by using the Z-transform to find the locking range as was the case for the digital tanlock loop (DTL) [12]. Therefore, the difference equation was solved numerically using the fixed point theorem [12-14] as in the case applied to the zero-crossing digital phase lock loop [12,15,16].

The second order loop utilizes a proportional plus accumulation digital filter transfer function $D(z)$ which is given by

$$D(z) = G_1 + G_2 / (1 - z^{-1}) \tag{14}$$

where G_1 *and* G_2 are positive constants. From (13) and (14), the system difference equation of the second order TDTL can be derived as

$$\begin{aligned}\phi(k+2) = {} & 2\phi(k+1) - \phi(k) \\ & - rK_1' h\left[\phi(k+1)\right] \\ & + K_1' h\left[\phi(k)\right]\end{aligned} \tag{15}$$

Where

$r = 1 + G_2 / G_1$ and $K_1' = G_1 \omega$.

Following the procedure presented in [12,15,16] with a fixed point analysis as in the second order TDTL, the locking range is given by

$$0 < K_1 < \frac{4}{1+r}\ W\ \sin\left(\frac{\psi_o}{W}\right) \tag{16}$$

where ψ_o is the nominal phase lag induced in the incoming signal by the time delay unit. The lower phase detector uses the DCO of the upper loop for sampling the incoming grid signal $y1(t)$, therefore, the phase error detector of the lower loop produces an error if there is a phase difference between DCO and the grid. The digital loop filter with a transfer function $D1(k)$ receives the error signal $e1(k)$ which produces the signal $c1(k)$. The digital filter of the lower loop is simply a gain block G_2.Therefore, the produced loop gain is $K_2' = G_2\omega$. This modifies the second order TDTL system difference equation (15) as

$$\begin{aligned}\phi(k+2) = {} & 2\phi(k+1) - \phi(k) \\ & - r(K_1' + K_2')h\left[\phi(k+1)\right] \\ & + (K_1' + K_2')h\left[\phi(k)\right]\end{aligned} \tag{17}$$

If there is no phase shift initially, the phase difference will be zero and consequently the loop gain is $K_2' = 0$. On the other hand, when a phase step is applied to the input a phase error $e1(k)$ is generated. Consequently the loop gain K_2' will be included in (17) and corrected by the first second order TDTL loop, as a result the signal $y(t)$ will synchronised with the grid i.e. with $y1(t)$.

3. Results

The proposed synchronization system depicted in Fig. 1 was tested by applying a consecutive ramp phase and multiple phase steps as shown in Fig. 2 and Fig. 3 respectively. Fig. 2 shows the phase error response and the phase plane showing that the phase error goes to zero. For the consecutive phase steps test of Fig. 3(a), the phase error and phase plane are shown in Fig. (3b) and (3c) respectively. Again it is evident that the system was successful in achieving synchronization between the grid and the WTG generator.

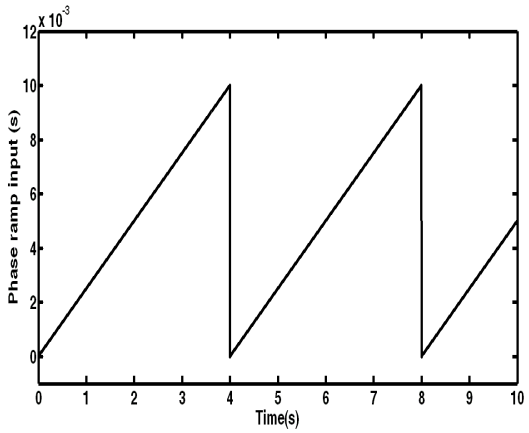

Fig. 2(a). Input ramp phase steps.

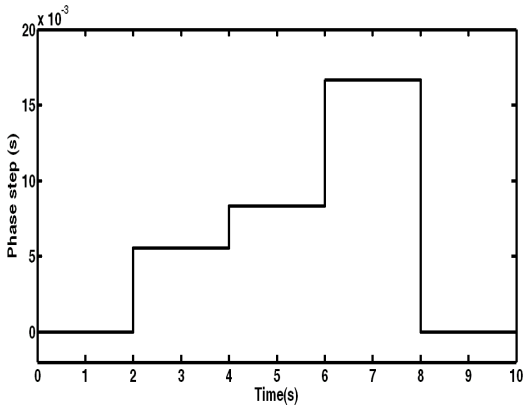

Fig. 3(a) Input multiple phase steps.

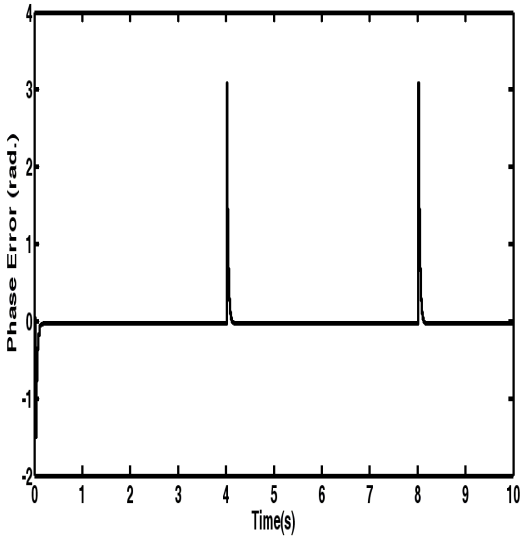

Fig. 2(b) Phase error for the ramp phase step input.

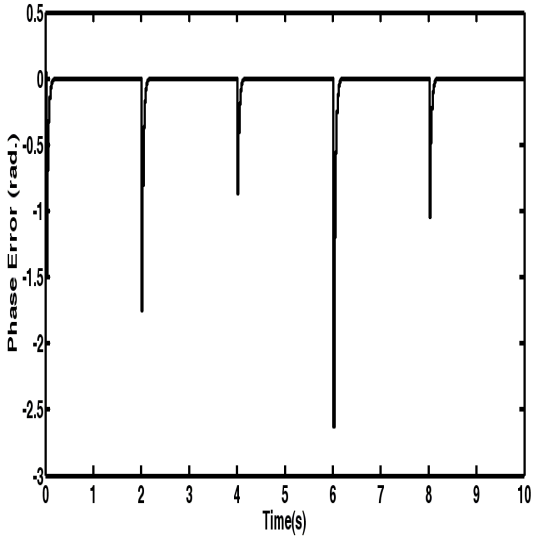

Fig. 3(b). Phase error for multiple phase steps input.

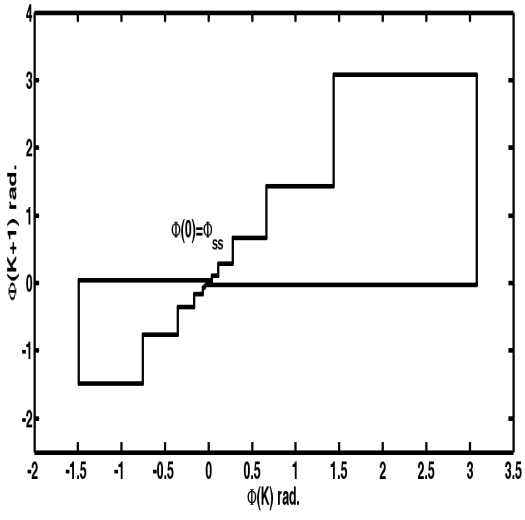

Fig. 2(c) Phase plane for the ramp phase step.

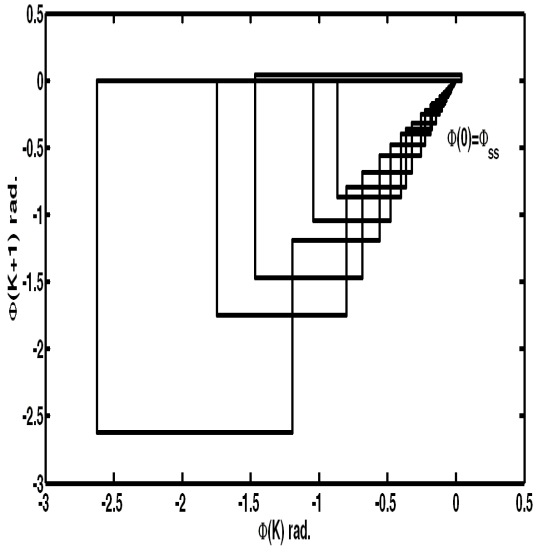

Fig. 3(c) Phase plane for multiple phase steps.

5. Conclusions

A digital phase-locked loop circuit topology based on the time delay digital tanlock loop (TDTL) has been presented. The circuit was simulated and tested using Simulink/Matalb. The circuit was able to synchronise a generator with the grid and re-establish synchronization when the grid voltage was subjected to different perturbations. The results of testing the circuit when the grid voltage was disturbed by applying a sequence of consecutive ramp phase and multiple phase steps were presented. In each case the system took less than 10 ms to achieve synchronization.

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