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Analysis of Current-Bidirectional Buck-Boost Based Switch-Mode Audio Amplifier

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Abstract. The following study was carried out in order to assess quantitatively the performance of the buck-boost converter when used as switch-mode audio amplifier. It comprises of, to begin with, the delimitation of design criteria based on the state-of-the-art solution, which is based in a differential mode buck-based amplifier with a boost converter as power supply. The averaged switch modelling of the differential mode current bidirectional topology is also used, in order to analyze the steady state and frequency-wise behaviour of this converter and parameterize it to meet the design criteria. Next, several piecewise-linear simulation results are shown with detail enough to emphasize the features of the converter. A simple prototype is implemented to verify the main predicted features. Presently no previous publication could be found containing a thorough analysis of this topology in such configuration when applied for audio.

Key words

Boost, losses, modelling, audio, amplifier.

1. Introduction

Despite the advantages featured by the buck-boost converter, no industrial application of this circuit can be found in the literature, using it directly as a DC-AC converter for audio, probably because of the risk of instability due to the right half plane (RHP) zero as well as the non-linearity of the DC gain characteristic, which normally leads to non acceptable distortion in the output.
This task is usually accomplished by a two-stage solution, normally with a buck converter as generator for the AC output.
The use of differential voltage in the load in stead of common voltage is currently applied in the state-of-art solution for automotive audio and will be applied here because of some advantages, as better noise immunity and response to DC much closer to linear in the working duty-cycle region. The converter non-linearity will be addressed in the subsequent article, which will deal with controller design for this specific configuration.

2. Design Considerations

The simulations were all carried out considering equal switch on-state-resistances of 15 mΩ and ESR of the inductor of 5 mΩ. The load was considered equivalent to the series association of an 8 Ω resistor and a 10 µH inductor.

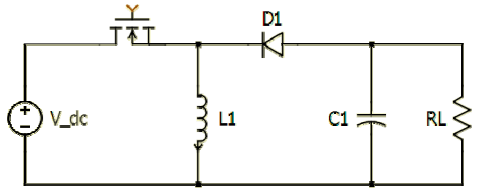

Fig. 1. Classic single-ended, Buck-Boost diagram

The nominally 12 V lead-acid battery works normally at the floating DDP of 14.2 V, and peaks up to 19 V may occur. When the battery voltage goes below 10 V, the audio subsystem must not draw currents higher than 50 A. The subsystem current must be below 40 A when the battery voltage is below 9 V, and not draw any current when is goes lower than 7 V. This means that considering that the system has two 250 W channels, even with purely resistive load, the battery will be able to provide power only enough for the sound system when it's about 10 V, and below this voltage the amplifier shall have a constant maximum gain of 6.32 until the battery voltage reaches 9 V, below which voltage the maximum gain will be reduced to 5.00, and shut down completely when the voltage reaches below 7 V.

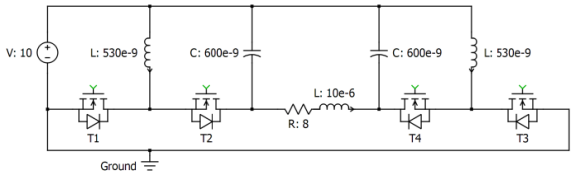

Fig. 2. Inverted, doubled and power-bidirectional version of the Buck-Boost converter

This regime calls for digital control, or a somewhat complex analogue control, but the only information needed for further restrict the design is that the maximum amplifier gain will be 6.32, which will result in an output voltage swing of ±63.2 V (126 Vpp), when the battery voltage is above 10 V. This will be the input voltage used for simulations.

The open-loop power bandwidth of an audio converter shall be designed to be at least of 40 kHz [5], which implies keeping poles and zeroes well away from this frequency.

In addition to the non-linear steady-state gain in relation to the control reference voltage, another challenge for stability is the right half plane zero. In order to determine the frequency of the RHP zeroes, one cannot use the same open loop control-to-output transfer function of the equivalent single-ended converters, because the main ones depend on the load impedance, which in this case consists of another active single-ended converter, connected in series with the passive speaker load [2].

The classical buck-boost topology, when implemented in a bidirectional manner, presents one construction disadvantage, namely the fact that no switches are referenced to ground, i.e. all switches are “high side”. This inconvenience is dealt with by inverting the direction of all voltages and currents of the mentioned circuit, and consequent change of the switch positions, as displayed in figure 2.

3. Summary of Conditions and Specifications

Peak Output Power per channel	250 W
Number of Channels	2
Load Impedance	8 Ω
Maximum load inductance	10 µH
Maximum DC source-to-output gain	6.32
Design Input Voltage	10 V
Open-loop PWM Power Bandwidth	40 kHz
Idle switching frequency	500 kHz
Single-ended input impedance	10 kΩ

4. Design Considerations

Figure 1 represents the single-ended DC-DC converter on which the following bidirectional Double Buck-Boost switch-mode audio amplifier is based.

The output from the Buck-Boost topology at continuous conduction mode ideally [4] has a steady-state modulation-to-output voltage according to

$$\frac{V1}{Vbat} = -\frac{D}{1-D}. \qquad (1)$$

Considering that the negative-side converter will be always driven by the complementary duty-cycle, it is possible to determine that

$$\frac{V2}{Vbat} = -\frac{(1-D)}{1-(1-D)} = -\frac{1-D}{D}$$; so

$$Vo = V1 - V2 = -\frac{Vbat \cdot D}{1-D} + \frac{Vbat \cdot (1-D)}{D}$$;

$$\frac{Vo}{Vbat} = \frac{2 \cdot D - 1}{D \cdot (D-1)}$$ and is the ideal DC transfer function of the complete converter, as shown in the gain vs. duty-cycle graph below:

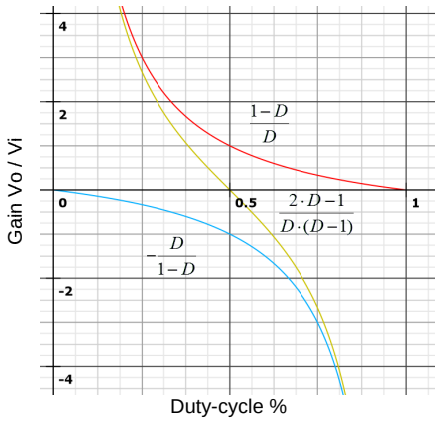

Fig. 3. Nonlinear steady-state control-to-output transfer function of the ideal double-buck-boost converter

The average open-loop control-to-output small-signal transfer function can be accurately determined using average modelling, which allows more simple solutions with low level of abstraction in converter analysis. The differential mode buck-boost converter is represented by the following average small-signal equivalent:

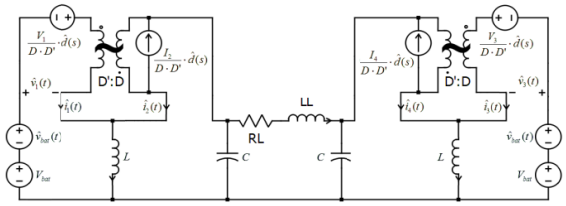

Fig. 4. Averaged small-signal model of the ideal double-buck-boost converter

It is interesting to notice that the single-ended converter on the left side (“positive side”) works with duty-cycle complementary to the one in the right side (“negative side”).

A. Small-signal analysis

For analysis of control dynamics only, the battery voltage oscillation may be bypassed. It is then possible to make use of the superposition theorem and determine the effect of each small-signal source on the output voltage:

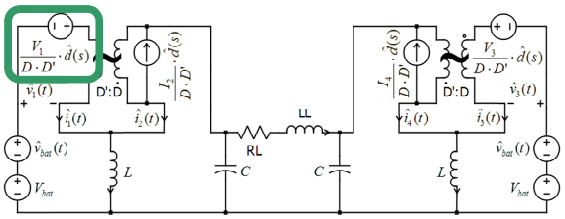

Fig. 5. Emphasizing the small-signal voltage source for the superposition

$$-(i4 + i3)\,Ls - v3 = 0$$

$$-\frac{-i4+io}{s\,C}+v4+(i4+i3)\,L\,s=0$$
$$-\frac{-i2-io}{s\,C}+io\,(RL+LL\,s)+\frac{-i4+io}{s\,C}=0$$
$$-(i1+i2)\,L\,s-v2+\frac{-i2-io}{s\,C}=0$$
$$-\frac{V1\,ds}{Du\,Di}+v1+(i1+i2)\,L\,s=0$$

$$i1\,Di=i2\,Du$$
$$i3\,Du=i4\,Di$$
$$v1\,Du=-v2\,Di$$
$$v3\,Di=-v4\,Du$$

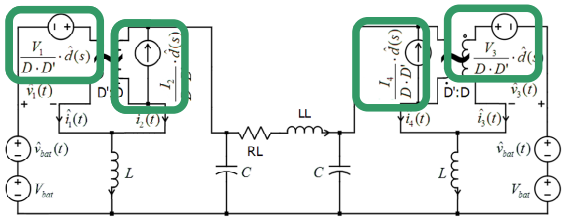

Fig. 6. Emphasizing the sources used for determination of control-to-output small signal transfer function

Adding up the found load current makes it possible to determine the total load voltage and the expression for the small-signal open-loop control-to-output transfer function.

This expression represents the control-to-output transfer function, where (vo/Vbat) represents the voltage gain of the amplifier, and ds a small variation in the duty cycle. Apart from the Laplace variable s, the right-hand side contains only constants, where Du is the duty cycle and Di is the complementary duty-cycle (1 – Du). L represents the inductance of both inductors and C the capacitance of both capacitors. RL is the load resistance and LL load inductance. V1 and V3 are the average ideal transformer voltages at the source side, and I2 and I4 the average transformer currents at the load side.

B. Steady-state transfer function with parasitic resistive elements

The same averaging technique can be used to determine the steady-state average output voltages and inductor currents. Eliminating all sources of disturbance in the small-signal model, the following diagram is obtained.

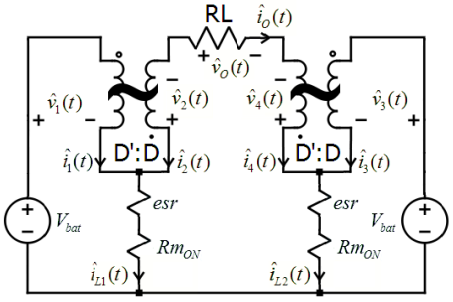

Fig. 7. DC averaged-switch model of the double buck-boost converter

The obtained steady-state voltage gain, considering the conductive losses is:

$$\frac{Vo}{Vbat}=\frac{(-1+2\,D)\,(-1+D)\,Rrel\,D}{(D^2-2\,D^3+D^4)\,Rrel+2\,D^2+1-2\,D}$$

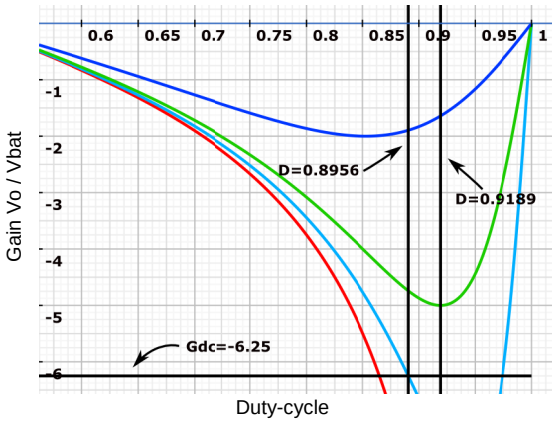

Fig. 8. Minimum possible resistance relations needed to achieve design criteria with steady state output

The results displayed in figure 8 are very important also to show that the points of maximum DC gain must be carefully determined, because if the switches are driven within certain duty-cycle values above or below the maximum and minimum gains for a time larger than the settling time with closed loop, the controller may encounter instability.

5. Conduction Losses

The theoretic maximum achievable efficiency of the converter can also be determined using the same model, considering the ratio between input and output power as follows:

$$P_o=\frac{G_{DC}{}^2\cdot V_{BAT}{}^2}{R_L};\qquad(2)$$

The inductor core loss, in the optimal case, can be considered of same magnitude as the inductor conduction loss [11].

$$P_{loss}=\left(I_{1RMS}+I_{2RMS}\right)^2\cdot\left(Rm_{ON}+2\cdot esr\right)\qquad(3)$$

With neglectable inaccuracy, the variations in the inductor current can be considered linear, leading to

$$\Delta I_1=\frac{D}{2}\cdot\frac{\left(V_{bat}-I_1\cdot R_{esr}\right)}{F_{SW}\cdot L}\qquad(4)$$

The average inductor current is obtained from the DC analysis in the previous section, ignoring the parasitic resistances to avoid further complexity.

$$I_1=\frac{V_{bat}\cdot(2\cdot D-1)}{R_L\cdot D^2}\qquad(5)$$

For a periodical output voltage, the average maximum achievable power efficiency may be then estimated as:

$$\eta_{\max}=Fo\cdot\int_T^{T+\frac{1}{Fo}}\left(I_{1RMS}+I_{2RMS}\right)^2\cdot\left(Rm_{ON}+2\cdot esr\right)\cdot dt$$

6. Switching Losses

The work required to move a certain charge between the conductors of a capacitor is given by:

$W_C = \int_{q=0}^{Q} V_C \cdot dq = \frac{1}{2} \cdot \frac{Q^2}{C} = \frac{1}{2} \cdot C \cdot {V_C}^2$, where V_C is the resulting voltage change.

In the case of Cgs this voltage change is fixed and independent of the drain-to-source voltage. According to the previous expression, the contribution of this capacitance to the switching energy losses will be $W_{GS} = C_{GS} \cdot {V_{GS}}^2 \cdot N_{sw.cycles}$, considering the total number of switching cycles in the period.

The magnitudes of the single-end voltages change, considering the relation between common mode and differential voltages can be expressed by:

$$\left|\Delta V_{DS}\right| = \frac{2 \cdot Vo \cdot V_{bat}}{Vo - 2 \cdot V_{bat} + \sqrt{Vo^2 + 4 \cdot V_{bat}^2}} \quad (6)$$

The same voltage excursion occurs in the parasite Cgd capacitors, even considering the gate-to-source voltage change.

For an Fo Hz sinusoidal output voltage with peak amplitude Vpk, with switching frequency Fsw, it's possible do determine the total energy spent in voltage cycling one Cgd capacitor in one entire Fo cycle, ignoring the difference between the ripple voltages of two switching semi-cycles:

$$E_{DS} = \sum_{N=0}^{\left(\frac{Fsw}{Fo}\right)} 2 \cdot C_{DS} \cdot \left(\frac{2 \cdot Vo_N \cdot V_{bat}}{Vo_N - 2 \cdot V_{bat} + \sqrt{Vo_N^2 + 4 \cdot V_{bat}^2}} \right)^2,$$

$$Vo_N = Vpk \cdot \sin\left(2 \cdot \pi \cdot N \cdot \tfrac{Fo}{Fsw}\right)$$

And this expression can be used to determine the average power loss as:

$$P_{DS} = Fo \cdot \sum_{N=0}^{\left(\frac{Fsw}{Fo}\right)} 2 \cdot C_{DS} \cdot \left(\frac{2 \cdot Vo_N \cdot V_{bat}}{Vo_N - 2 \cdot V_{bat} + \sqrt{Vo_N^2 + 4 \cdot V_{bat}^2}} \right)^2 \quad (7)$$

At turn off time, the input switch is conducting the peak inductor current, and is subject to the output voltage plus battery voltage. Considering that the current transitions occur linearly, the energy released as heat during each crossover time is:

$$W_{DSc} = \frac{1}{2} \cdot V_{DS} \cdot I_{PK} \cdot t_c \quad (8)$$

Applying equations (4) and (5) from the previous section, the peak inductor current is determined:

$$I_{PK} = \frac{V_{bat} \cdot (2 \cdot D - 1)}{RL \cdot (D-1)^2} + \frac{D \cdot (V_{bat} - I1 \cdot R_{esr})}{2 \cdot F_{SW} \cdot L} \quad (9)$$

Expression (10) can be modified to sum up the total energy and obtain the crossover power loss in sinusoidal operation:

$$P_C = Fo \cdot \sum_{N=0}^{\left(\frac{Fsw}{Fo}\right)} V_{DS(N)} \cdot I_{PK(N)} \cdot t_c$$

7. Choice of Passive Components

We may consider that a converter with power bandwidth of 40 kHz is one that can reproduce sinusoidal waveform with this frequency, at rated output voltage, in the present case $2 \cdot Vbat \cdot Gdc$, 126 Vpp.

The system could achieve the required voltage swing dynamically, but to stay on the safe side, it is better to consider that the required slew rates are obtained with slope-steady voltages. This can be interpreted as a requirement that the output voltage should stabilize at the same speed, or faster, than the slew rate of the considered sinusoidal waveform.

Another concern should be stability, which, if approached with a classical point of view, would make believe that the system is unstable, because of zeroes with positive real part, along with some other features. The simulations, however, prove the system is convergent for a wide range of filter values and operating points.

These criteria gives limit to the highest possible values for capacitors and inductors, but puts no limit to how fast and accurate the system can be, as long as the resulting input ripple currents and output ripple voltages are tolerated.

Figure 9 shows one possible bode plot of the obtained small-signal transfer function, using the design conditions and arbitral passive components:

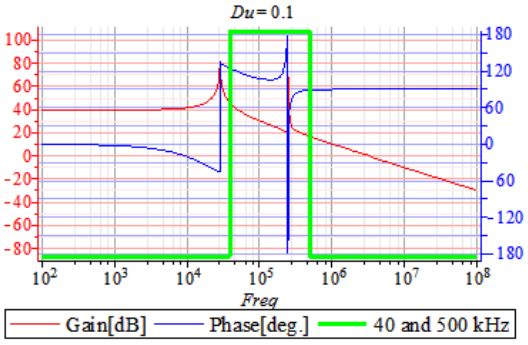

Fig. 9. Frequency response of the double buck-boost at an extreme duty-cycle.
Gain scale to the left, phase scale to the right

Further analytical evaluation makes possible to determine the imaginary portion of the two pairs of complex poles, and demonstrates that the resonance peaks happen at the following frequencies:

$$\omega 0_a = \frac{(1-D)}{\sqrt{L \cdot C}} \quad (10)$$

$$\omega 0_b = \frac{D}{\sqrt{L \cdot C}} \quad (11)$$

The relation between the passive components has to be, consequently,

$$L \cdot C = \frac{D^2}{(\omega_s - \omega_{rip})^2}, \quad (12)$$

being ω_s the switching frequency and ω_{rip} the distance taken to reduce the output voltage ripple.

Taking for instance the fixed switching frequency of 500 kHz and the required maximum duty-cycle 0.88 obtained from the DC analysis, and a distance from the switching frequency of it's half,

$$L \cdot C = 3.16 \cdot 10^{-13} \tag{13}$$

Thus placing the lower resonance frequency according to equation (5), at

$$\omega 0_a = \frac{(1 - 0.8829)}{\sqrt{3.1592 \cdot 10^{-13}}} = 208.34\, krad/s = 33{,}2\, kHz$$

As an additional criterion, neglecting parasite resistances, the inductor current ripple over the average inductor current, may be represented by the following expression:

$$\Delta i_L = \frac{V_{bat} \cdot D}{F_{SW} \cdot L}, \tag{14}$$

Arbitrating a peak ripple of 50% above the average inductor current obtained from the DC analysis, the given example results in an inductance L = 0.53 µH and capacitance C = 0.60 µF

8. Open Loop Sensitivity to Battery Voltage Oscillations

It is important also to determine the need for input filters in the amplifier. Using the averaged switch method makes it also possible to determine the transfer function from variations in the battery voltage to the differential output of the converter, and have a bode plot of this function.

The following bode plot uses the values obtained in the previous section:

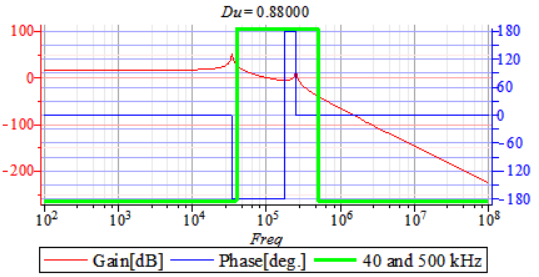

Fig. 10. Frequency response plot for verifying the effect of input voltage variations

9. Simulation Results

The control was performed using simple open-loop 500 kHz PWM with a sinusoidal reference waveform, making the duty cycle vary according to a sinus wave compensated with the inverse steady-state transfer function of the converter, in order to obtain a linear open-loop response, and consequently generating a sinus output voltage Vo with average in zero volts. Switches T1 and T3 turn on together, complementarily with T2 and T4. All simulation results are displayed oscilloscope-like, The following voltage vs. time graph shows the common mode V1 and V2 outputs (green and red) from the circuit above with a 1 kHz reference waveform, for comparison with the Vbat voltage, in blue.

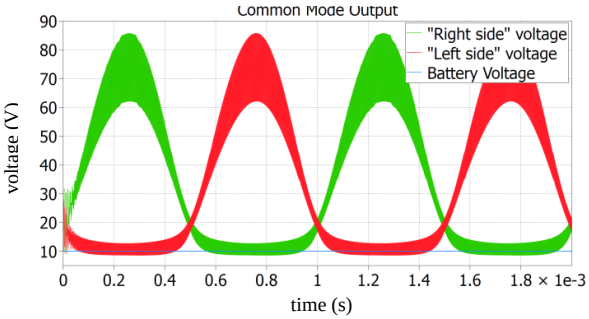

Fig. 11. Common mode voltages from simulation

Follows the voltage vs. time graph of the resulting differential output voltage Vo (red), also compared with Vbat (blue):

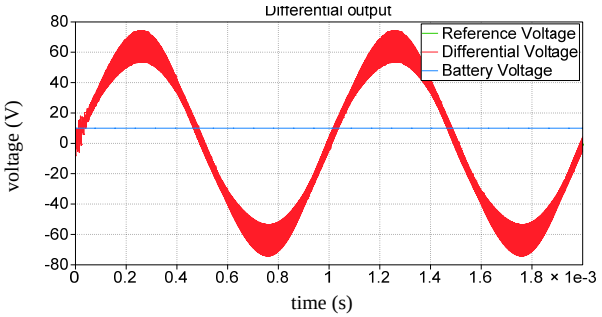

Fig. 12. Differential mode voltage from simulation

The current in the inductors determine inductor design, and the EMI generated by them. Next are shown the inductor current waveforms in the same period of time shown before, at peak output power, along with the current in the load (blue), for comparison.

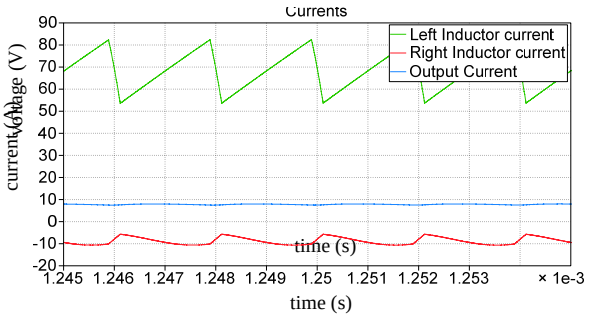

Fig. 13. Inductor currents at peak power

Inductor currents peak at 84.6 A and have a maximum peak-to-peak value of 28.9 A. Furthermore the RMS current at both inductors is 30.6 A, considering an entire low-frequency cycle at peak output power.

10. Experimental Verification

A simple mini mount prototype was performed in order to verify real operational details.

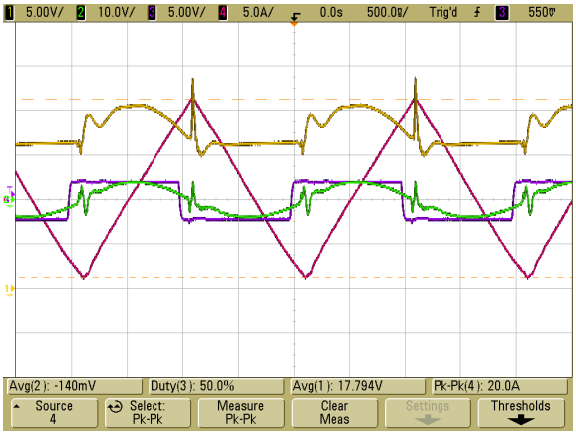

Fig. 14. Measurements at idle power

The oscilloscope picture above shows, from channel 1 to 4, differential output voltage, PWM reference and left inductor current, respectively.

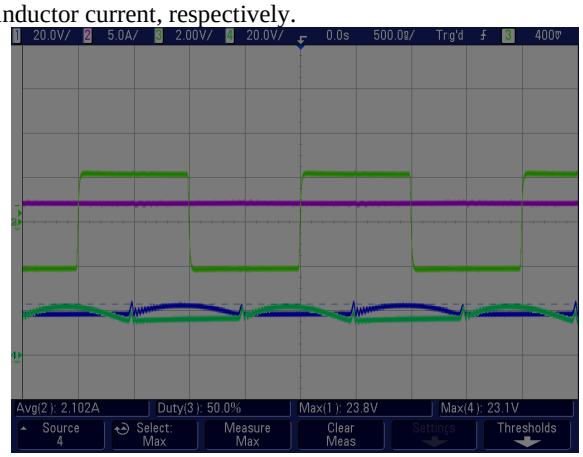

Fig. 15. Measurements at idle power

Figure 15 displays the common mode output voltages at idle, channels 1 and 4, along with the averaged input current at channel 2. Follow the same measurements at peak power, in figure 16.

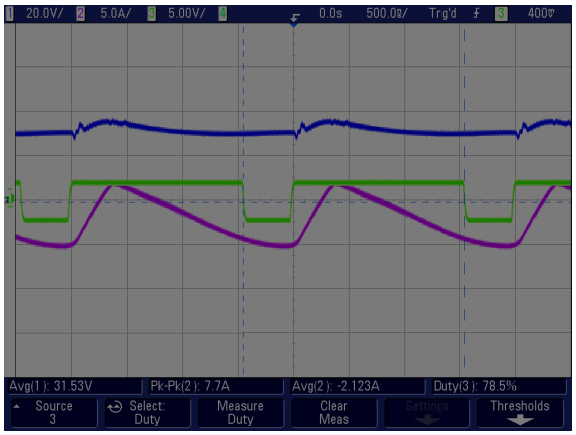

Fig. 16. Measurements at peak power

11. Conclusion

The possibility of using the buck-boost converter in symmetrical doubled differential mode configuration for application as audio amplifier was studied. Averaged switch modelling was employed was employed to obtain estimations about conductive and switching losses, as well as an estimative of the overall efficiency of the converter.

The same modelling strategy was employed to determine small-signal wise the optimum passive components in order to realize a class-D amplifier capable of delivering 250 W to an 8 Ω inductive speaker for full audio bandwidth.

The small signal study proved that, in open-loop operation, this topology is not capable of delivering full audio bandwidth at the rated power level, due to the fixed distance between the poles for a given gain level. Simulations were conducted, considering the parasitic elements, in order to validate the estimations.

A simple mini mount prototype was performed, in order to verify differences in the operation due to non-idealities. Some were observed, as asymmetrical inductor currents due to different inductances, and a sensible decrease in the voltage gain as the dead time increases.

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