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Research On 400Hz Input Multi-Level PFC Techniques

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Abstract. Input current distortion in the vicinity of input voltage zero crossings is a major concern for conventional single-phase Boost PFC applications, especially under high ac line frequencies. This paper discusses the previously known causes for the input current distortion and points out that the multi-level power conversion technique can effectively reduce the zero-crossing distortion under high frequencies. A three-level (TL) Boost converter containing flying capacitors is then presented as the PFC topology. The system control method of the converter is also discussed. Experimental results are presented to validate the effectiveness of the proposed method.

Key words:

PFC, zero-crossing distortion, high frequency input, phase shift, multi-level converters

1. Introduction

In recent years, the application of power electronics has enabled the rapid development of power factor correction (PFC) technology. The single-phase boost converter has been widely used as the front-end single-phase PFC converter due to its low input current ripple, high output voltage, simple topology, high reliability and low cost. On the other hand, it has been widely observed that the input current of single-phase PFC converters almost always contains some residual distortion, especially under high ac line frequencies.

Cusp distortion and discontinuous conduction mode (DCM) of operation of the Boost inductor have been considered as the two major causes for the zero-crossing distortion in single-phase PFC converters[1]. The cusp distortion occurs right after the input voltage crossover where there is very limited voltage across the boost inductor to drive its current up. As the result, the inductor current may not be able to follow the reference for a short time period after the zero crossing, causing the current distortion. While the inductor current is discontinuous, the lower current loop gain and the smaller bandwidth can deteriorate the input current response. And finally, it becomes more difficult for the inductor current to follow the reference. In addition, the leading-phase effect and the lack of critical damping in the current loop also add to the predominant causes for the zero-crossing distortion under high input line frequencies. Both causes are shown to be related to fundamental characteristics of converter dynamics.

To sum up, the causes of zero-crossing distortion are analyzed in detail in the next section along with a suitable solution: the multi-level power conversion technique. The characteristics and control strategies of the multi-level converter containing flying-capacitors are then discussed in section 3. Experimental results to validate the effectiveness of the proposed methods are presented in section 4.

2. Zero-crossing Distortion

A. Analysis on the process of zero-crossing distortion

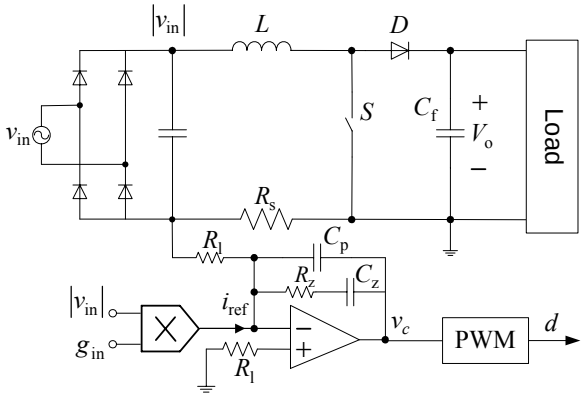


Fig.1. Boost single-phase PFC converter with average current control

Fig.1 depicts a typical boost single-phase PFC converter with average current control. Note that the output voltage feedback loop is not considered here, as the voltage loop has nothing to do with the current loop in steady state when properly designed. In that case, the following input current to input voltage transfer function can be expressed as[2]:

$$\frac{\hat{i}_L(s)}{\hat{v}_{in}(s)} = \frac{g_{in}R_l}{R_s} \cdot \frac{1 + s\left(\frac{1}{\omega_z} + \frac{1}{K_c} + \frac{R_s}{gR_lL\omega_n^2}\right)}{D(s)} \quad (1)$$

where: $K_c = \frac{1}{(C_p + C_z)R_l}$, $\omega_n = \sqrt{\frac{R_sV_oK_c}{LV_m}}$, $\omega_z = \frac{1}{C_zR_z}$.

Therefore, the leading phase angle of the input current , θ, can be obtained:

$$\theta(\omega)=\tan^{-1}\frac{\left(1-\frac{\omega^2}{\omega_n^{\ 2}}\right)\left(\frac{\omega}{\omega_z}+\frac{\omega}{K_c}+\frac{V_m}{g_{in}V_o}\cdot\omega(C_p+C_z)\right)-\frac{\omega}{\omega_z}}{1-\frac{\omega^2}{\omega_n^{\ 2}}+\frac{\omega^2}{\omega_z^{\ 2}}+\frac{V_m}{g_{in}V_o}\cdot\omega(C_p+C_z)\cdot\frac{\omega}{\omega_z}} \quad (3)$$

Next, Fig.2 is taken as an example to analyse the process of zero-crossing distortion.

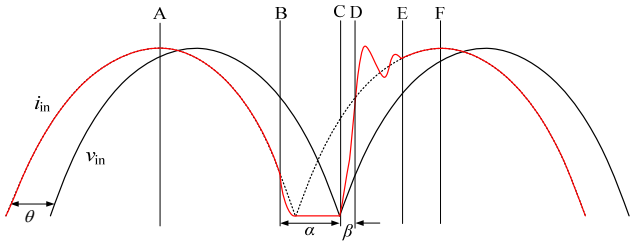


Fig. 2. Input current zero-crossing distortion

1) From A to B. the waveform of the input current contains no distortion.

2) From B to C. At point B, the current of the boost inductor falls down to a relatively low value, causing the discontinuous conduction. The input current and the output voltage then can't reverse their direction due to the diode bridge rectifier. As a result, the input current will be clamped at zero. The length of the converter under DCM operation is α.

3) From C to D. The inductor current should follow up the reference instantaneously right after point C. By this moment，the current rising rate provided by the converter can reach: $V_m \sin\omega t / L$, while the required current rising rate can be expressed as:

$$\frac{d}{dt}\left[I_m \sin(\omega t+\theta)\right]=\omega I_m \cos(\omega t+\theta) \quad (3)$$

As can be seen, the required current rising rate will become bigger as the input line frequency increases. Assuming that the needed angle to follow up the reference current equals β, yields:

$$\frac{V_m}{\omega L}(1-\cos\beta)=I_m \sin(\beta+\theta) \quad (4)$$

4) From D to E. The admittance eigen function of the converter becomes: $D(s)=1+s/\omega_z+s^2/\omega_n^2$. The current compensator zero, ω_z, is usually placed at the crossover frequency, $\omega_z=\omega_c$, in order to maximize the loop gain in the low-frequency region and to ensure a 45°phase margin. Therefore, $\omega_z=\sqrt[4]{2}\omega_n$, and the damping factor is $\xi=\omega_n/2\omega_z=0.42<0.707$. As such, the current response will be characterized by overshoot and possibly oscillation, following a typical trajectory of second-order systems, due to the lack of critical damping factor.

5) From E to F.The inductor current waveform returns to normal, and is identical to the reference.

B. Resolutions

As mentioned before, the length of DCM, α, will reduce according to the decrease of θ, due to a necessity that $\alpha<\theta$. Besides, the current oscillation angle is only related to β under a given value of critical damping factor. Therefore, the zero-crossing distortion problem can be effectively eliminated by reducing θ and β.

3. Multi-level Converters

Equation (2) indicates that, in order to achieve a constant θ under the varied high input line frequency, the following expressions: ω/ω_z， ω/ω_n and $\omega(C_p+C_z)$ must be kept as fixed values, meaning a reduction in L, C_p and C_z. When reducing β, the value of L must be reduced accordingly so as to lower the required current rising rate of the converter. Due to the harmonic current restrictions and system stability requirements, the equivalent switching frequency must be improved accordingly as the values of L, C_p and C_z are reduced.However, the switching frequency is limited by devices and magnetic core. The multi-level converter can improve the equivalent switching frequency and decrease inductance without increasing the switching frequency, as shown in Table I. Therefore, the multi-level converter is adopted as the main topology.

Table I. – Comparison between multi-level converters and conventional converters

Converter	Inductor size	Equivalent Switching Frequency
Boost	L	f_s
(n+1) Boost	L/n^2	nf_s

A. The Form of Flying-capacitor Boost ML Converter

Fig.3 depicts the main circuit of a typical Boost n+1 level PFC converter. The basic unit (the dashed frame) comprise of a switch, Q_k, a diode, D_k and a flying capacitor C_k. The Q_k and D_k are conducted alternatively. Likewise, each switch is conducted one by one following a phase shift of $2\pi/n$. The voltage of the flying capacitor C_k (k=1, 2,……,n-1) will be automatically stabilized at kV_o/n under the same duty ratio of each switch. When Q_k or D_k is turned off, the Q_k or D_k bears a voltage difference of two flying capacitors nearby. As can be seen, the switches of multi-level converter endure a lower voltage stress than that of the conventional Boost converter.

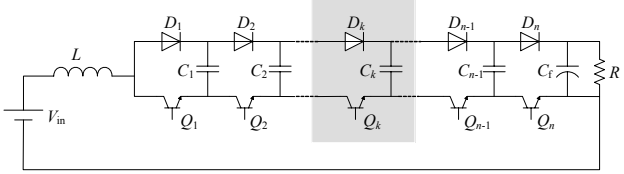


Fig. 3. Flying-capacitor Boost ML converter

The operation modes of the converter are as following:

1) Operation mode 1—— $d\in(0,1/n]$

Assuming the duty ratio, d ,is located in [0,1/n], no more than one switch of converter can be conducted.

For only one switch is turned on, the boost inductor charging voltage is V_{in}-(n-1)V_o/n. The inductor current will follow a linear increase:

$$\Delta i_{L(+)}=\frac{(V_{in}-\frac{n-1}{n}V_o)}{L}\cdot d\cdot T_s \quad (5)$$

When the switch is turned off， the boost inductor discharging voltage becomes V_{in}-V_o， and inductor current will follow a linear decrease:

$$\Delta i_{L(-)} = \frac{V_o - V_{in}}{L} \cdot (\frac{1}{n} - d) \cdot T_s \quad (6)$$

where $\Delta i_{Lf(+)}$=$\Delta i_{Lf(-)}$ holds under steady state. Integrating equation (1) and (2), we have:

$$V_o / V_{in} = 1/(1-D) \quad (7)$$

2) Operation mode n——d ∈[(n-1)/n,1)

For $d \in [(n\text{-}1)/n,1)$， no less than n-1 switches can be conducted at the same time.

When there are n switches conducting simultaneously, the boost inductor charging voltage changes to V_{in}. The inductor current will follow a linear increase:

$$\Delta i_{L(+)} = \frac{V_{in}}{L} \cdot (d - \frac{n-1}{n}) \cdot T_s \quad (8)$$

While Q_1,Q_2,…,Q_n is turned off in sequence， the boost inductor discharging voltage becomes V_{in}-V_o/n ， and inductor current will follow a linear decrease:

$$\Delta i_{L(-)} = \frac{V_o / n - V_{in}}{L} \cdot (1-d) \cdot T_s \quad (9)$$

where $\Delta i_{Lf(+)}$=$\Delta i_{Lf(-)}$ holds under steady state. Integrating equation (4) and (5), thus:

$$V_o / V_{in} = 1/(1-D) \quad (10)$$

3) Operation mode k——d ∈[(k-1)/n, k/n] (k=2,3,…,n-1)

For $d \in [(k\text{-}1)/n,k/n]$, there are k-1 or k switches conducting at the same time.

When there are k switches conducting simultaneously, the boost inductor charging voltage changes to V_{in}-$(n\text{-}k)V_o/n$. The inductor current will follow a linear increase:

$$\Delta i_{L(+)} = \frac{V_{in} - (n-k)V_o / n}{L} \cdot (d - \frac{k-1}{n}) \cdot T_s \quad (11)$$

When there are only k-1 switches conducting, the boost inductor discharging voltage changes to V_{in}-$(n\text{-}k\text{+}1)V_o/n$. The inductor current will follow a linear decrease:

$$\Delta i_{L(-)} = \frac{(n-k+1)V_o / n - V_{in}}{L} \cdot (\frac{k}{n} - d) \cdot T_s \quad (12)$$

where $\Delta i_{Lf(+)}$=$\Delta i_{Lf(-)}$ holds under steady state. Integrating equation (4) and (5), therefore:

$$V_o / V_{in} = 1/(1-D) \quad (13)$$

As can been seen from equation (7)、(10) and (13), the input-output voltage relation is invariant under any kind of operation mode.

B. The Control Methods of Boost TL PFC Converter

The PFC control methods of the circuit topology based on flying-capacitor Boost TL converter are presented in this section.

The duty ratio of two switches can't completely equal to each other in a real circuit due to the different characteristics, causing an imbalance in flying capacitor voltage. Therefore, a close-loop control is called for the flying capacitor voltage balancing[3],[4].

Next, a control method to decouple the flying capacitor voltage from the input voltage loop is presented[5]. Since there is only one flying capacitor in Boost TL converter, thus the control method becomes very simple. The analysis process is as following:

The voltage change of flying capacitor C_1 over one switching cycle can be expressed as:

$$\Delta V_{C_1} = \frac{T_s}{C_1} \cdot I_{C_1} = \frac{T_s}{C_1}\left(I_{Q_2} - I_{Q_1}\right) = \frac{I_L \cdot T_s}{C_1}\left(d_2 - d_1\right) \quad (14)$$

Defining: d_1=d+Δd_1, d_2=d+Δd_2, yields：

$$\Delta V_{C_1} = \frac{I_L \cdot T_s}{C_1}\left(\Delta d_2 - \Delta d_1\right) \quad (15)$$

As can be seen, $G_{v_o d_2} = G_{v_o d_1}$. Therefore, the decoupling control of the flying capacitor voltage and the input voltage can be achieved, where the regulation of flying capacitor voltage has no impact on output voltage, as long as the equation $\Delta d_1 = -\Delta d_2$ or $\Delta d_1 + \Delta d_2 = 0$ is ensured.

The voltage balancing control circuit is added to the Boost TL PFC converter based on the above analysis, as shown in Fig. 4:

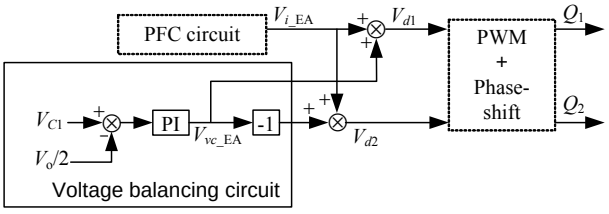


Fig. 4. The PFC control diagram with voltage balancing circuit

Fig. 4 depicts the control method of voltage balancing loop: For V_{C1}>V_o/2, the error amplifier in voltage balancing loop produces a positive output signal, V_{vc_EA}, which adds to the PFC control output, V_{i_EA}, thus causing a higher V_{d1}. As a result, the duty ratio of Q_1 will increase accordingly. On the other hand, the inverted signal, V_{vc_EA}, will add to V_{i_EA}, causing a lower V_{d2}, along with an decrease in the duty ratio of Q_2.Thus, D_1>D_2 , therefore, the value of V_{C1} will decrease. On the contrary, for V_{C1}< V_o/2, V_{vc_EA} changes to a negative value, causing a lower V_{d1} and a higher V_{d2} along with an decrease in D_1 and an increase in D_2, so that D_1< D2 , therefore, the value of V_{C1} will increase. In summary, the voltage balancing control circuit can revise the duty ratio according to the change in flying capacito voltage, therefore, the voltage balancing of flying capacitor, V_{C1}=V_o/2, can be achieved.

C. The Control Methods of Boost TL PFC Converter

Fig. 5 shows the small signal model of Boost TL PFC converter when the voltage balancing compensator is adopted.

Defining H_{v2} is the transfer function of voltage balancing compensator. k_c is the adjustment coefficient of duty ratio. As can be seen from Fig. 5, the current loop, voltage loop and voltage balancing loop couple with each other, causing a challenge for closed loop designing, therefore decoupling control is needed to simplify these three loops.

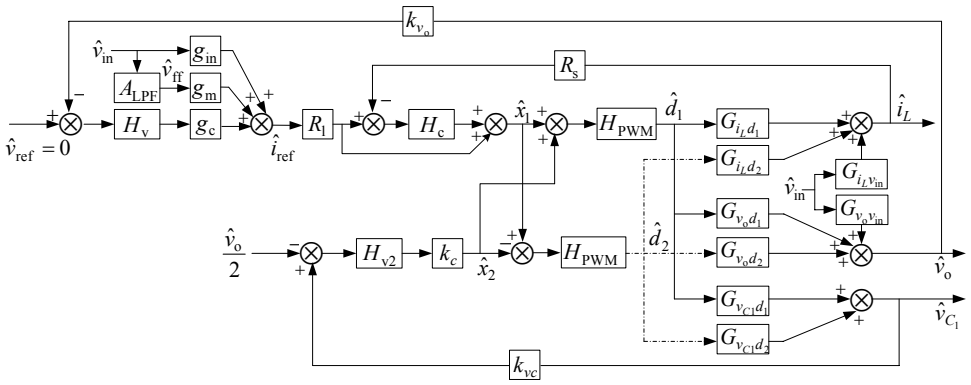


Fig. 5. The small signal model of Boost TL PFC converter

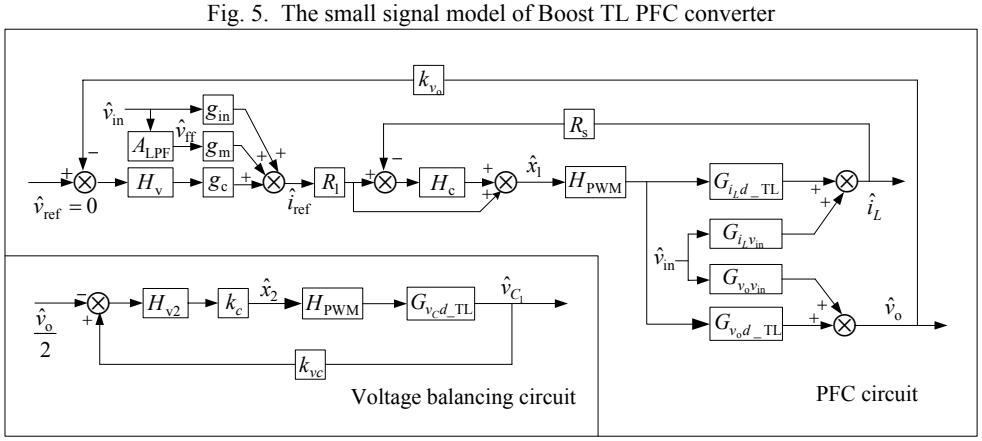


Fig. 6. The small signal model of the decoupled converter

Defining:

$$G_{v_o d_1} = G_{v_o d_2} = \frac{1}{2} G_{v_o d\_TL}, \quad G_{i_L d_1} = G_{i_L d_2} = \frac{1}{2} G_{i_L d\_TL},$$

$$G_{v_C d_1} = -G_{v_C d_2} = \frac{1}{2} G_{v_C d\_TL},$$

From Fig. 5, we have:

$$\hat{d}_1 = H_{PWM} \cdot (\hat{x}_1 + \hat{x}_2) \tag{16}$$

$$\hat{d}_2 = H_{PWM} \cdot (\hat{x}_1 - \hat{x}_2) \tag{17}$$

$$\hat{i}_L = G_{i_L d_1} \hat{d}_1 + G_{i_L d_2} \hat{d}_2 + G_{i_L v_{in}} \hat{v}_{in} \tag{18}$$

$$\hat{v}_o = G_{v_o d_1} \hat{d}_1 + G_{v_o d_2} \hat{d}_2 + G_{v_o v_{in}} \hat{v}_{in} \tag{19}$$

$$\hat{v}_{C_1} = G_{v_{C1} d_1} \hat{d}_1 + G_{v_{C2} d_2} \hat{d}_2 \tag{20}$$

Equations above can be simplified as:

$$\hat{i}_L = G_{i_L d\_TL} \cdot H_{PWM} \cdot \hat{x}_1 + G_{i_L v_{in}} \hat{v}_{in} \tag{21}$$

$$\hat{v}_o = G_{v_o d\_TL} \cdot H_{PWM} \cdot \hat{x}_1 + G_{v_o v_{in}} \hat{v}_{in} \tag{22}$$

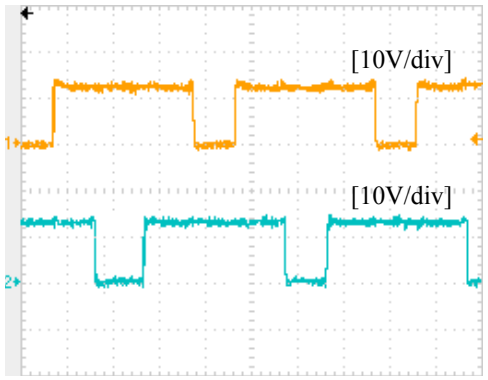
$$\hat{v}_{C_1} = G_{v_C d\_TL} \cdot H_{PWM} \cdot \hat{x}_2 \tag{23}$$

Hence, the small signal model of the decoupled converter can be obtained, as shown in Fig. 6.

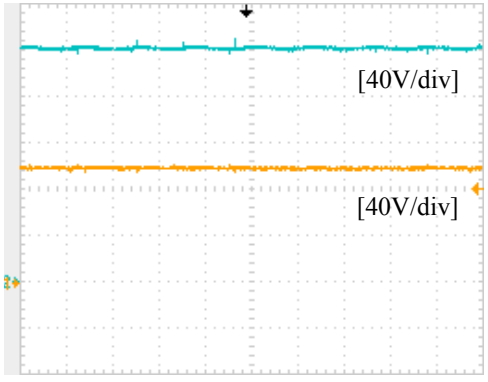
4. Experimental Verification

Prototype of a 250W flying-capacitor Boost TL converter is built in our lab to verify the effectiveness of the proposed method. The converter has the following parameters: V_{in}=115V±10%AC, f_{in}=400Hz, V_o=200VDC, f_s = 100kHz.As for the circuit parameters: L=0.35mH, C_1=5.6uF, C_f=220 uF, R_s=0.15Ω.

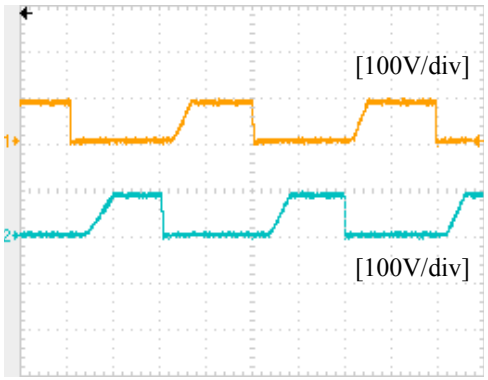
Fig.7 shows the experimental results of Boost TL PFC converter. As can be seen from Fig.7-(a), the driving signals of Q_1 and Q_2 are interleaved with a 180° phase-shift, while the voltage of flying capacitor C_1 is half that of the output voltage in Fig.7-(b). As the result, the voltage stresses of both switches can be automatically balanced at 100V.



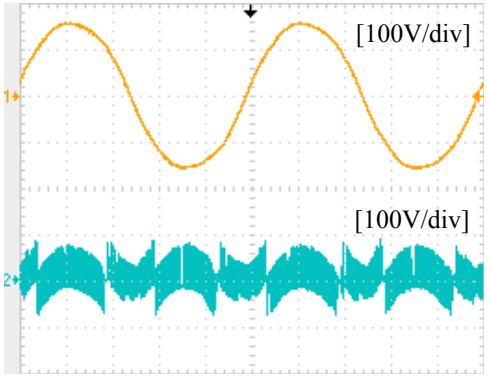
(a) d_1 and d_2



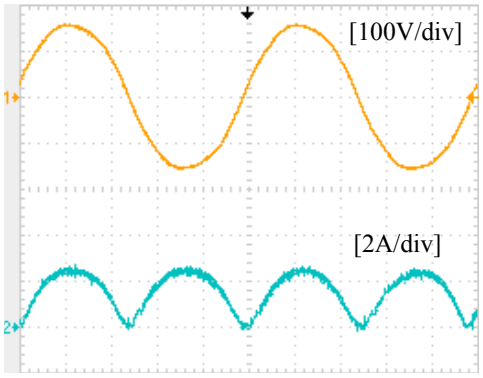
(b) v_o and v_{C1}



(c) v_{DS} of Q_1 and Q_2



(d) v_{in} and v_L



(e) v_{in} and i_{in}

Fig.7. Experimental results of Boost TL PFC converter

Fig.7-(d) and (e) shows the waveforms of the inductor voltage, v_L and the input current, i_{in}. When the input voltage is close to zero, the input current will be clamped at zero. The input current contains some distortions around zero crossings of the input voltage, which is not severe under the ac line frequency of 400Hz.

5. Conclusion

The zero-crossing distortion of input current should be considered a predominant issue for most high-power applications with 400Hz inputs as far as meeting regulatory requirements is concerned. Since θ and β are considered the two major causes for the zero-crossing distortion in single-phase PFC converters, reducing the value of θ and β can effectively reduce the zero-crossing distortion. The multi-level converter can improve the equivalent switching frequency and decrease inductor without increasing the switching frequency, so that the value of θ and β are decreased, therefore, the zero-crossing distortion is effectively reduced. At last, experimental results are given to verify the effectiveness of the proposed method.

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