European Association for the Development of Renewable Energies, Environment and Power Quality (EA4EPQ)

International Conference on Renewable Energies and Power Quality (ICREPQ'11)
Las Palmas de Gran Canaria (Spain), 13th to 15th April, 2011

A Novel Method to Eliminate Negative Time Period of SVPWM using DSP TMS320F2812

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Abstract: **Conventional SVPWM method generates negative time period during lower switching frequency at higher voltage magnitudes. This paper presents a simplified method for implementation of Space Vector PWM technique for two level VSI using DSP TMS320F2812. Methodology presented is to implement SVPWM without lookup table and to calculate time periods independent of voltage magnitude. Experimental results show that proposed method overcomes problem of negative time period for said conditions. An experimental setup is developed in the laboratory around TMS320F2812 to obtain and verify the desired results. This work is a part of project titled "Development of FPGA-DSP Controlled Multilevel Inverter Interface for Grid connection of Wind Turbine Generators" funded by AICTE New Delhi.**

Keywords: Voltage **source inverter, Space Vector PWM, DSP TMS320F2812.**

I. INTRODUCTION

Power quality is the major issue in the power system. As the complexity of power system increases, power quality gets affected due to switching circuits. Thus, it is necessary to develop optimized control technique for inverter switches to achieve quality output voltage of desired amplitude and frequency. The efficiency of the inverter depends on the efficiency of the control technique involved in switching the power transistors. With PWMs, the inverter can be thought of as three separate push-pull driver stages which create each phase waveform independently. The PWM pulses are applied to inverter switches. Various PWM techniques were developed for optimized performance of converter in applications like power system and renewable energy sources [1-3]. Sinusoidal PWM reduces the harmonics and increases the control on phase current; SVPWM technique increases the utilization of DC bus voltage and reduces the switching losses [3].

SVPWM technique can be implemented in DSP using look up table [1]; this method increases the execution time and overload the processor during closed loop operation. An alternate method includes the calculation of three sub intervals of the time period [4]. This method generates the time period varying with voltage magnitude. This will result in negative time period for higher range of voltages. The problem of the negative time period is addressed [5] by setting negative time period to zero. Other two sub intervals of the time period are calculated such that the algebraic sum of the two time values will be equal to the total time period, but this method looses the symmetry of switching waveform, which results distortion in output voltage.

In few cases [2-4] the problem of processor overloading is avoided by setting duty cycle value in the compare registers of DSP. However in this method as the time periods are generated depending on the voltage magnitudes, negative time periods are generated for certain range of voltages.

This paper presents simplified method for the implementation of the SVPWM algorithm using Texas Instrument Digital Signal processor (TMS320F2812). Methodology used in the algorithm is to generate switching pulses independent of magnitude of voltages and without using the lookup table. TMS320F2812 DSP processor has components like compare units and event manager, which is suitable for implementation of SVPWM algorithms [6]. The proposed methodology of inverter control extends the operating voltage and frequency to a wide range.

II. SPACE VECTOR PWM METHOD

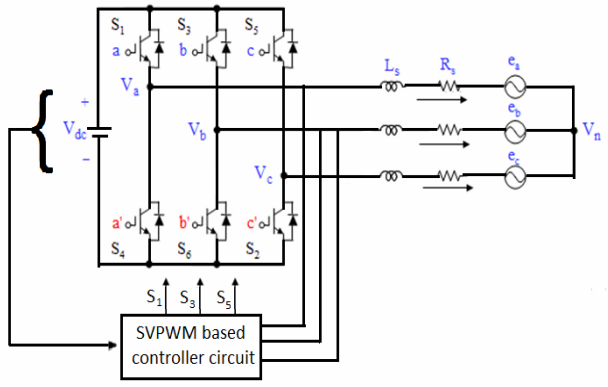

Fig.1: Structure of typical 3-phase VSI

Space vector PWM refers to a switching scheme of the six power switches of a 3-phase VSI. It generates minimum harmonic distortion and also provides more efficient use of DC supply voltage in comparison with

the sinusoidal modulation method. The topology of conventional two level voltage source inverter is shown in Fig.1.

Modeling of two level voltage source inverter in terms of switching function is given by (1).

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & 2 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} S_1 \\ S_3 \\ S_5 \end{bmatrix} \quad (1)$$

The space phasor can be defined by using two voltages V_α and V_β and is given by

$$V_\alpha = \frac{3}{2} \times V_{an} \quad (2)$$

$$V_\beta = \frac{\sqrt{3}}{2} \times [V_{bn} - V_{cn}] \quad (3)$$

The reference voltage is given by,

$$V_s = V_\alpha + j \times V_\beta \quad (4)$$

$$\alpha = \tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \quad (5)$$

It should be noted that at any instant of time there are only eight possible positions of the voltage space phasor as shown in fig.2

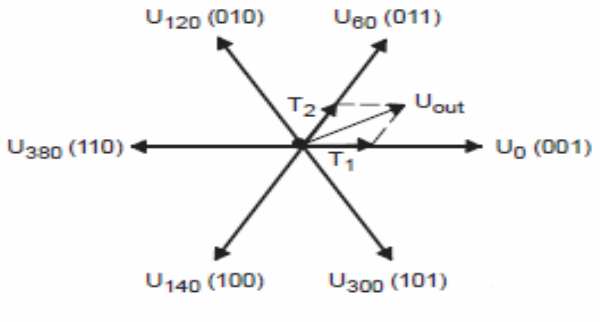

Fig.2: Voltage space vectors

SVPWM treats the inverter as a single unit. Specifically the inverter can be driven to eight unique states. Modulation is accomplished by switching the state of inverter.

Space vector pulse width modulation treats the sinusoidal voltage as a constant amplitude vector rotating at constant frequency. This PWM technique approximates the reference voltage V_{ref} by a combination of the eight switching patterns (V_0 to V_7). The vectors (V_1 to V_6) divide the plane into six sectors, V_{ref} is generated by two adjacent non-zero vectors and two zero vectors. Method includes determination of the V_{ref}, phasor angle α associated with the space phasor and the time durations T_1, T_2, T_0.

III. PWM USING TMS320F2812

TMS320F2812 consists of two event manager modules (A & B), inbuilt Analog to Digital converter and consists of 12 PWM output pins, 6 pins for each Event Manager Module. The ADC module include 12 bit core with built in dual sample and hold circuits with fast conversion at 25 MHz. Module takes the input between 0 to 3V. The start of conversion process can be triggered through the event manager. It has module has 16 channels, configurable as two independent 8 channel modules to serve event manager modules. Two independent modules can be cascaded to form a 16 channel module. The two 8-cnannel modules have capability to auto sequence a series of conversions. Each module has the choice of selecting any one of the respective eight channels available through an analog MUX. In cascaded mode auto sequencer functions as a single 16-channel sequencer. Once conversion is complete the selected channel value is stored in its respective ADCRESULT register. Auto sequencing allows the system to convert the same channel multiple times, allowing the user to perform oversampling algorithms.

PWM waveform generations with compare units and associated circuits require configuration of the Event Manager registers [7], [8]. The setup process for PWM generation includes the following steps

- Setup and load ACTRx
- Initialize CMPRx
- Setup and load COMCONx
- Setup and load T1CON (for EVA) or T3CON (for EVB) to start the operation
- Rewrite CMPRx with newly determined values

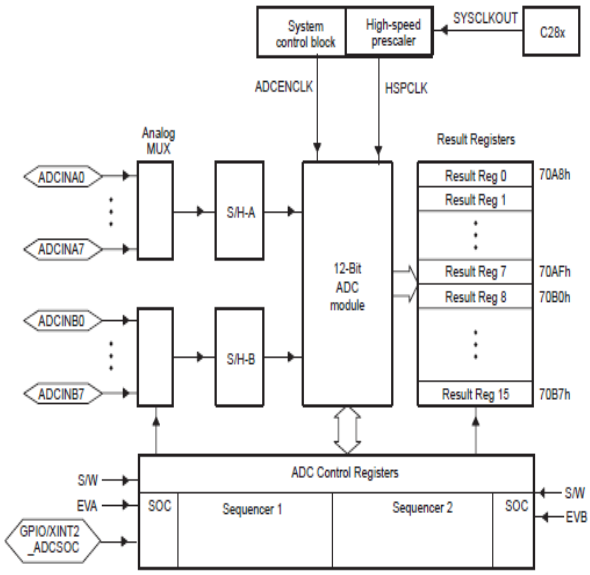

Fig.3: Block diagram of ADC Module

IV. IMPLEMENTATION OF SVPWM ALGORITHM

Three phase voltages are connected as input to the 3 ADC pins. The digital values of the three voltages are stored in the corresponding ADCRESULT registers. Phase voltages i.e. V_{an}, V_{bn}, V_{cn} are converted to two phase rotating reference frame as V_α and V_β using (1) & (2) and angle α is calculated using the (4). Sector number is determined in which reference vector located, by calculating the variables P_0, P_1, P_2 is given by following equations

$$P_0 = V_\beta \quad (6)$$

$$P_1 = \sin 60 \times V_\alpha - \sin 30 \times V_\beta \quad (7)$$

$$P_2 = -\sin 60 \times V_\alpha - \sin 30 \times V_\beta \quad (8)$$

Variable B is defined computed using the variables P_0, P_1, and P_2 for identification of sectors. Fig 4 gives flow chart for identification of sector and Table1 represents values of B corresponding to sector number [6].

Table.1: Identification of sector number

B	1	2	3	4	5	6
SECTOR	2	6	1	4	3	5

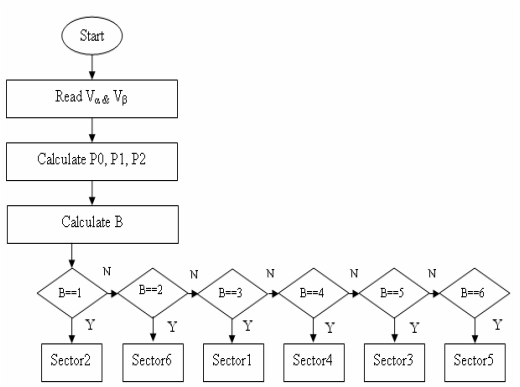

Fig.4: Flow chart for identification of sectors

$$B = 4\,sign(P2) + 2\,sign(P1) + sign(P0) \quad (9)$$

Where Sign (p) is a function given by,
Sign (p) =0, if p<0;
Sign (p) =1, if p>0;

The switching pattern can be obtained by calculating three sub intervals (T_1, T_2, T_0) from the sampling period T_s [2].

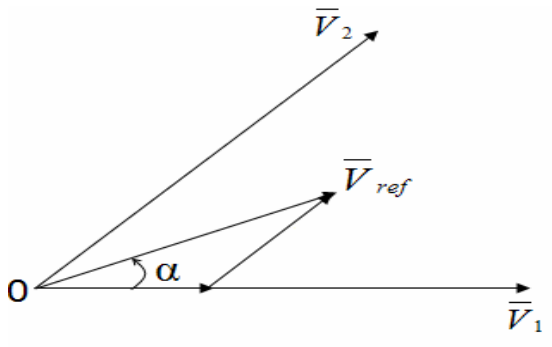

Fig.5: Combination of voltage space phasors

Fig.5 shows the combination of voltage space phasors. Reference voltage is placed in the first sector, between V_1 and V_2. The space phasor voltage is obtained by switching the vectors V_1 and V_2 for T_1 and T_2 seconds respectively. V_0 and V_8 vectors are switched for $T_0/2$ seconds. Three sub intervals of time period are calculated by,

$$T_1 = T_s \times a \times \sin(60 - \alpha) / \sin 60 \quad (10)$$

$$T_2 = T_s \times a \times \sin \alpha / \sin 60 \quad (11)$$

$$T_0 = T_s - T_1 - T_2 \quad (12)$$

The equations (10), (11), (12) presented above do not include any term relates the magnitude of the voltage. Hence time periods are totally independent of the voltage magnitude. The variation in the voltage magnitude will be considered through the modulation index "a", which will be in the range of 0.3 to 0.9. Three duty cycles T_a, T_b, T_c are set in the compare registers to generate SVPWM pulses are calculated using the equations.

$$T_a = \frac{T_0}{4} \quad (13)$$

$$T_b = T_a + \frac{T_1}{2} \quad (14)$$

$$T_c = T_b + \frac{T_2}{2} \quad (15)$$

Once the sector is determined, duty cycle for each pulse is assigned to compare registers CMPR1, CMPR2 and CMPR3. Comparing the general purpose timer with the CMPR registers, corresponding PWM signals will be generated at 6 PWM pins of event manager. The general purpose timer will be set to the continuous up and down mode. Table.2 gives the content of compare registers for different sectors.

Table.2: Identification of sector number

Register	Sector 1	Sector 2	Sector 3	Sector 4	Sector 5	Sector 6
CMPR1	T_a	T_b	T_c	T_c	T_b	T_a
CMPR2	T_b	T_a	T_a	T_b	T_c	T_c
CMPR3	T_c	T_c	T_b	T_a	T_a	T_b

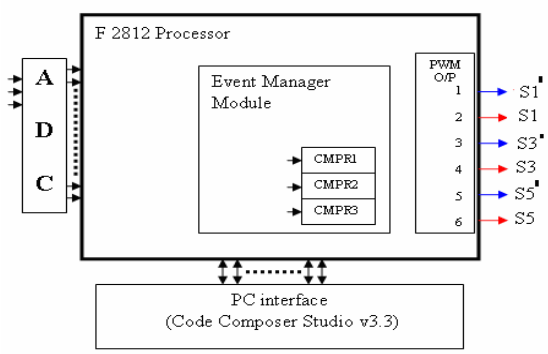

Fig.6: Block diagram of experimental setup.

The conventional approaches generate the negative values of T1, T_2, and T_0. Therefore the duty cycle values obtained will also be negative, which will cause distortion in waveforms at PWM outputs pins.
Fig.4 shows the general block diagram of experimental setup. Two event manager modules are available in the TMS320F2812 viz. A and B. Both modules are having 6 PWM output pins. Module-A has pin numbers 9 to 14 and B module has pin numbers 30 to 35.

For experimental purpose module A is used for generation of switching pulse S_1, S_3 and S_5 at pins 10, 12 and 14 respectively. Other three pins will have inverted output of previous pins and hence pulses for S_2, S_4, and S_6 can be obtained. Fig.5 shows flow chart for implementation of SVPWM using TMS320F2812. Three phase voltages are read from ADC output pins and space phasor voltage is obtained by using (2), (3), (4). The

sector number and duty cycle values are determined. Duty cycle values are loaded in to the corresponding compare registers. General purpose timer will be continuously compared with the compare registers to produce PWM pulses.

Fig.6 shows experimental setup. The DSP module will be connected to computer through 25 pin parallel port. Code composer studio 3.1v is used for interaction between the DSP and the computer. As the code is executed in CCStudio PWM pulses will be generated at the PWM output pins. These pulses can be observed in scope.

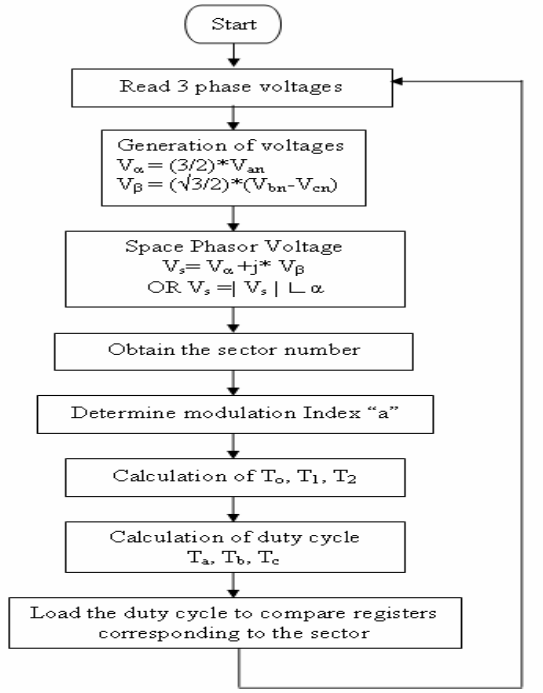

Fig7: Flow chart for SVPWM Implementation

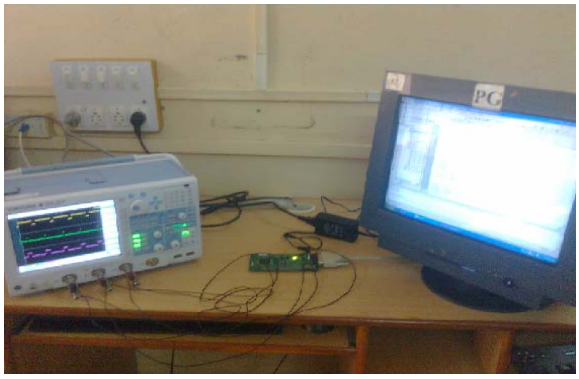

Fig 8: Experimental set up

V. RESULTS AND DISCUSSIONS

The space vector PWM waveforms generated are symmetric with respect to the middle of each PWM period. Symmetric waveform generation will eliminate even harmonics and reduces the odd harmonics. Symmetric space vector PWM generation is shown in Fig.9.

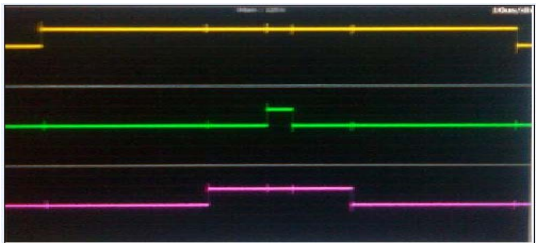

Fig.9: Symmetric wave form generation

Fig.10 shows the generation of symmetric switching waveform for all six sectors using TMS320F2812. Waveform is generated using PWM channels of DSP having the following characteristics.

- Each PWM channel switches twice per every PWM period except when the duty cycle is 0% or 100%.
- There is a fixed switching order among the three PWM channels for each sector.
- Every PWM period starts and ends with 000.
- The amount of 000 inserted is the same as that of 111 in each PWM period.

Waveforms are generated for different values of three phase voltages and for different frequencies.

Fig. 10a: First sector

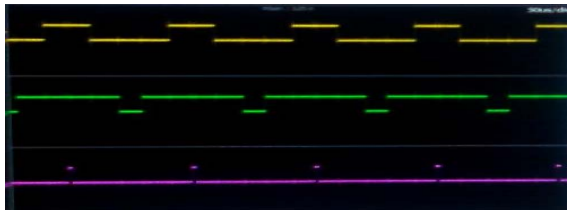

Fig. 10b Second sector

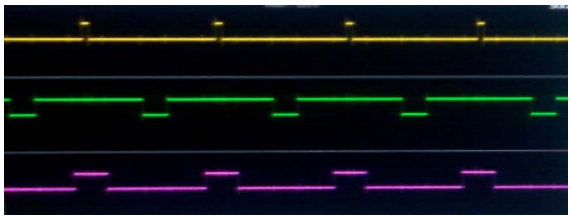

Fig 10c: Third sector

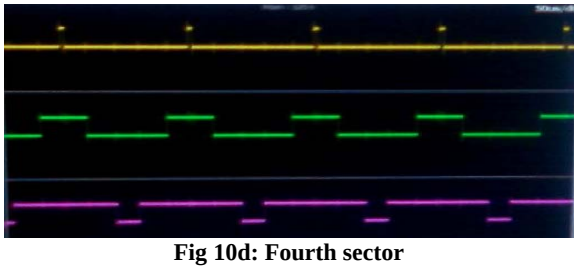

Fig 10d: Fourth sector

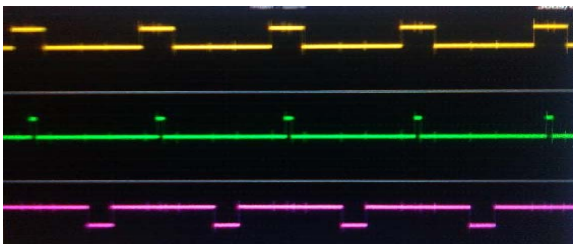

Fig 10e: Fifth sector

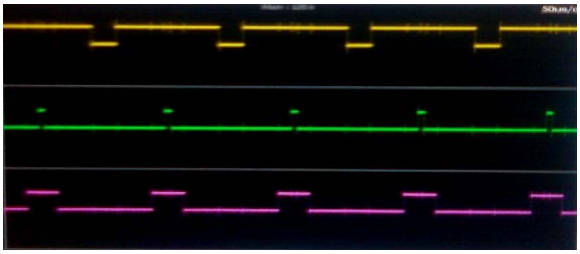

Fig 10f: Sixth sector

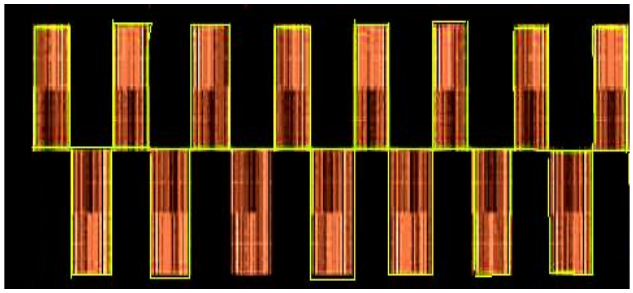

Fig 11: Output voltage of 2-level inverter

Line voltage waveform is shown in fig.10. Waveforms are generated for different values of three phase voltages and for different frequencies. The generated PWM signals are given to inverter and output waveforms are obtained. Fig.9 shows the output waveforms of inverter and fig.10 shows line current.

Fig 12: Line current waveforms

VI. CONCLUSION

The detailed implementation of SVPWM algorithm for the inverter switching control scheme using DSP board TMS320F2812 is presented in this paper. The operating principle of the DSP board and the generation of the SVPWM pulses are discussed. The symmetric PWM waveforms are obtained for individual sectors. The proposed algorithm is verified for wide range of voltage magnitude, frequencies and modulation index from 0.3-0.9. Adoption of the present method for the inverter control system will increase the range of operating voltage and frequency. As the response time of the DSP is very fast, it is an excellent choice for real time applications in the power system. The result obtained from the experiments conducted in laboratory clearly shows successful implementation of the SVPWM using DSP.

ACKNOWLEDGEMENT

The authors thank AICTE- New Delhi for the RPS grant. Authors also thank Techno-Com, Bangalore, India for supplying the TMS320F2812 DSP kit and accessories.

REFERENCES

[1]. Zhiyong Du, Xianfing Wang, "SVPWM Speed Governing System of Induction Motor Based on DSP"EUROCON 2007 The International Conference on "Computer as a Tool" Warsaw, September 9-12.

[2]. Ying-Shieh Kung, Pin-Ging Huang, "High Performance Position Controller for PMSM Drives Based on TMS320F28 12 DSP", Proceedings of the 2004 IEEE International Conference on Control Applications Taipei, Taiwan, September 2-4,2004eZdspTM F2812 Technical Reference, (506265-0001), SPECTRUM DIGITAL, INC.

[3]. Zhenya Yu, Arefeen Mohammed, Issa Panahi,"Review of Three PWM techniques",Texas Instruments, DSP Automotive/Industrial Applications, Houston, TX 77477.

[4]. Agileswari Ramasamy, Vigna Kumaran Ramachandaramurthy, Rengan Krishna Iyer, Liew Zhan Liu, "Control of Dynamic Voltage Restorer using TMS320F2812", 9th international conference, Electric power quality and utilization, Barcelona, October 2007

[5]. Xing Xu, Doug Deng, "Three phase inverter circuit with improved transition from SVPWM to six step operation" United States Patent, patent No 5,552,977. Date of patent Sep 3,1996

[6]. Zhenyu Yu, "Space-Vector PWM With TMS320C24x/F24x Using Hardware and Software Determined Switching Patterns", Digital Signal Processing Solutions, Application Report, (SPRA524).

[7]. TMS320C281x Analog to Digital Converter Reference Guide (SPRU060), Texas Instrument

[8]. TMS320C281x Event Manager Reference Guide (SPRU065), Texas Instrument.

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