



Digital controller for an isolated Step-Up DC-DC converter based on three-phase high-frequency transformer for grid-connected PV applications

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Abstract. This paper presents the control system design of a DC-DC converter with a three-phase high frequency transformer for dual-stage grid-connected PV applications. This converter is designed to be used in the input stage of parallel single-string PV arrangements for residential applications. The proposed control strategy uses a maximum power point tracking algorithm with an outer voltage loop and an inner current loop. The current loop includes a resonant control action in order to eliminate the 120Hz ripple of the DC bus in the PV modules. Simulation results are presented to validate the proposed control strategy.

Key words

Photovoltaic systems, DC-DC converter, digital control, resonant controller.

1. Introduction

Photovoltaic energy became one of the major focus of investments in renewable energies. The use of photovoltaic (PV) modules has several advantages such as not emitting CO₂, requiring short maintenance, having simple installation, among others [1], [2]. Among the existing PV applications, the most significant is the grid-connected photovoltaic systems (GCPS). These configurations have contributed with about 99% of new PV systems installed worldwide in 2009 [1]. GCPS are installed to supply the energy directly to end users and sells the exceed of energy for the electric power distributor.

GCPS using central inverters (CI) schemes have some advantageous characteristics such as: low cost of the converter, reduced system complexity, reliability, easy installation and maintenance. Central inverters can be classified by the number of power processing stages: single-stage and dual-stage. Dual-stage single-string is the most usual configuration, where a DC-DC converter is responsible for the MPPT and a DC-AC inverter controls the grid current. In this configuration is required a bulky DC bus capacitor to filter the voltage ripple with double of

AC grid frequency. The reduction of DC bus capacitance is desirable due to high cost and low mean time between failures (MTBF). However, a lower DC bus capacitance may result in a higher current ripple in the PV array. This current ripple is undesirable because interfere in the operation of the algorithm of maximum power point tracking (MPPT) and reduces the energy production of the PV modules.

Several PV arrangements and power conversion systems have been developed [3], [4]. The single-string configuration using parallel arrangements of PV arrays is attractive for residential applications, due to its high Fill Factor (FF) when occur partial shading of PV [5]. Additionally, PV arrangements with few modules in series operate with low voltage in the PV terminals, which reduces the risk of electric shock during installation and maintenance [7], [8].

This paper proposes a digital controller for the input stage of a GCPS employing a three-phase DC-DC converter isolated in high frequency (TDIHF) [9]. This topology is suitable for parallel PV arrays with a few PV modules in series, because the transformer allows the implementation of high voltage gain (up to 10 times) in a single stage. Galvanic isolation avoids the problems associated with leakage currents, which make easy the grounding of PVs and reduce the risks of electric shock. Moreover, the three-phase structure reduces the input current ripple which allows the reduction of input capacitors.

The purpose of the control system is to make possible the reduction of DC bus capacitance without impact on the energy production of the PV array. To achieve this objective is proposed two control loops, an outer voltage loop with a PI controller to track the reference provided by the MPPT algorithm and an inner current loop with a resonant controller action to eliminate the inverter ripple that would appears in the input of the DC-DC converter.

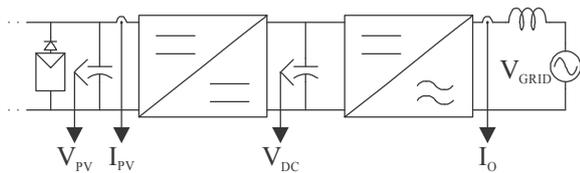


Fig. 1. Block diagram of the proposed PV system.

The contributions to the proposed control system are: i) the use of a resonant controller for rejection of the current ripple in the PV modules; ii) the generation of a voltage reference from the MPPT algorithm; iii) a fast current control law calculated with a delay of one third of switching period; and iv) the inclusion of an anti-windup to improve the transient performance. Some analyses illustrate the system behavior for variation in the AC grid frequency and a parametric variation of the plant. Finally, simulation results are presented to demonstrate the operation of the proposed digital control laws GCPS in different irradiation and temperature conditions of the PV array.

2. Proposed System

A. Topology

The proposed system is shown in Fig. 1. The system consists of a set of photovoltaic (PV) modules, a step-up DC-DC converter, a DC bus and a single phase inverter. The total peak power of PV array is 5850W, which is the sized for consumption of a typical residence [10]. The modules are arranged in an array of 15 strings of 3 PV modules connected in series.

The DC-DC converter is designed to track the maximum power point of the PV array, to increase the voltage from the PV array for the needs of the inverter, to provide galvanic isolation, and to decouple the input current from DC bus voltage ripple. The chosen topology is shown in Fig. 2, whose operation details are described in [9]. One can observe the use of an input capacitor C_{in} to cut off the high frequency ripple in PV modules.

The DC bus is used to store the energy processed by the input stage. This voltage must be greater than the grid voltage, given that the inverter operates in step-down mode. The output stage consists of a single phase inverter with a full-bridge topology and an inductive filter. This inverter is controlled to inject the energy produced by the PV array on the AC grid.

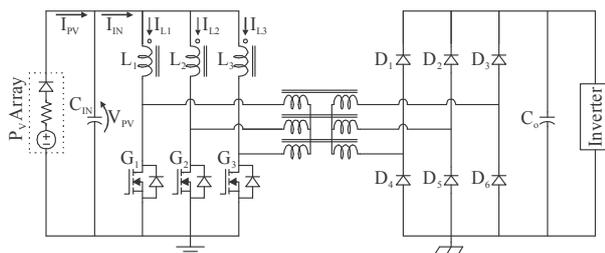


Fig. 2. Three-phase step-up DC-DC converter isolated in high frequency.

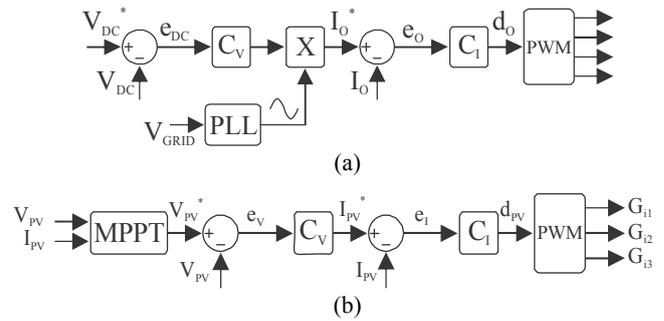


Fig. 3. Control structure. (a) Output stage. (b) Input stage.

B. Control Structure

Fig. 3 shows the control structure of the proposed system. The control system consists of two independent structures: one to control the input stage and another to control the output stage.

Fig. 3 (a) presents the control scheme of the output stage (inverter). The output structure that acts on the inverter has the objective of: i) inject the power generated by the photovoltaic system into the AC grid with unity power factor; ii) regulate the DC bus average voltage. This control scheme is based in two cascaded control loops: an outer loop controls the voltage level of the DC bus while an inner current loop guarantees the tracking of the sinusoidal reference.

Fig. 3 (b) shows the control scheme of input stage, whose actuation is on the DC-DC converter. This structure has the following objectives: i) track the maximum power point (MPP) of the PV modules; ii) reject possible ripple in the input current of the DC-DC converter due to the voltage ripple of the DC bus. The control structure of the input stage uses two cascaded control loops. An algorithm of maximum power point tracking (MPPT) is used to generate a voltage reference of the PV array [11]. The voltage loop generates the input current reference of the DC-DC converter, which is regulated by an inner current loop. This loop has fast dynamic and is designed to eliminate current ripple in the PV modules.

The proposed control of the input stage employs a proportional-integral (PI) controller in the voltage loop. This controller guarantees that the reference voltage generated by the MPPT algorithm is tracked with zero steady state error. The proposed inner current loop uses a resonant controller with a phase-lead compensation. The resonant controller is used to obtain a high gain at 120Hz, which allows the rejection of steady-state current ripple at input of the DC-DC converter due to voltage ripple on DC bus.

The proposed controller uses a MPPT algorithm that generates a voltage reference instead of a current reference. Although unusual, recent studies show that the use of the voltage loop results in better performance of the system [7]. Analyzing the maximum power point in typical V-I curves, one can observe that voltage variations depends on the temperature of the PV modules, while the current variation are related to

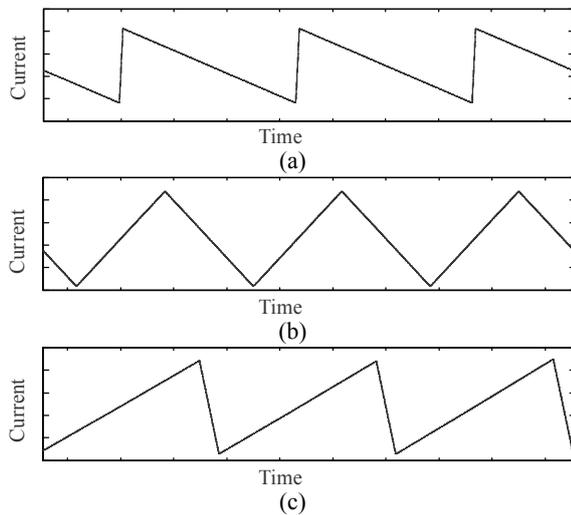


Fig. 4. Input current in the TDIHF converter in R_2 region. (a) $d = 0.33$ (b) $d = 0.50$ (c) $d = 0.66$

changes on irradiation over the modules. As temperature changes much slower than irradiation, the dynamic of the algorithm have lower impact in MPPT performance.

3. Input Stage Control

A. Sampling and updating of the control signals

Fig. 4 shows the waveforms of the input current I_{PV} of the converter given in Fig. 3, at the operating region R_2 , for the following duty cycles: $d = 0.33$ (minimal), $d = 0.50$, and $d = 0.66$ (maximum). Analyzing these waveforms, one can conclude that it is not possible to obtain the average current synchronizing the modulation with the instants of sampling of input current. Moreover, we observe that any instant free of switching for $0.33 < d < 0.66$. Therefore, the current must be filtered before sampling for reduction of switching noise. So it is required an anti-aliasing filter to obtain the average value of the input current.

Fig. 5 shows the three triangular carriers used for generation of PWM signals for switches G_1 , G_2 and G_3 . These waveforms have the same frequency but are phase-shifted 120° . Both sampling and updating frequencies are the same, but the sampling instant is phase-shifted in 120° . This delay is required for implementation on a digital signal processor.

B. Dynamic models

In order to design the current loop is derived the dynamic model of the TDIHF which relates the duty-cycle and the input current of this converter. Considering the operation

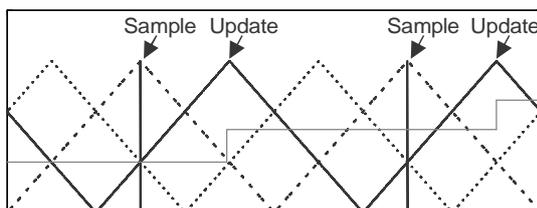


Fig. 5. Modulation signals and sampling/updating instants.

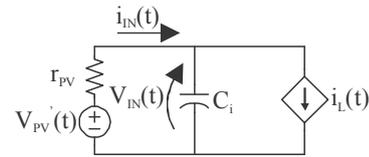


Fig. 6. Equivalent electric circuit of the converter.

exclusively at operation region R_2 , one can obtain the simplified model as follows [9]:

$$\frac{i_L(s)}{d(s)} = \frac{3.V_o}{s.n.L} \quad (1)$$

On the other hand, to design the control loop is derived a model which relates the input voltage and input current of the TDIHF. This model is obtained from the equivalent electrical circuit shown in Fig. 6, where is assumed that current loop have a bandwidth much wider than voltage loop. As a result, both can be considered dynamically decoupled, which result in the following model:

$$\frac{V_{IN}(s)}{i_L(s)} = -\frac{1/C_i}{s+1/(C_i.r_{PV})} \quad (2)$$

C. Controller design

The converter specifications are presented in Table I. From these specifications were obtained the parameters of the converter which are given in Table II. This table also presents some parameters related to the implementation of the control law in DSC MC56F8257 of Freescale.

1) Current Controller

Fig. 7 shows the block diagram of the current loop. This control law is designed to have a gain crossing frequency of 1.5 kHz and phase margin greater than 55° . In order to simplify the design were considered unitary gains for

Table I - DC-DC converter specifications.

Input power (P_{IN})	5852W
Output voltage (V_O)	360V
Input voltage (V_{IN})	34,14 V ~ 58,49 V
Output voltage variation (ΔV_O)	40 V
Input current variation (ΔI_{IN})	2 A
Switching frequency (f_s)	20 kHz
Grid frequency (f_i)	60 Hz

Table II - Converter and control parameters.

Transformer ratio - n	4
Inductor L_1, L_2, L_3	187.5 μ H
Input capacitor - C_{IN}	10 μ F
Output capacitor - C_O	1000 μ F
Sample frequency - f_A	20 kHz
Current sensor - H_i	0.1
Input voltage sensor - H_v	0.1667
AD gain - K_{AD}	1241.21
PWM gain - K_{PWM}	1/1500
Sensor signal attenuation - K_{AG}	0.22

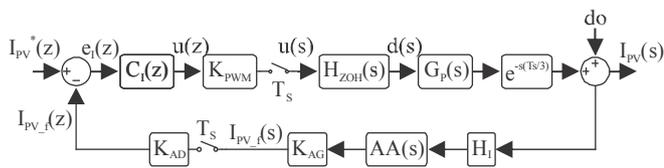


Fig. 7. Block diagram of the current loop.

ADC, PWM and sensor.

In this project was designed a second order anti-aliasing filter with a cutoff frequency equal to a half the switching frequency and with a damping factor of 0.7:

$$H_{AA}(s) = \frac{3.948 \cdot 10^9}{s^2 + 8.796 \cdot 10^4 s + 3.948 \cdot 10^9} \quad (3)$$

The plant model presented in (1) had been discretized assuming the implementation delay of 1/3 of cycle. This model can be obtained from the modified z transform technique [12]. So the discrete-time model of the plant shown in (1) with the anti-aliasing filter expressed in (3) is given by:

$$G_p(z) = \frac{16.26z^3 + 56.84z^2 + 9.586z + 0.07685}{z^4 - 0.8617z^3 - 0.126z^2 - 0.0123z} \quad (4)$$

The controller was designed using *w*-plane technique [12], since the bandwidth of current loop is lower than ten times the switching frequency. The dynamic model shown in (4) is given in the *w*-plane by:

$$G_p(w) = \frac{17.78w^4 - 3.12 \cdot 10^5 w^3 - 1.04 \cdot 10^{11} w^2 + 4.77 \cdot 10^{14} w + 1.21 \cdot 10^{20}}{w^4 + 1.30 \cdot 10^5 w^3 + 5.72 \cdot 10^9 w^2 + 8.42 \cdot 10^{13} w} \quad (5)$$

From this model was designed the current controller. In order to eliminate harmonics components with twice the mains frequency was designed a phase-lead-resonant compensator:

$$G_I(z) = G_R(z) + G_{LEAD}(z) \quad (6)$$

The resonant compensator was tuned to eliminate harmonics at 120Hz and the phase-lead compensator to increase the phase margin of the system. The resulting compensators are given by:

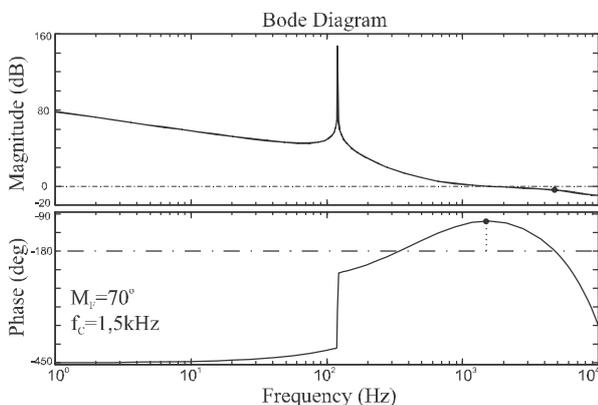


Fig. 8. Bode diagram of the current loop.

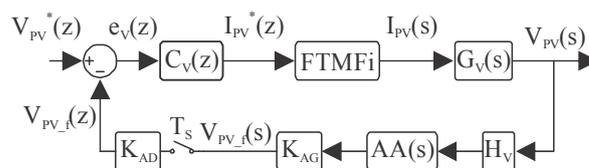


Fig. 9. Block diagram of the voltage loop.

$$C_R(z) = \frac{0.04946432z - 0.047227616}{z^2 - 1.998579189z + 1} \quad (7)$$

$$C_{LEAD}(z) = \frac{0.6913051z - 0.4293188}{z - 0.133947515}$$

Fig. 8 presents the Bode diagram of the current loop. One can observe that both gain crossing frequency and phase margin meet the specifications.

2) Voltage Controller

Fig. 9 shows the block diagram of the voltage loop. This control law is designed to have a gain crossing frequency two decades lower than current loop and a phase margin greater than 55°. As well as in current loop, for design purposes was considered a unitary gain for ADC, PWM and sensor.

The crossover frequency was chosen to avoid dynamic interaction with the current loop. As a result, the current loop can be simplified as a gain without lost of generality. Due this, the current loop is represented by the block FTMFi in Fig. 9. Moreover, one can observe that implementation delay is not represented in Fig. 9. This delay was neglected because does not affect significantly the frequency response at low frequencies.

The plant that relates the input current with the input voltage shown in (2) is discretized using bilinear method:

$$G_v(z) = -\frac{0.1638(z+1)}{z-0.3104} \quad (8)$$

whose model in *w*-plane is given by:

$$G_v(w) = \frac{-10000}{w + 21050.06} \quad (9)$$

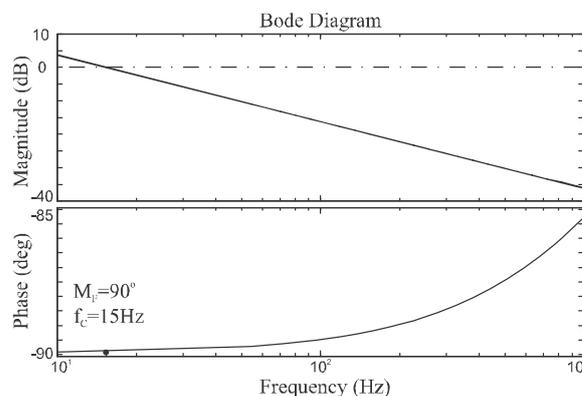


Fig. 10. Bode diagram of the voltage loop.

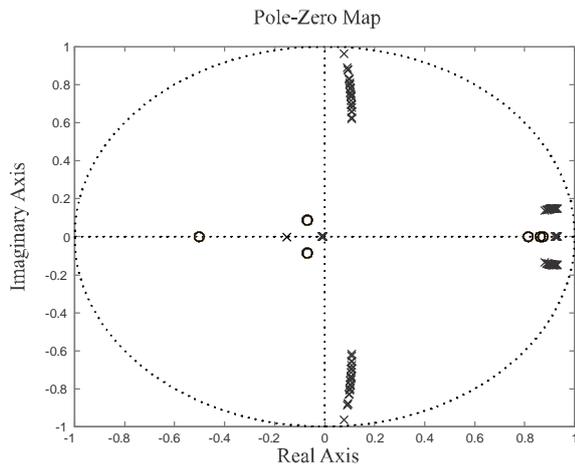


Fig. 11. Closed loop poles in the current loop according to parametric variations of L , V_o e n .

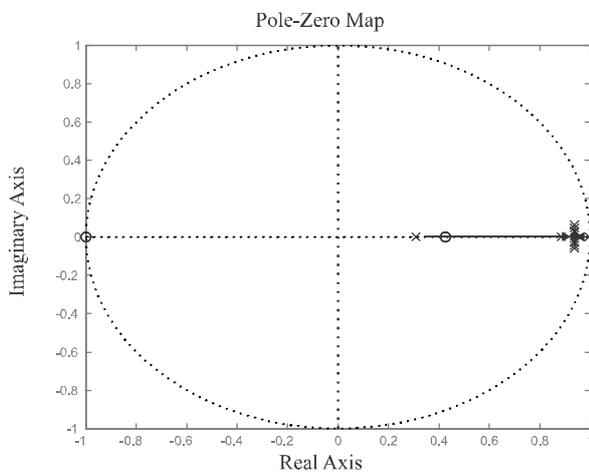


Fig. 12. Closed loop poles in the loop voltage for variations in r_{pv} .

From this model was designed the voltage controller. In order to achieve zero steady-state error was designed the following PI compensator:

$$C_{PI}(z) = \frac{-0.06080128}{z-1} - 0.10593018 \quad (10)$$

Fig. 10 shows the Bode diagram of the voltage loop. One can observe that both gain crossing frequency and phase margin meet the design specifications.

4. Control System Analysis

First is analyzed the robustness of current loop under parametric variation of the plant. It has been considered deviation from nominal value of $\pm 15\%$ on inductances L_1 , L_2 and L_3 , output voltage V_o and transformer ratio n . Fig. 11 shows the closed loop poles of the system for all possible excessive variations. One can observe that the control system is always stable.

Next is analyzed the robustness of the voltage loop under variations of equivalent resistance of PV array. The values of equivalent resistance among the operating limits of irradiation and temperature of the PV modules at MPPT were considered ($0,3939\Omega < r_{pv} < 4,6827\Omega$). Fig. 12 shows

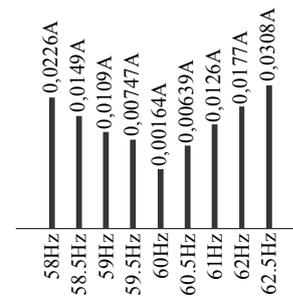


Fig. 13. Magnitude of the input current ripple under grid frequency variations.

the closed loop poles of system for the variations of r_{pv} in this range, where one can observe that control system is always stable.

At last it is analyzed the impact of the grid frequency variation in the input current ripple. Fig. 13 shows the magnitude of harmonics of the input current for a ripple of ± 20 V in DC bus. One can observe that input current controller reject significantly disturbances in the input frequency for grid frequency variations of ± 2 Hz.

5. Simulation and Experimental Results

Simulations and experimental results are presented to illustrate the system performance in steady-state. The steady-state analysis of TDIHF converter is performed for 12 PV modules with an irradiation and temperature around 600W/m^2 and 60°C to be equal to the environmental conditions of the experimental results. Fig. 14(a) shows the PV current of the converter in this condition. The 120 Hz harmonic component has been eliminated although the waveform reveals an envelope with this frequency. The explanation for this waveform is the phenomena of “beat frequency” of harmonics frequencies. Fig. 14(b) shows the voltage across the terminals of the PV array.

Preliminary experimental results are presented in Fig. 15 and show the results of a simulation of 100ms. One can observe that in Fig. 15 (a), the results are very similar to

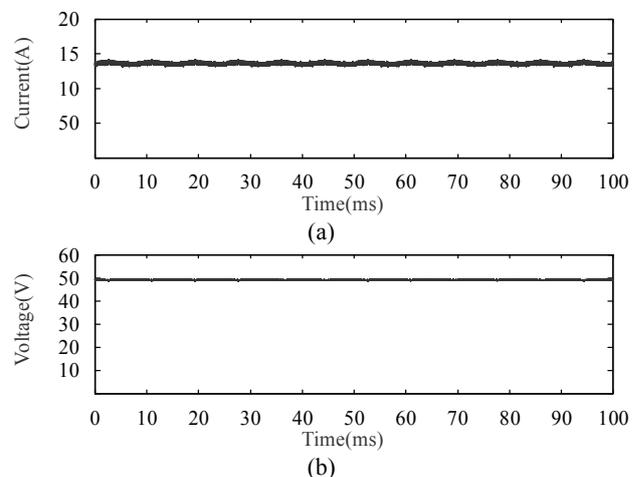


Fig. 14. Simulation in steady state. (a) PV current of the DC-DC converter. (b) Voltage over the PV array.

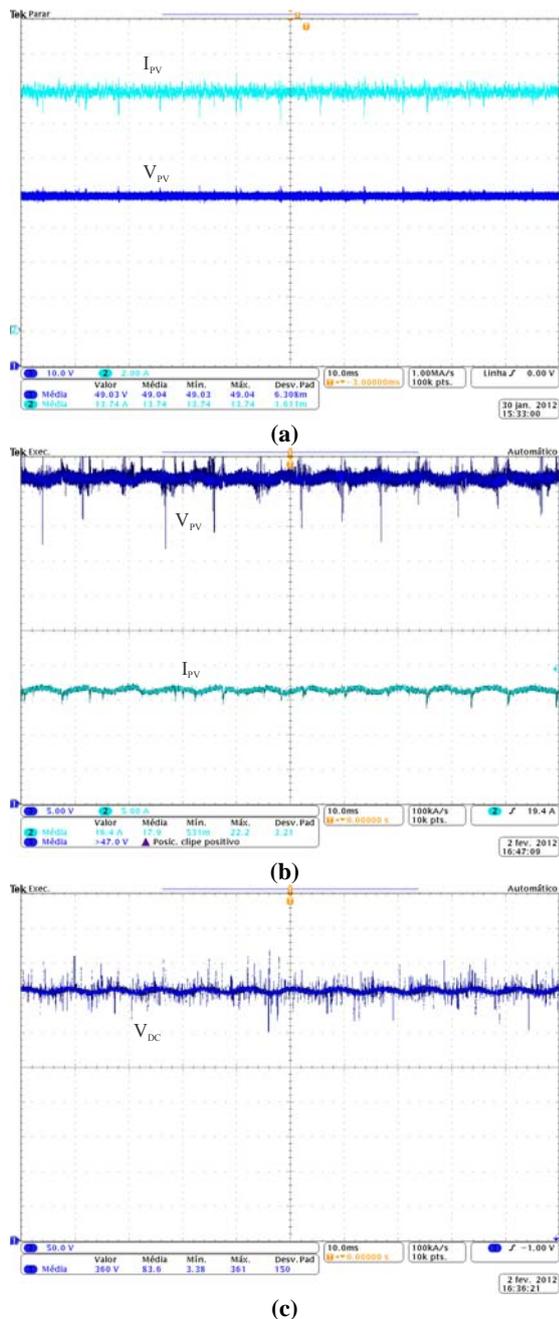


Fig. 15. Experimental results in steady state. (a) PV current and voltage of the DC-DC converter with resonant current control. (b) PV current and voltage of the DC-DC without resonant current control. (c) Output voltage of the DC-DC converter.

the simulation validating the proposed control strategy. Fig. 15 (b) shows the same experimental results but without using the resonant current control. Fig. 15 (c) presents the output voltage of the DC-DC converter to show the presence of a 120Hz ripple.

The prototype build was a DC-DC converter of 1500W and an inverter with an L filter connected to the grid to generate the 120Hz ripple in the DC bus. The PV array used has 12 PVs with the configuration of 3 modules in series and 4 modules connected in parallel.

6. Conclusion

This paper presented the design and implementation of a digital controller for a three-phase DC-DC converter isolated with a high frequency transformer for grid-connected PV application. The proposed control scheme uses two control loops based on a resonant controller in the inner current loop and a PI controller in the outer voltage loop. This control strategy makes possible the reduction of DC bus capacitance without negative impact on the energy generation of the PV array.

Simulation results are presented to validate the proposed control scheme. Steady-state results demonstrate the high rejection capability in PV array current of harmonics with twice the mains frequency.

Preliminary experimental results are presented to compare with the simulation and validate the control strategy.

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