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Performance Analysis of Multilevel Inverters Using Variable Switching Frequency Carrier Based PWM Techniques

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Abstract. In this paper, various pulse width modulation techniques are proposed, which can minimize total harmonic distortion and enhance the output voltages in five-level inverters. Multilevel inverters are important for power electronics applications, such as flexible AC transmission systems, renewable energy sources, uninterruptible power supplies and active power filters. Two methodologies adopting phase disposition and phase opposition disposition pulse width modulation concepts are proposed in this paper. These methodologies are divided into two techniques: sinusoidal pulse width modulation which minimizes total harmonic distortion and sinusoidal pulse width modulation with zero sequence signal which enhances the output voltage. FPGA has been chosen to implement the pulse width modulation due its fast prototyping, simple hardware and software design. The simulation and experimental results are presented.

Key words

Multilevel Inverters, Sinusoidal with zero sequence, harmonics, Variable switching frequency, Total harmonic distortion.

1. Introduction

Recently, multilevel inverters have become more attractive to researchers and industrial companies due to fast developing of high power devices, and related control techniques. Different multilevel inverter structures are cascaded H-bridge, diode clamped and flying capacitor [1]-[4]. Increasing the number of levels in the inverter without requiring higher ratings on individual devices can increase the power rating [5]. The advantages of multilevel inverters are an enhanced output voltage, reduced total harmonic distortion, and reduced voltage stress on semiconductor switches and a decrease in EMI problems [6]-[10].

In this paper, two carrier based pulse width modulation schemes, namely phase disposition and phase opposition disposition variable switching frequency multicarrier pulse width modulation, are presented. These techniques take advantage of special properties available in multilevel inverters to minimize total harmonic distortion and increase output voltage [11]-[14]. Illustrative examples are provided to demonstrate the feasibility of the proposed methods.

2. Three Phase Cascaded Multilevel Inverter

A three phase cascaded multilevel inverter is shown in Fig.1.

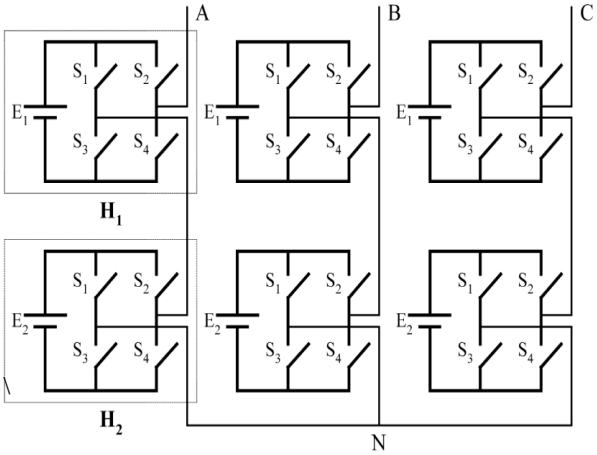

Fig. 1. Three phase cascaded five level inverter.

The circuit is designed for a five-level inverter consisting of 12 switches. Each DC source connected with its respective H-bridge, and generates three different output voltages, $+V_{dc}$, 0, and $-V_{dc}$, using various combinations of switching. The output of the multilevel inverter is synthesized by H-bridges connected in series. The number of output phase voltage levels in a cascaded inverter is given as m=2s+1, where s is the number of separate DC sources and m is the inverter level.

3. Variable Switching Frequency Multicarrier Pulse Width Modulation

In this chapter the analysis of variable switching frequency multicarrier PWM techniques are presented. Here variable frequency carrier signals are compared with reference voltage. In variable switching frequency PWM techniques PD, POD modulating techniques are proposed using sinusoidal and sinusoidal with zero sequence pulse width modulation methods.

3.1. Phase disposition Pulse width modulation

3.1.A. Sinusoidal Pulse Width Modulation

Fig. 2 shows the sinusoidal pulse width modulation of an m-level inverter, (m-1) carriers with the same frequency f_c and same amplitude A_c are positioned such that the bands they occupy are contiguous. The reference waveform has peak to peak amplitude of A_m and a frequency f_m. Its zero amplitude is centered in the middle of the carrier set. The reference is continuously compared to each of the carrier signals. If the amplitude of the reference is greater than the amplitude of the carrier signal, then the switch corresponding to that carrier is switched

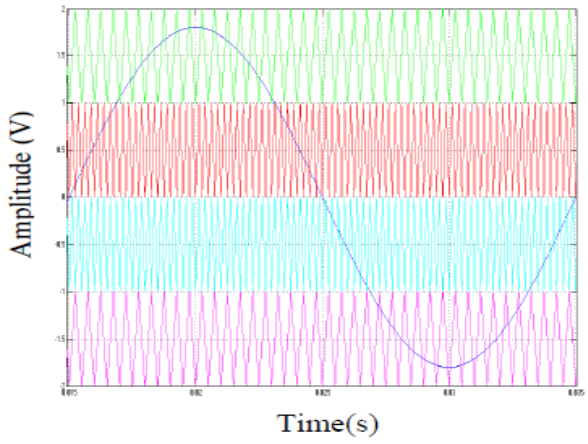

Fig.2. Phase disposition sinusoidal pulse width modulation.

In multilevel inverters, the amplitude modulation index Ma and the frequency ratio Mf are defined as:

$$M_a = \frac{A_m}{(m-1)A_c} \quad (1)$$

$$M_f = \frac{f_c}{f_m} \quad (2)$$

In this technique, as carriers are in phase across all the bands, significant harmonic energy is concentrated at the carrier frequency. Since, it is a co-phasal component, the line to line voltage does not appear. Here, the carrier waves having variable switching frequencies of 2000 Hz and 4000Hz are compared with the reference wave of 50Hz as shown Fig.3.

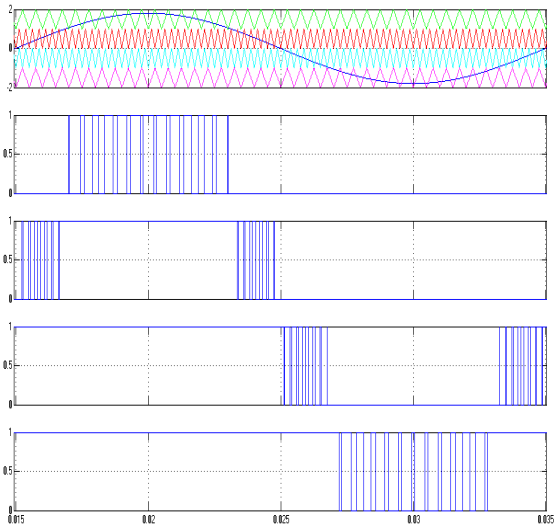

Fig.3.Phase disposition sinusoidal pulse width modulation generation.

3.1.B. Sinusoidal with Zero sequence Pulse Width Modulation

Fig. 4 shows the sinusoidal pulse width modulation with zero sequence in which a triplen harmonic voltage is added to each of the reference waveforms.
The method takes the instantaneous average of the maximum and minimum of the three reference voltages (V_a, V_b, V_c) and subtracts the value from each of the individual reference voltages to obtain the modulation waveforms:

$$V_{off} = \left\{ \frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2} \right\} \quad (3)$$

$$V_a SZS = V_a - V_{offset} \quad (4)$$

$$V_b SZS = V_b - V_{offset} \quad (5)$$

$$V_c SZS = V_c - V_{offset} \quad (6)$$

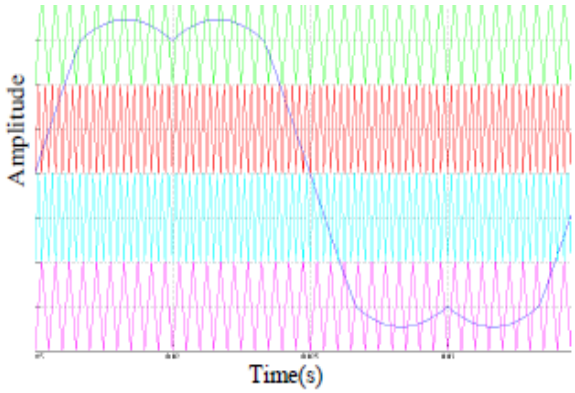

Fig.4.Phase disposition sinusoidal with zero sequence pulse width modulation.

Here, the reference wave is a sine wave with a zero sequence signal. The resulting flat topped waveform in this method allows overmodulation while maintaining excellent AC and DC spectra. This is an alternative method to improve the output voltage without entering the overmodulation range. So any carriers employed for this reference will enhance the output voltage by 15% without increasing the harmonics:

In this technique, carrier waves with variable switching frequencies of 2K Hz and 4KHz are compared with the reference wave of 50Hz as shown in Fig. 5.

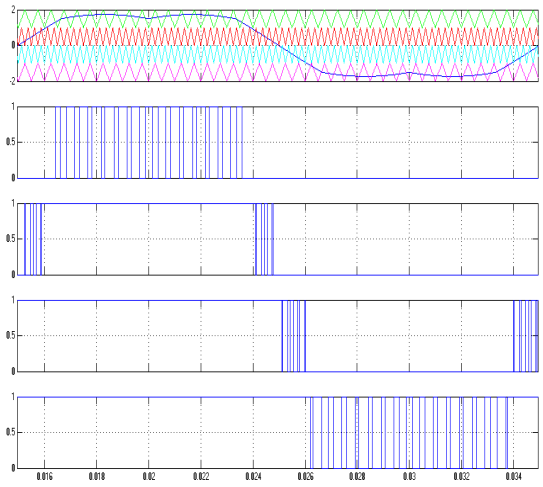

Fig.5. Phase disposition sinusoidal with zero sequence pulse width modulation generation.

3.2. Phase opposition disposition Pulse width modulation

3.2.A. Sinusoidal Pulse Width Modulation

For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 180º out of phase with those below zero. Fig.6 demonstrates the sine-triangle method for a five level inverter. Therein, the phase modulation signal is compared with four (N-1 in general) triangle waveforms.

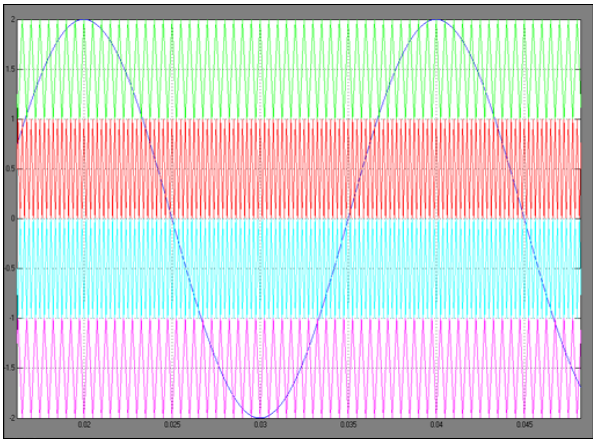

Fig.6. Phase opposition disposition sinusoidal pulse width modulation.

The rules for the phase opposition disposition method, when the number of level N = 5 are
(i) The N –1 = 4 carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 180º out of phase with those below zero.
(ii) The converter is switched to + V_{dc} / 2 when the reference is greater than both carrier waveforms.
(iii) The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.
(iv) The converter is switched to - V_{dc} / 2 when the reference is less than both carrier waveforms.

In this technique, carrier waves with variable switching frequencies of 2KHz and 4KHz are compared with the reference wave of 50Hz as shown in Fig. 7.

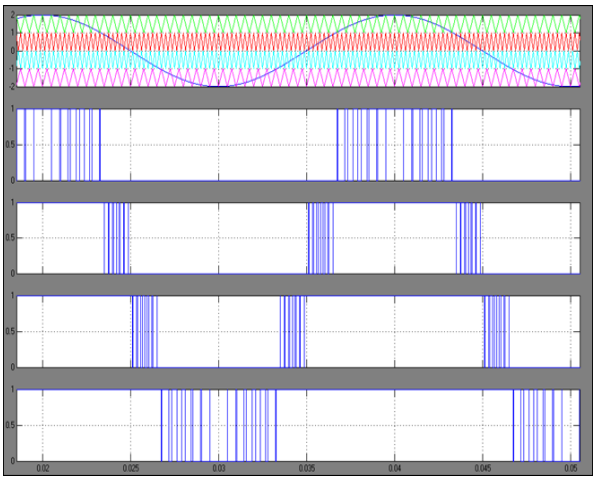

Fig.7.Phase opposition disposition sinusoidal pulse width modulation generation.

3.2.B. Sinusoidal with Zero Sequence Pulse Width Modulation

Fig. 8 shows the sinusoidal pulse width modulation with zero sequence in which a triplen harmonic voltage is added to each of the reference waveforms.

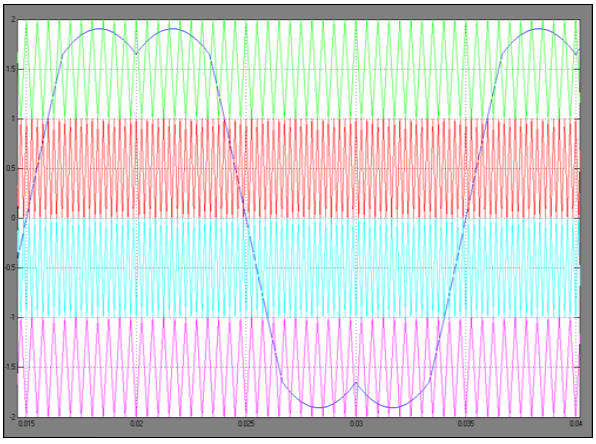

Fig.8. Phase opposition disposition sinusoidal with zero sequence pulse width modulation.

In this technique, carrier waves with variable switching frequencies of 2KHz and 4KHz are compared with the reference wave of 50Hz as shown in Fig. 9.

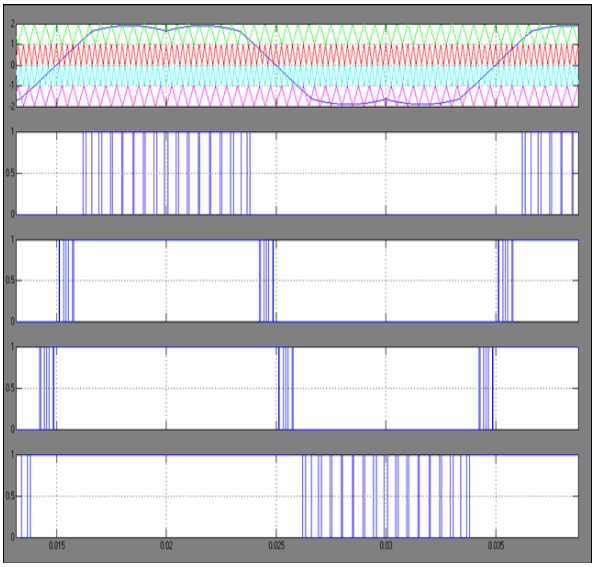

Fig.9. Phase opposition disposition sinusoidal with zero sequence pulse width modulation generation.

4. Results

THD and output voltage values for phase disposition and phase opposition disposition for variable switching frequency pulse width modulation are shown in Table 1. The THD and output voltage values are less in the sinusoidal pulse width modulation technique, whereas the values are higher in the sinusoidal with zero sequence signal technique. It is determined that to minimize THD and to enhance the output voltage, that sinusoidal pulse width modulation is better than sinusoidal pulse width modulation with zero sequence signal.

TABLE 1

PWM METHODS	SPWM		SPWM with ZS	
	THD %	V_{AC}	THD%	V_{AC}
VCF-PD	**10.10**	**180.1**	**22.45**	**200.0**
VCF-POD	**11.39**	**199.9**	**23.68**	**220.1**

4.A. Simulation Results

The simulation parameters for variable switching frequency pulse width modulation are as follows:

Inverter rating = 500VA
Three-phase load R = 100 Ohms & L = 20mH
Voltage level of each source Vdc = 100V
Switching frequency = 2 kHz and 4 kHz

Figs. 10 and 11 show the simulated results of the phase disposition sinusoidal pulse width modulation of an output phase voltage and harmonic spectrum.

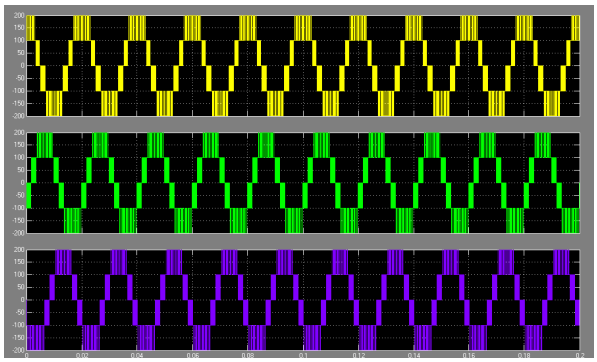

Fig.10. Simulation output voltage for PD sinusoidal pulse width modulation.

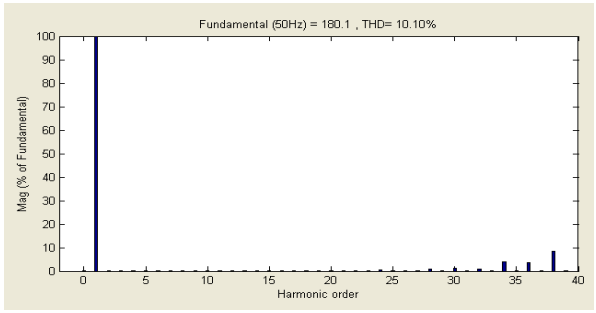

Fig.11. Harmonic spectrum for PD sinusoidal pulse width modulation.

Figs. 12 and 13 show the simulated results of the phase disposition sinusoidal with zero sequence pulse width modulation of an output phase voltage and harmonic spectrum.

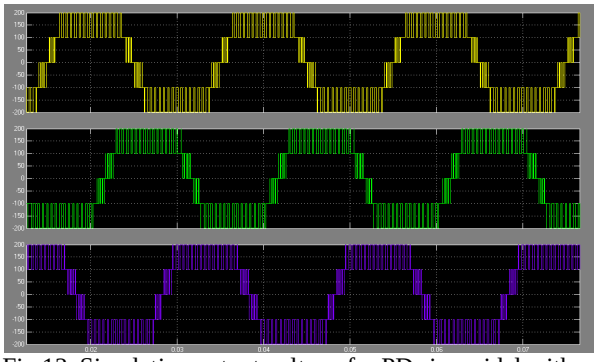

Fig.12. Simulation output voltage for PD sinusoidal with zero sequence pulse width modulation.

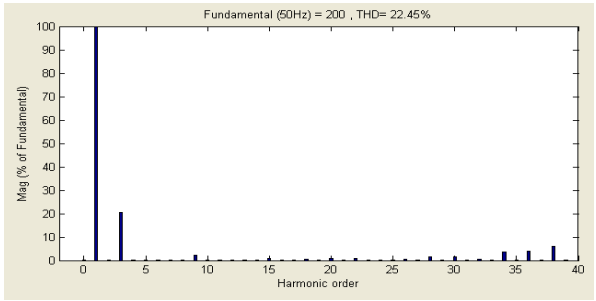

Fig.13. Harmonic spectrum for PD sinusoidal with zero sequence pulse width modulation.

Figs. 14 and 15 show the simulated results of the phase opposition disposition sinusoidal pulse width modulation of an output phase voltage and harmonic spectrum.

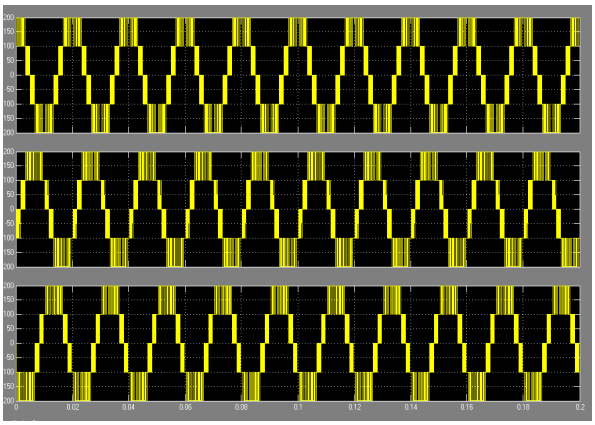

Fig.14. Simulation output voltage for POD sinusoidal pulse width modulation.

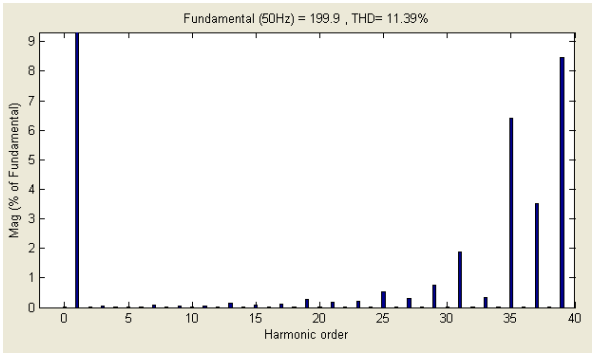

Fig.15.Harmonic spectrum for POD sinusoidal pulse width modulation.

Figs.16 and 17 show the simulated results of the phase opposition disposition sinusoidal with zero sequence pulse width modulation of an output phase voltage and harmonic spectrum.

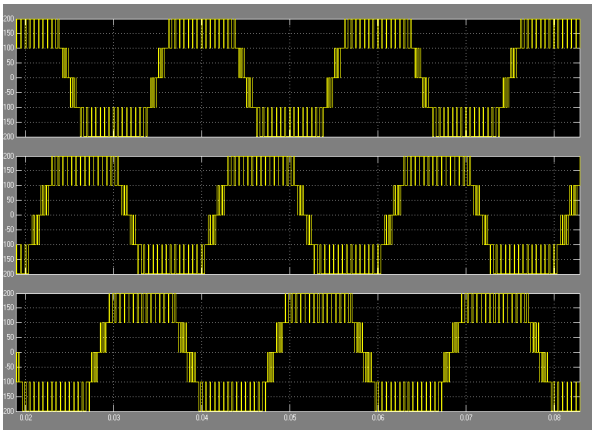

Fig.16. Simulation output voltage for POD sinusoidal with zero sequence pulse width modulation.

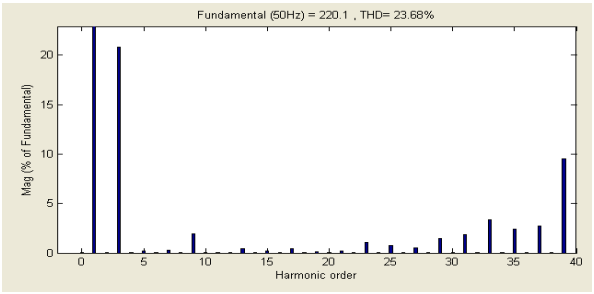

Fig.17.Harmonic spectrum for POD sinusoidal with zero sequence pulse width modulation.

5. *B. Hardware Results*

A 500VA hardware setup of the three-phase five-level cascaded inverter has been built to validate the theoretical analysis. The hardware parameters for variable switching frequency pulse width modulation are as follows:
Three-phase load, R = 100 Ohms , L = 20mH
Voltage level of each source Vdc = 100V
Fundamental frequency = 50Hz
Switching frequency = 2 kHz & 4 kHz
Xilinx Spartan – DSP controller (FPGA)

The three phase output voltage waveform for the variable switching frequency phase disposition sinusoidal pulse width modulation method is shown in Fig. 18, and the phase disposition sinusoidal pulse width modulation with zero sequence signal method is shown in Fig. 19.

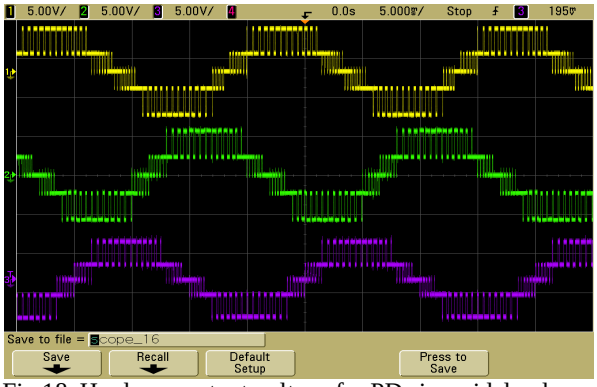

Fig.18. Hardware output voltage for PD sinusoidal pulse width modulation.

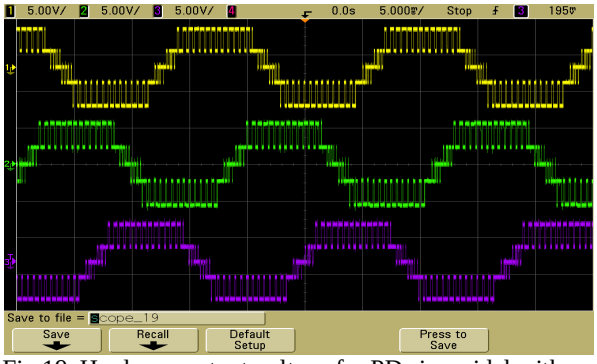

Fig.19. Hardware output voltage for PD sinusoidal with zero sequence pulse width modulation.

The output voltage waveform for the variable switching frequency phase opposition disposition sinusoidal pulse width modulation method is shown in Fig.20, and the phase disposition sinusoidal pulse width modulation with zero sequence signal method is shown in Fig. 21.

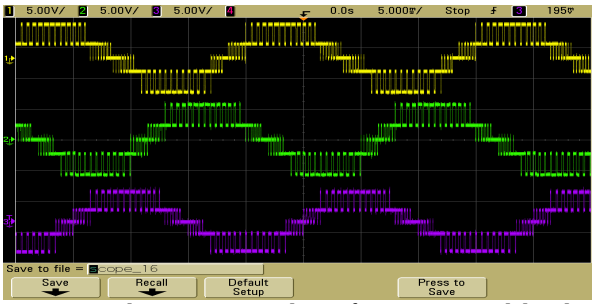

Fig.20. Hardware output voltage for PD sinusoidal pulse width modulation.

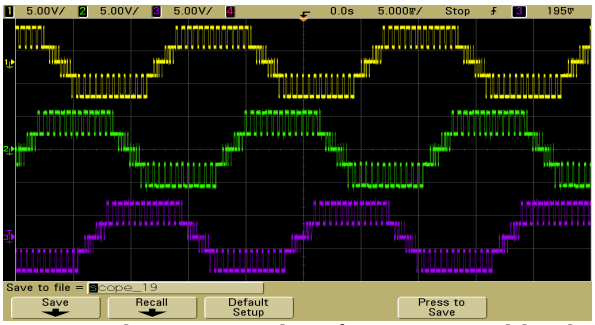

Fig.21. Hardware output voltage for POD sinusoidal with pulse width modulation.

6. Conclusion

In this paper, two new schemes adopting the phase disposition and phase opposition disposition variable switching frequency multicarrier pulse width modulation concepts are considered. The sinusoidal pulse width modulation and sinusoidal pulse width modulation with zero sequence signal techniques are analyzed with all three methods. It is observed that the sinusoidal pulse width modulation and sinusoidal pulse width modulation with zero sequence signal in phase shifted carrier pulse width modulation gives better results than the other two methods. Here, the sinusoidal pulse width modulation strategy reduces the total harmonic distortion and the sinusoidal pulse width modulation with zero sequence signal strategy enhances the fundamental output voltage. The multilevel inverter improves the output voltage, and reduces total harmonic distortion and voltage stress on the semiconductors switches. The results are validated by simulation and experimental hardware setup.

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