Selective Harmonics Elimination PWM with Self-Balancing DC-link Capacitors in Five-Level Inverter

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Abstract. In this paper it is shown that the make use of the redundant states with selective harmonics elimination PWM in the case of multilevel inverters is possible so as to produce the required fundamental voltage while at the same time not generate higher order harmonics and balance the four *dc* voltage sources without additional circuitry.

Key words

Multilevel converter, SHEPWM, Redundant states, Self-balancing.

1. Introduction

Multilevel inverter has been attracting extensive attention from academia as well as industry in the recent decade. They have emerged as the solution to many problems related to the traditional two-level inverter. The principal advantage is to generate a good waveform quality reducing the voltage stresses on power semiconductor devices [1][2]. So, they are very useful in high power *ac* applications. Several multilevel-PWM methods are developed for the two-level inverter and expanded to the multiple levels. The most popular are the multilevel carrier-based PWM derivatives. However, these techniques offer good performances using high switching frequency [3]. The SHEPWM-based method can theoretically provide various performance advantages over all the PWM methods [4][5]. These advantages include, produced the desired fundamental sinusoidal voltage while at the same time certain order harmonics are eliminated.

Otherwise, the use of this kind of inverter poses the dc-link capacitor unbalance problem [7]. Two main approaches have been proposed. 1) The use of additional passive and/or active components. 2) The manipulation of the redundant switching states.

The first solution causes an increase of system cost and additional power losses. For the second one, it is generally used in the space vector PWM.

In fact, this paper shows that the redundant states can be associated to the selective harmonics elimination PWM in order to improve more and more the performance system in term of quality signal and power losses.

2. NPC Five Level Inverter

The three legs of the NPC five-level inverter is shown in Fig.1. The input inverter is formed by four storage capacitors. Turning-on the suitable switches can produce five different voltage levels by leg (V_{dc}, ¾ V_{dc} , ½ V_{dc}, ¼ V_{dc}, 0), as shown the stepped waveforms of fig.2.(b). The commutation of the switches permits the addition of the capacitor voltages which reach high voltage at the output.

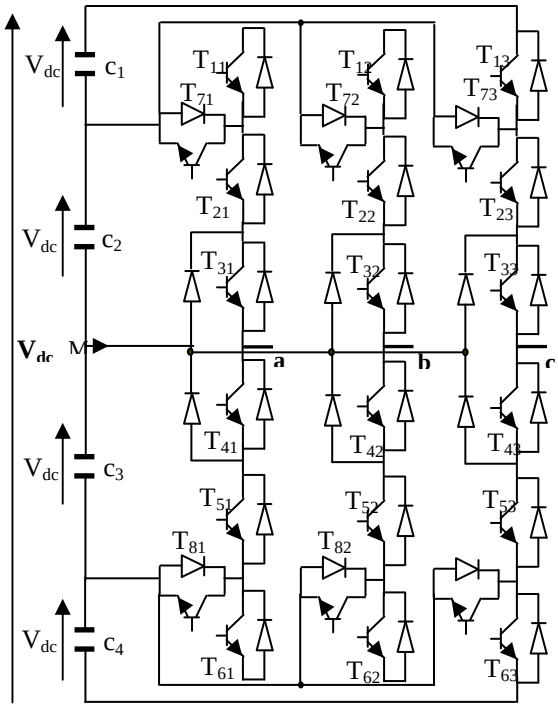


Fig.1. Schematic diagram of a NPC-5-level inverter

Table I. – Equivalent Commutation Circuit

Gate signals			*Switching functions*						
T_{1k}	T_{2k}	T_{3k}	f_{1c}	f_{2c}	f_{3c}	f_{4c}	V_{km}	V_{c0}	$S_{w(a,b,c)}$
1	1	1	1	0	0	0	$2\ V_{dc1}$	U_{s1}	4
0	1	1	0	1	0	0	V_{dc1}	$3/4\ U_{s1}$	3
0	0	1	0	0	1	0	0	$1/2\ U_{s1}$	2
1	0	0	0	0	0	1	$-\ V_{dc1}$	$1/4\ U_{s1}$	1
0	0	0	0	0	0	0	$-2\ V_{dc1}$	0	0

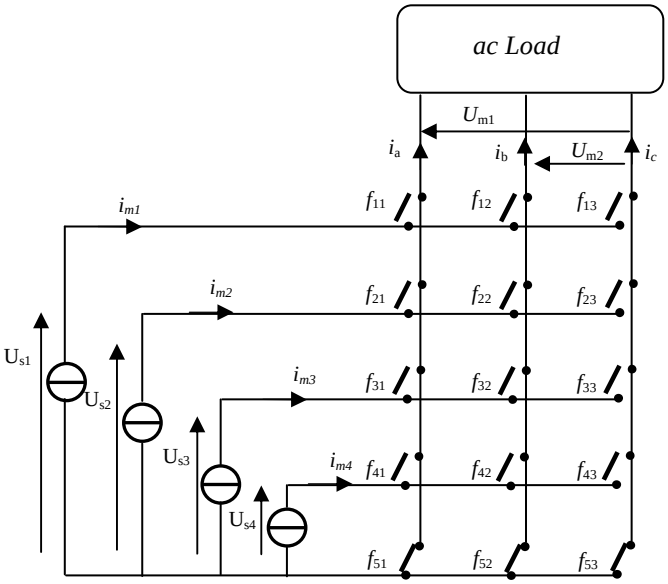
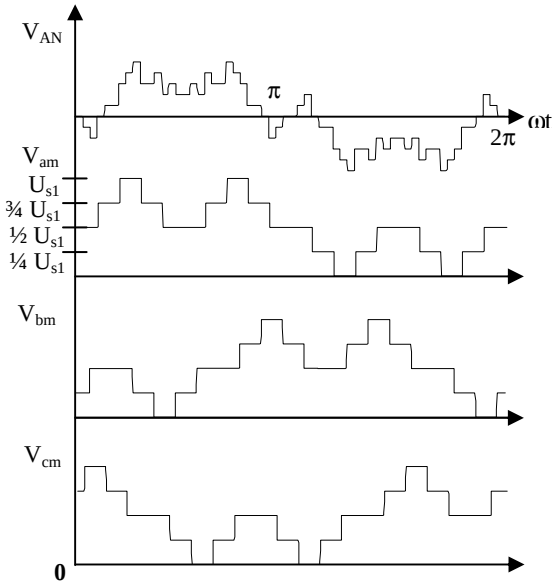


Fig.2. (a) Equivalent matrix inverter representation



(b) Staircase waveform produced by 4 *dc* multilevel inverter

It has been proved the five-level inverter is equivalent to commutation circuits with five ideal switches instead of eight (Fig.2.(a)).

So, the five-level NPC inverter is equivalent of 2*5 matrix inverter. The switches functions (f_{rk}) are related to the gate transistor signals (T_{rk}) by the relations of system (1):

$$\begin{cases} f_{1k} = T_{1k}\,T_{2k}\,T_{3k} \\ f_{2k} = T_{2k}\,T_{3k} \\ f_{1k} = \overline{T_{1k}}\,\overline{T_{2k}}\,T_{3k} \\ f_{4k} = T_{1k}\,\overline{T_{2k}}\,\overline{T_{3k}} \end{cases} \quad (1)$$

$k \in \{1,2,3\}$ *related to the legs* a, b, c

$r \in \{1,2,3,4,...\}$ *related to the switches number*

Moreover, voltage vectors in (U_{m1}, U_{m2}, *0*) plane are the functions of inverter switches states S_a, S_b, S_c. Using the expression (2) results in 125 (5^3) switching states that produce only 61 distinct voltage vectors.

$$Vs = \sqrt{\frac{2}{3}} V_{dc}[S_{wa} + S_{wb}\,e^{j2\pi/3} + S_{wc}\,e^{j4\pi/3}] \quad (2)$$

Where S_{wi} i∈(a, b, c) represents the four legs states Tab.I. Figure 3 gives the position of the 125 vectors in the (U_{m1}, U_{m2}, *0*) plane. Where U_{m1} and U_{m2} are the modulation voltages related to the phases *a* and *b*. Among the four hexagons, three represent the redundant switching configurations. The closer one to the center is formed by voltage vectors having two redundancies (a,b). The second hexagon contains vectors with three redundancies (a,b,c) and each vector of the fourth one have four states (a,b,c,d). The center vector represents the zero voltage. It has five switch states.

The modulation voltages expressed by the *dc* voltages and the switche functions are given as:

$$\begin{aligned} U_{m1} &= (V_{am} - V_{cm}) = m_{11}U_{s1} + m_{21}U_{s2} + m_{31}U_{s3} + m_{41}U_{s4} \\ U_{m2} &= (V_{bm} - V_{cm}) = m_{12}U_{s1} + m_{22}U_{s2} + m_{32}U_{s3} + m_{42}U_{s4} \end{aligned} \quad (3)$$

With:

$$\begin{cases} m_{11} = (f_{11} - f_{13}), \quad m_{12} = (f_{12} - f_{13}) \\ m_{21} = (f_{21} - f_{23}), \quad m_{22} = (f_{22} - f_{23}) \\ m_{31} = (f_{31} - f_{33}), \quad m_{32} = (f_{32} - f_{33}) \\ m_{41} = (f_{41} - f_{43}), \quad m_{42} = (f_{42} - f_{43}) \end{cases} \quad (4)$$

Table II. – Voltage Vector for the Example

U		U_{m1}	U_{m2}	Sw_a	Sw_b	Sw_c
⋮						⋮
6	a	-3	-3	0	0	3
6	b	-3	-3	1	1	4
7	a	-3	-2	0	1	3
7	b	-3	-2	1	2	4
⋮						⋮

The third modulated voltage is unnecessary for the modeling because it is linked to other ones by:

$$U_{m3} = U_{m1} - U_{m2} \tag{5}$$

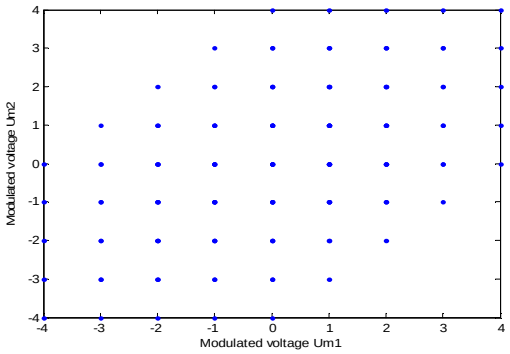


Fig.3. The space vector voltages of five-level inverter (U_{m1}, U_{m2},0)

In our study, the proposed method is applicable in the case of *Vdc* constant, so:

$$\frac{dV_{dc}}{dt} = \frac{dV_{dc1}}{dt} + \frac{dV_{dc2}}{dt} + \frac{dV_{dc3}}{dt} + \frac{dV_{dc4}}{dt} \tag{6}$$

Therefore:

$$0 = \frac{1}{c} i_{c1} + \frac{1}{c} i_{c2} + \frac{1}{c} i_{c3} + \frac{1}{c} i_{c4} \tag{7}$$

By using this relation, the current capacitors are:

$$\begin{cases} i_{c1} = 1/4(3i_{m2} + 2i_{m3} + i_{m4}) \\ i_{c2} = -1/4(i_{m2} - 2i_{m3} - i_{m4}) \\ i_{c3} = -1/4(i_{m2} + 2i_{m3} - i_{m4}) \\ i_{c4} = -1/4(i_{m2} + 2i_{m3} + 3i_{m4}) \end{cases} \tag{8}$$

These equations function of the current load are given as follow:

$$\begin{cases} i_{c1} = a_{11} i_a + a_{12} i_b \\ i_{c2} = a_{21} i_a + a_{22} i_b \\ i_{c3} = a_{31} i_a + a_{32} i_b \\ i_{c4} = a_{41} i_a + a_{42} i_b \end{cases} \tag{9}$$

Where :

$$\begin{cases} a_{21}=1/4(m_{11}-2m_{21}-m_{31}-2m_{41}),\ a_{22}=1/4(m_{12}-2m_{22}-m_{32}-2m_{42}) \\ a_{11}=1/4(-3m_{11}-2m_{21}-m_{31}-2m_{41}),\ a_{12}=1/4(-3m_{12}-2m_{22}-m_{32}-2m_{42}) \\ a_{31}=1/4(m_{11}+2m_{21}+3m_{31}+2m_{41}),\ a_{32}=1/4(m_{12}+2m_{22}+3m_{32}+2m_{42}) \\ a_{41}=1/4(m_{11}+2m_{21}-m_{31}+2m_{41}),\ a_{42}=1/4(m_{12}+2m_{22}-m_{32}+2m_{42}) \end{cases} \tag{10}$$

3. Selective Harmonics Elimination PWM

The principle of the SHEPWM is to compute the suitable switching angles so as provide an output waveform without certain lower harmonics order. In our study the target is to cancel the 5th, 7th, 11th harmonics and to control as well as possible the fundamental voltage at the same time. Therefore, we have firstly to choose the leg waveform profile with four commutations per quarter of period (Fig.4).

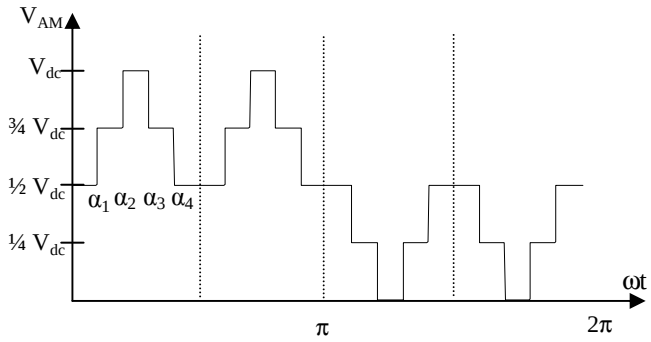


Fig.4. Assigned form of the leg voltage for the 5-level inverter

To proceed, note that the signals related to the three legs have a Fourier series expression of the form:

$$V_{km}(\omega t) = \frac{V_{dc}}{\pi n} \sin(\omega t) \sum_{n=1,3,5,..}^{\infty} [\ell_1 \cos(n\alpha_1) + \ell_2 \cos(n\alpha_2) + ... + \ell_c \cos(n\alpha_c)] \tag{11}$$

Where: n is the harmonic number, c the considered number of angles necessary to eliminate (c-1) harmonics and ℓ_i are unitary coefficients depending on the form of the arm voltage (Fig.4).

In the case of figure 4, these parameters are as follows:

n= 5, 7 and 11, c=4,
ℓ_1=1, ℓ_2=1, ℓ_3=–1, ℓ_4=–1.

Under the constraint:

$$0 \le \alpha_1 \le \alpha_2 \le \alpha_3 \le \alpha_4 < \frac{\pi}{2} \tag{12}$$

While replacing these parameters in the equation 11 and introducing the modulation index *r*, we obtain the system (13) of algebraic equations.
Using the resultant theory method, the solutions of the system 13 are given in the figure 5 [6].
For some modulation range multiple solutions exist. So, a choice of suitable angles is possible. The selection is based on the lower THD offer by the switching angles of these modulation indices. The results are given in figure 6.

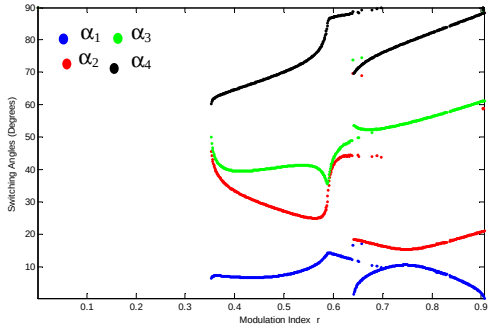
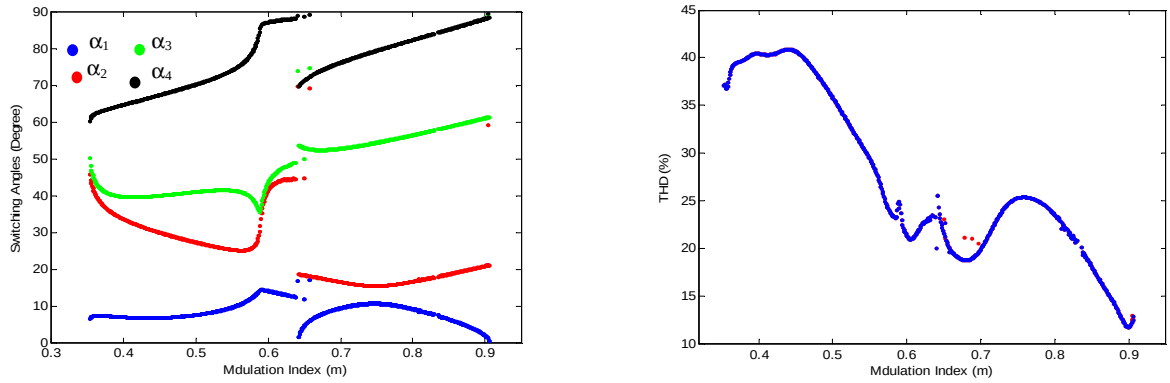


Fig.5. Switching angles of a five levels inverter obtained by the resultant theory



(a) (b)

Fig.6.The optimized switching angles (a) given the best THD (b)

Table III. – Voltages and Current Equation for Example

						i_{c1}		i_{c2}		i_{c3}		i_{c4}	
	S_{wa}	S_{wb}	S_{wc}	U_{m1}	U_{m2}	a_{11}	a_{12}	a_{21}	a_{22}	a_{31}	a_{32}	a_{41}	a_{42}
.	…	…	…	…	…	…	…	…	…	…	…	…	…
a	0	0	3	-3	-3	3	3	-1	-1	-1	-1	-1	-1
b	1	1	4	-3	-3	-1	-1	-1	-1	-1	-1	3	3
.	…	…	…	…	…	…	…	…	…	…	…	…	..

$$\begin{cases} \cos(\alpha_1)+\cos(\alpha_2)-\cos(\alpha_3)-\cos(\alpha_4)=\dfrac{r\pi}{2} \\ \cos(5\alpha_1)+\cos(5\alpha_2)-\cos(5\alpha_3)-\cos(5\alpha_4)=0 \\ \cos(7\alpha_1)+\cos(7\alpha_2)-\cos(7\alpha_3)-\cos(7\alpha_4)=0 \\ \cos(11\alpha_1)+\cos(11\alpha_2)-\cos(11\alpha_3)-\cos(11\alpha_4)=0 \end{cases} \quad (13)$$

With $r=\dfrac{V_{\max}}{2V_{dc}}$

In order to bear out the validity of the SHE strategy, a test is carried out for r = 0.8. The switching angles resulting from figure 6.(a) lead to a phase voltage and a harmonics spectrum shown in figure 7.

By analyzing figures 5 and 7, we note that the aim of the SHEPWM is achieved [6]. All the solutions system are determined using the resultant theory method instead of *Newton-Rphson* method. In addition, the three undesirable harmonics are cancelled with a good control of the fundamental one.

4. Proposed DC-link Balancing Technique

The inverter is fed by a five-level rectifier to supply an induction motor.The rectifier is controlled by sinusoidal carrier-based PWM. To achieve the balancing of the divider capacitors, we have first to stabilize the rectifier output voltage. This can be carried out using PI controller.

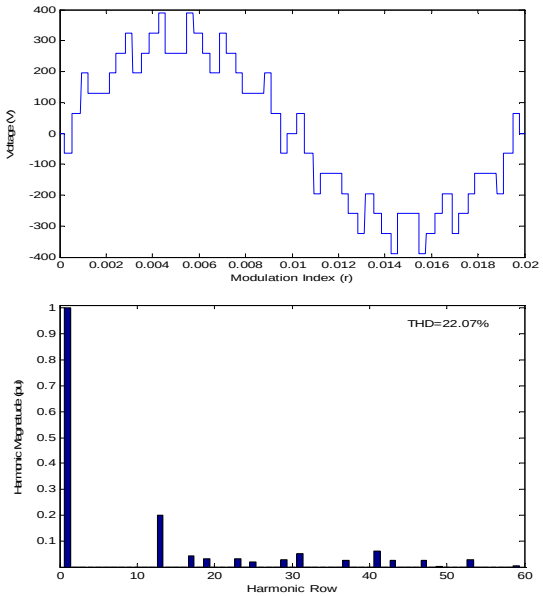


Fig.7. Output line voltage waveform of a five level inverter and its frequency spectrum (m = 0.8)

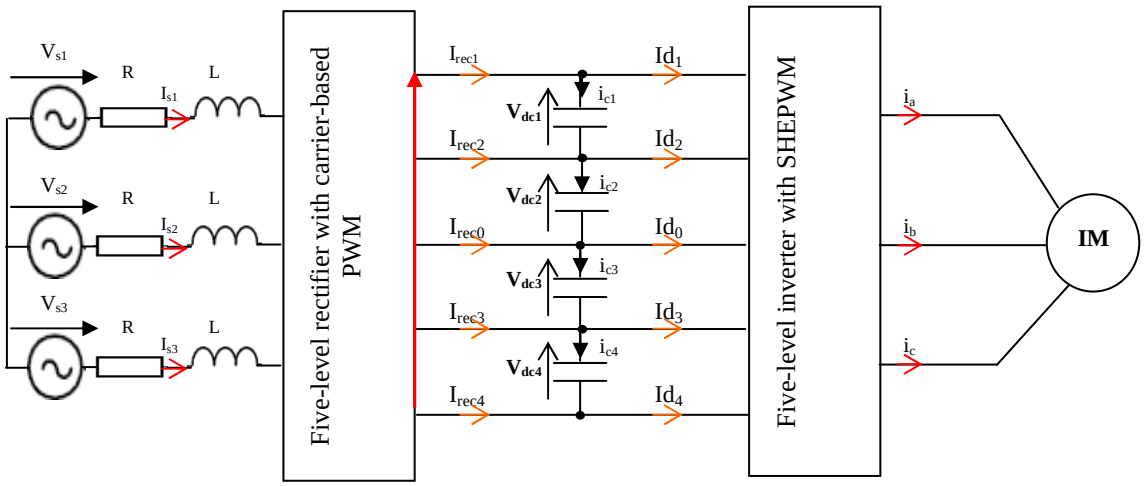


Fig.8. 5-level rectifier –5-level inverter – Induction Motor

In order to keep the four voltages equal, we will make use of the switch states of the 5-level inverter. Three groups are distinguished from 125 switch states. The first one (last hexagon Fig.3) is formed by 24 vectors which do not connect any of the phases to the common capacitors potential and so the capacitor voltages remains unaffected. The second group has 36 vectors with multiple switch states (61).

The last one is the vector zero with five different switch states. They have any effect on the DC-link voltages. So, only the second group will be used to ensure the capacitor voltages balance.

Different switch states force load current to flow through different paths. Thus the direction of current through the DC-link capacitors is different and variation of capacitor voltages is different. We express the capacitor currents by the two *ac* load current i_a and i_b (Fig.2.a & Eq.8). According to their sign, we can know the effect of each state on the capacitor behaviour (charge or discharge). The principle of the balancing algorithm is to minimize the difference between the voltages of the four capacitors by selecting the suitable redundancy among the voltage vectors of group 2. The switch state selected has to unload the most loaded capacitor voltage and load the unloaded one.

Therefore, 24 capacitor voltage derivations have to be considered. As an example, let imagine the following state of the dc-link voltages:

$V_{dc1} < V_{dc2} < V_{dc3} < V_{dc4}$, and the actual modulation obtained by the SHEPWM is 1 1 4 that correspond to the voltage vector (U_{m1},U_{m2}=-3,-3) with V_{dc}=4 (Tab.II).

Using the equations system (8) the coefficients a_{ij} take the values given in table III. According to this table, only C_1 and C_4 can be affected by the changing of the switch state for the vector (-3,-3). If $i_{c1} < 0$ we have to substitute the modulation 1 1 4 by the first redundancy (0 0 3) which allows charging C_1 and discharging C_4. In the contrariwise, we let the initial state.The same operation is done using the PWM signal given by the SHE technique

At the end, we obtain another leg voltage waveform which provides the same modulation voltage waveform and the same harmonics spectrum (Fig.6).

The proposed capacitor balancing method has been assessed by simulation. The five-level inverter operates with two different loads: static and dynamic.

Figure 9.(a) shows the capacitor voltages for the first load at different modulation indices and capacitor voltages are unbalancing from the beginning. The *dc* rail voltage and capacitances are 400 V and 7µF, respectively. At 2.25s the DC-link balancing is reached.

To investigate the effect of dynamic loading on dc-link capacitor balancing, we have replaced the static load by an induction motor (Appendix).

The *dc* rail voltage is fixed at 800V, the capacitances at 20 mF and the modulation index at 0.8. The dc-link voltages are depicted in figure 9.(b).

Firstly, the output voltage rectifier tracks the desired value (800V) using the PI regulator. The same observation about current source using the rectifier carrier-based PWM. It is on the phase with the voltage source.

From figure 9.(b), it can be seen the capacitor voltages maintain balanced while keeping the SHEPWM proprieties.

The most important error is obtained during the changing machine operation from the start-up state to the the steady state.

5. Conclusion

Both optimization of switching angles of 5-level output waveform using SHEPWM and DC-link voltages balance are investigated in this study. The programmed PWM allows eliminating harmonics row 5, 7 and 11 with a good control of the fundamental voltage. In order to keep as well as possible the four capacitor voltages equal, we have made use the 61 switch states of the 5-level inverter. Its matrix representation simplify the redundant states analyze. The obtained results show the DC-link balancing while maintaining the SHEPWM performances.

Appendix

a) RL load: R=2Ω L=50mH.

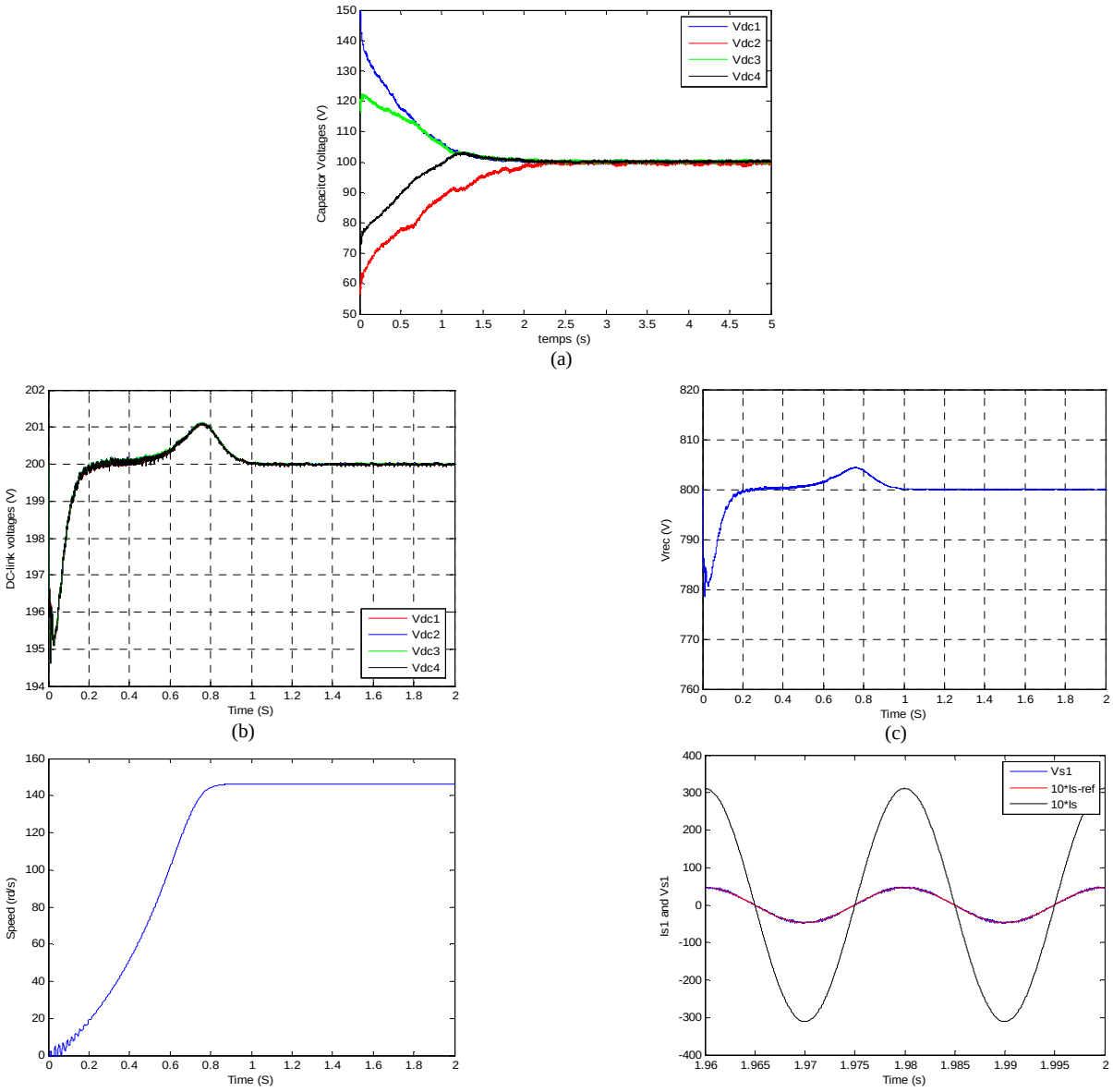


Fig.9.The performances cascade: (a)-DC-link voltages for static load, (b) - DC-link voltages for dynamic load, (c)-Output voltage rectifier, (d)-Induction Motor speed, (e)- The line current and voltage source .

b) Machine Parameters (7.5 KW)

Rs=0,455 Ω ; Rr=0,62 Ω ; Ls=0,084 H ; Lr=0,081 H ; M= 0.078 H ; J=0.3125 kg.m² ;f=6,73.10-3 N.m.s-1

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