Study on Split-Capacitors Applied in Positive Output Super-Lift Luo-Converters

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Abstract — **Voltage Lift Technique has been successfully employed in design of DC/DC converters, e.g. three series Luo-Converters. However, the output voltage increases in arithmetic progression. Super Lift Technique is the most significant contribution in Power Electronics, e.g. four series Super-Lift Converters. Their output voltage increases in geometric progression. This paper introduces a novel approach – Super Lift Technique Armed by Split-Capacitors that implements the output voltage increasing in higher geometric progression. It effectively enhances the voltage transfer gain in power series as well**.

***Index Terms* —** *Voltage Lift Technique, Super-Lift Technique, Arithmetic/Geometric Progression, Super Lift Technique Armed by Split-Capacitors, Power Series, Voltage Transfer Gain.*

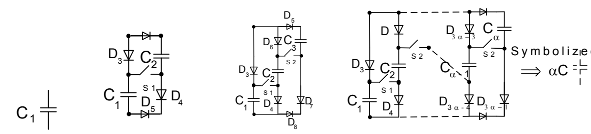
I. INTRODUCTION

Voltage Lift (VL) Technique is a popular method widely used in electronic circuit design. It has been successfully employed in DC/DC converter applications in recent decades, and opened a way to design high voltage gain converters. Three series Luo-Converters [1–3] are the examples of VL technique implementations. However, the output voltage increases in stage by stage just along the arithmetic progression [4]. Super Lift (SL) Technique is the most significant contribution in Power Electronics, e.g. four series Super-Lift Converters [4, 5]. Their output voltage increases in geometric progression. This paper introduces a novel approach – Super Lift Technique Armed by Split-Capacitors that implements the output voltage increasing in stage by stage along higher geometric progression. It effectively enhances the voltage transfer gain in power series as well [6 - 8].

In order to sort these converters different from existing VL converters, we entitle these converters "Positive Output Super-lift Luo-Converters armed by Split-Capacitors". There are few sub-series, we only introduce two subseries: ***main series*** and ***additional series*** in detail in this paper, and summarize other series. Each circuit of the main series and additional series has one switch S, n inductors (where n is the stage number), other capacitors and diodes. The conduction duty ratio is k, switching frequency is f, switching period is T = 1/f, the load is resistive load R. The input voltage and current are V_{in} and I_{in}, out voltage and current are V_O and I_O. Assume no power losses during the conversion process, V_{in} x I_{in} = V_O x I_O. The voltage transfer gain is G: $G = \frac{V_O}{V_{in}}$

II. SPLIT-CAPACITORS

A capacitor C_1 as shown in Figure 1 (a) can be split into two parts: two capacitors C_1 and C_2 as shown in Figure 1 (b); and three parts: three capacitors C_1 , C_2 and C_3 as shown in Figure 1 (c). Furthermore, it can be split into α parts that are shown in Figure 1 (d).



(a) (b) (c) (d)

Figure 1. The single capacitor, and α split capacitors: (a) One capacitor, (b) Two Split capacitors, (c) Three Split capacitors (d) α Split capacitors.

The split stage can be defined α-times. Now, we define the single capacitor to be in α = 1 split stage as shown in Figure 1 (a); We define the two split capacitors to be in α = 2 split stage as shown in Figure 1 (b), the slave switch S1 is exclusively switched with the Main switch S; We define the three split capacitors to be in α = 3 split stage as shown in Figure 1 (c), the slave switches S1 and S2 are exclusively switched with the Main switch S. We define the α split capacitors to be symbolized by **αC**. These capacitors can be charged by a DC voltage V_{in}. In the steady-state, each capacitor is assumed to be charged to the source voltage V_{in}. All split capacitors are charged by source voltage V_{in} in parallel. When the capacitors are discharged, all split capacitors are discharged by an external voltage in series.

III. SPLIT CAPACITORS APPLIED IN THE ELEMENTARY POSITIVE OUTPUT SUPER-LIFT LUO-CONVERTER

Elementary positive output (P/O) super-lift Luo-converter is shown in Figure 2. Its circuit diagram in Figure 2 (a), and its equivalent circuits in switch-on and switch-off are shown in Figure 2 (b) and (c) respectively.

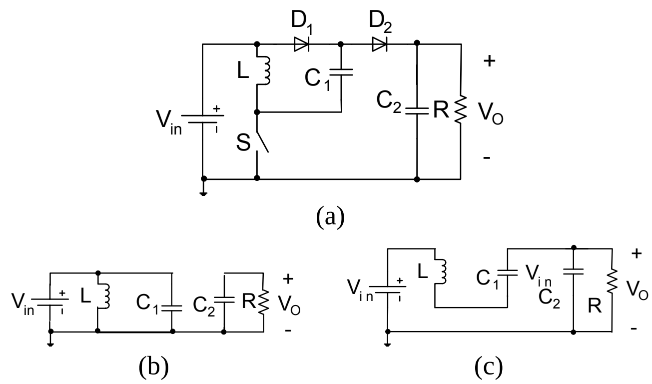


Figure 2. Elementary P/O SL Luo-Converter: (a) Circuit diagram, (b) Equivalent circuit during switching-on, (c) Equivalent circuit during switching-off.

The Elementary circuit and its equivalent circuits during switching-on and -off are shown in Figure 2. The voltage across capacitor C_1 is charged to V_{in} in the steady state. The current i_L flowing through inductor L increases with voltage V_{in} during switching-on period kT and decreases with voltage $-(V_O - 2V_{in})$ during switching-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_L is:

$$\Delta i_L = \frac{V_{in}}{L} kT = \frac{V_O - 2V_{in}}{L}(1-k)T \tag{1}$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \frac{2-k}{1-k} \tag{2}$$

A. A 2 Split Capacitors (α = 2) Applied in The Elementary P/O SL Circuit.

If the capacitor C_1 is split to two capacitors C_1 and C_2, The circuit and its equivalent circuits during switching-on and -off are shown in Figure 3 (as mentioned that the slave switch S1 is exclusive switch with the Main switch S).

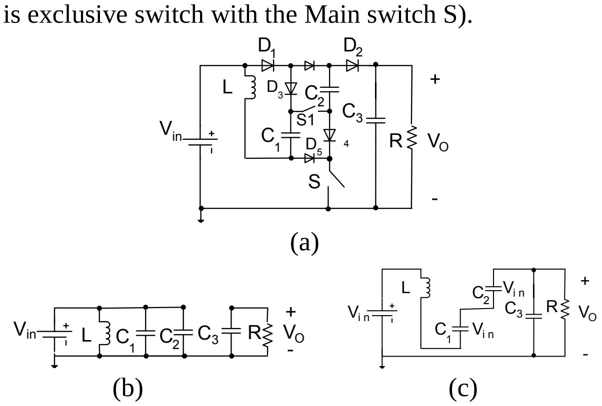


Figure 3. A two split capacitors applied in the Elementary P/O SL Luo-Converter: (a) Circuit diagram, (b) Equivalent circuit during switching-on, (c) during switching-off.

The voltage across capacitors C_1 and C_2 are charged to V_{in} in the steady state. The current i_L flowing through inductor L increases with voltage V_{in} during switching-on period kT and decreases with voltage $-(V_O - 3V_{in})$ during switching-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_L is:

$$\Delta i_L = \frac{V_{in}}{L} kT = \frac{V_O - 3V_{in}}{L}(1-k)T \tag{3}$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \frac{3-2k}{1-k} \tag{4}$$

B. A 3 Split Capacitors (α = 3) Applied in The Elementary P/O SL Circuit.

If the capacitor C_1 is split to three capacitors C_1, C_2 and C_3, The circuit and its equivalent circuits during switching-on and -off are shown in Figure 4 (as mentioned that the slave switches S1 and S2 are exclusively switched with the Main switch S).

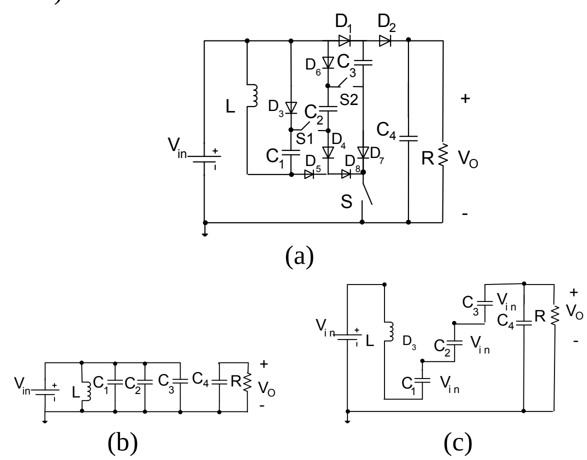


Figure 4. Elementary P/O SL Luo-Converter armed by three split capacitors. (a) Circuit diagram; (b) Equivalent circuit during switching-on; (c) during switching-off.

The voltage across capacitors C_1, C_2 and C_3 are charged to V_{in} in the steady state. The current i_L flowing through inductor L increases with voltage V_{in} during switching-on period kT and decreases with voltage $-(V_O - 4V_{in})$ during switching-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_L is:

$$\Delta i_L = \frac{V_{in}}{L} kT = \frac{V_O - 4V_{in}}{L}(1-k)T \tag{5}$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \frac{4-3k}{1-k} \tag{6}$$

C. A α Split Capacitors Applied in the Elementary P/O SL Circuit.

If the capacitor C_1 is split to α capacitors, the circuit is shown in Figure 5.

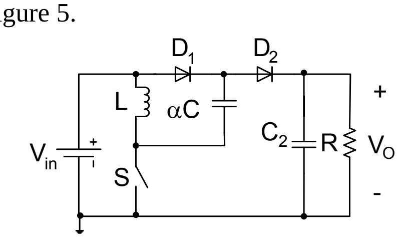


Figure 5. A α split capacitors applied in the Elementary P/O SL Luo-Converter.

The voltage across the α capacitors are charged to V_{in} in parallel during switch-on in the steady state. The current i_L flowing through inductor L increases with voltage V_{in} during switching-on period kT and decreases with voltage $-[V_O - (\alpha+1)V_{in}]$ during switching-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_L is:

$$\Delta i_L = \frac{V_{in}}{L} kT = \frac{V_O - (\alpha+1)V_{in}}{L}(1-k)T \qquad (7)$$

The voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = \frac{\alpha+1-\alpha k}{1-k} \qquad (8)$$

IV. MAIN SERIES

The Main series has several Circuits such as Re-lift circuit, Triple-lift circuit and high-order-lift circuit. We defined the stage as n = 1 means Elementary circuit; n = 2 means Re-Lift circuit, n = 3 means Triple-lift circuit, and n can be higher number means the high-order-lift circuit. Figure 5 shows the Elementary circuit. Figure 6 shows the Re-Lift circuit, and Figure 7 shows the Triple-Lift circuit.

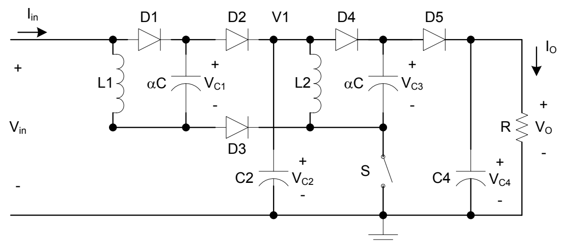


Figure 6. The Re-Lift circuit

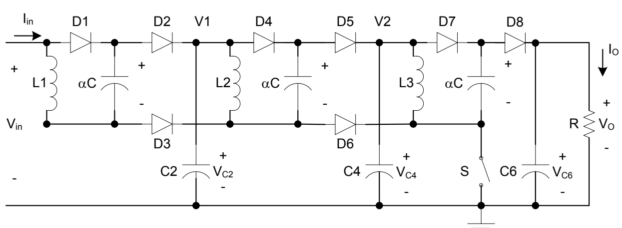


Figure 7. The Triple-Lift circuit

The voltage transfer gain of the Re-Lift circuit is

$$G = \frac{V_O}{V_{in}} = (\frac{\alpha+1-\alpha k}{1-k})^2 \qquad (9)$$

The voltage transfer gain of the Triple-Lift circuit is

$$G = \frac{V_O}{V_{in}} = (\frac{\alpha+1-\alpha k}{1-k})^3 \qquad (10)$$

The voltage transfer gain of the nth-order-Lift circuit, if each stage use split capacitor αC, the voltage transfer gain is

$$G = \frac{V_O}{V_{in}} = (\frac{\alpha+1-\alpha k}{1-k})^n \qquad (11)$$

It is a very high voltage transfer gain. For example, if Vin = 20 V, n = 3, α = 4 and k = 0.5, the voltage transfer gain G is equal to 216. The output voltage will be 4320 V!

V. MEC, SPLIT CAPACITORS USED IN DEC

The original Double/Enhance Circuit (DEC) is shown in Figure 8, which consist of two diodes (D_{11} and D_{12}) and two capacitor (C_{11} and C_{12}).

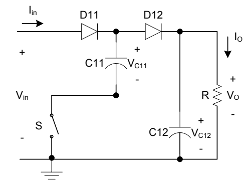


Figure 8. The Double/Enhanced Circuit (DEC)

The output voltage is $V_O = 2V_{in}$ (12)

If the capacitor C_{11} replaced by a γ-split Capacitor γC as show in Figure 9. We can call it Multiple/Enhance Circuit (MEC).

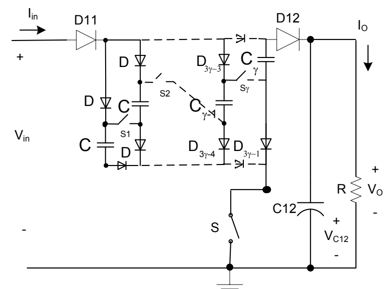


Figure 9. Multiple/Enhance Circuit (MEC)

The output voltage will be $V_O = (\gamma+1)V_{in}$ (13)

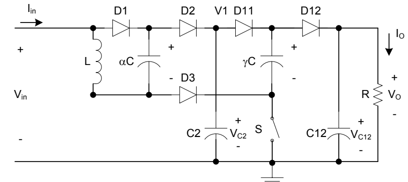
VI. ADDITIONAL SERIES

All circuits of Positive Output Super-Lift Converters – Additional Series are derived from the corresponding circuits of the main series. We can add a MEC following all circuits to obtain the circuits of the Additional Series.

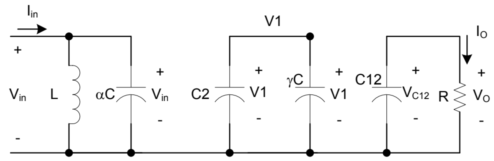
The first three stages of this series are shown in Figures 10 – 12. For convenience to explain, we call them Elementary additional circuit, Re-Lift additional circuit and Triple-Lift additional circuit respectively. We can number them as n = 1, 2 and 3.

A. Elementary additional circuit

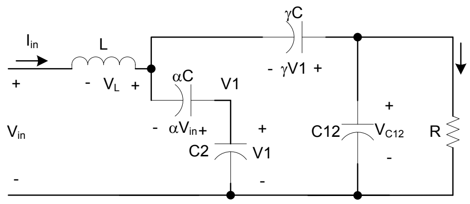
This circuit is derived from Elementary circuit with adding a MEC (D_{11}-D_{12}-γC-C_{12}). Its circuit and switch-on and -off equivalent circuits are shown in Figure 10.



(a) Circuit diagram



(b) Equivalent circuit during switching-on



(c) Equivalent circuit during switching-off

Figure 10. Elementary additional circuit

The voltage across all capacitor αC_2 is V_1 in steady state as shown in Equation (11). The inductor current increases during switch S on, and decreases during switch S off. The current variation is $\frac{V_{in}}{L}kT = \frac{V_O - \gamma V_1 - V_{in}}{L}(1-k)T$ (14)

Therefore the output voltage V_O is

$$V_O = [\frac{1}{1-k} + \gamma\frac{\alpha+1-\alpha k}{1-k}]V_{in} \quad (15)$$

B. Re-Lift additional circuit

This circuit is derived from Elementary additional circuit by adding the parts (L_2-D_3-D_4-D_5-C_3-C_4). Its circuit diagram is shown in Figure 11.

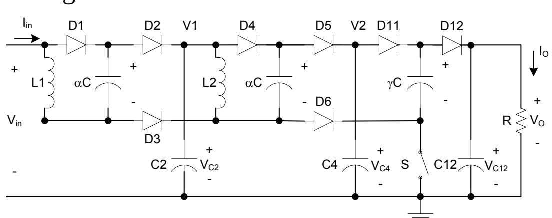


Figure 11. Re-Lift additional circuit

The voltage across capacitor C_2 is charged to V_1 and voltage across capacitor C_4 is charged to V_2. All γC is charged to V_2. The V_2 is shown in Equation (13). The second inductor current increases during switch S on, and decreases during switch S off. The current variation is

$$\frac{V_1}{L_2}kT = \frac{V_O - \gamma V_2 - V_1}{L_2}(1-k)T \quad (16)$$

and $V_2 = \frac{\alpha+1-\alpha k}{1-k}V_1$

Therefore the output voltage V_O is

$$V_O = \frac{V_1}{1-k} + \gamma V_2 = [\frac{1}{1-k} + \gamma(\frac{\alpha+1-\alpha k}{1-k})]V_1$$
$$= [\frac{1}{1-k} + \gamma(\frac{\alpha+1-\alpha k}{1-k})](\frac{\alpha+1-\alpha k}{1-k})V_{in} \quad (17)$$

C. Triple-Lift additional circuit

This circuit is derived from Re-Lift additional circuit by adding the parts (L_3-D_6-D_7-D_8-C_5-C_6). Its circuit diagram is shown in Figure 12.

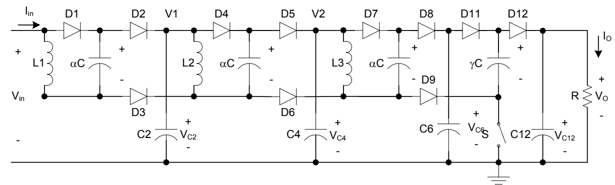


Figure 12. Triple-Lift additional circuit

The voltage across capacitor C_2 is charged to V_1. The voltage across capacitor C_4 is charged to V_2 and voltage across capacitor C_6 is charged to V_3. All γC is charged to V_3 shown in Equation (15). The inductor current increases during switch S on, and decreases during switch S off. The current variation is $\frac{V_2}{L_3}kT = \frac{V_O - \gamma V_3 - V_2}{L_3}(1-k)T$ (18)

and $V_3 = \frac{\alpha+1-\alpha k}{1-k}V_2 \qquad V_2 = (\frac{\alpha+1-\alpha k}{1-k})^2 V_{in}$

Therefore the output voltage V_O is

$$V_O = \frac{V_2}{1-k} + \gamma V_3 = [\frac{1}{1-k} + \gamma(\frac{\alpha+1-\alpha k}{1-k})]V_2$$
$$= [\frac{1}{1-k} + \gamma(\frac{\alpha+1-\alpha k}{1-k})](\frac{\alpha+1-\alpha k}{1-k})^2 V_{in} \quad (19)$$

D. Higher Order Lift additional circuit

Higher Order Lift additional circuit can be designed by just multiple repeating the parts (L_2-D_3-D_4-D_5-C_3-C_4). For nth order lift additional circuit, the final output voltage is

$$V_O = [\frac{1}{1-k} + \gamma(\frac{\alpha+1-\alpha k}{1-k})](\frac{\alpha+1-\alpha k}{1-k})^{n-1}V_{in} \quad (20)$$

VII. Summary of P/O Super-Lift Luo-Converters Applying Split Capacitors

All circuits of Positive Output Super-Lift Luo-Converters using split capacitors αC and MEC (with γC) as a family can be shown in Figure 13 (the family tree). From the analysis of previous two sections we can have the common formula to calculate the output voltage:

$$V_O = \begin{cases} (\frac{\alpha+1-\alpha k}{1-k})^n V_{in} & main\_series \\ [\frac{1}{1-k} + \gamma(\frac{\alpha+1-\alpha k}{1-k})](\frac{\alpha+1-\alpha k}{1-k})^{n-1}V_{in} & additional\_series \end{cases} \quad (21)$$

The voltage transfer gain is

$$G = \begin{cases} (\frac{\alpha+1-\alpha k}{1-k})^n & main\_series \\ [\frac{1}{1-k} + \gamma(\frac{\alpha+1-\alpha k}{1-k})](\frac{\alpha+1-\alpha k}{1-k})^{n-1} & additional\_series \end{cases} \quad (22)$$

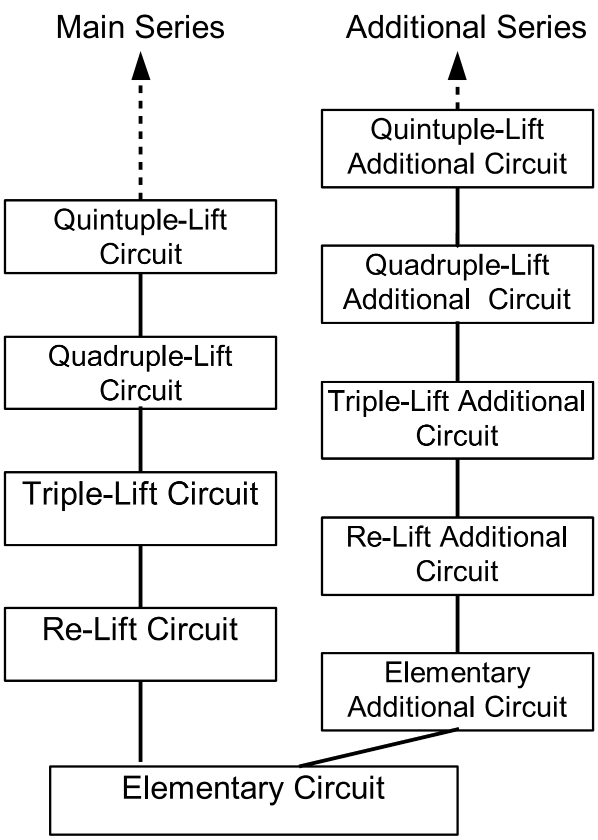


Figure 13. The family tree of p/o super-lift Luo-Converters applying split capacitors

VIII. Simulation Results

To verify the design and calculation results, PSim simulation package was applied to these converters. We checked the Re-lift circuit with n = 2 and $\alpha = 2$. Choosing $V_{in} = 20$ V, $L_1 = L_2 = 10$ mH, all Capacitances are 2 μF and R = 30 kΩ, and using k = 0.5 and f = 50kHz.

A. Simulation results of a Re-lift circuit

We obtain the voltage values V_{in} and V_O of a Re-lift circuit (with n = 2 and $\alpha = 2$) to be 20 V and 320 V respectively. The simulation results are shown in Figure 14. The voltage values are matching on the calculated results.

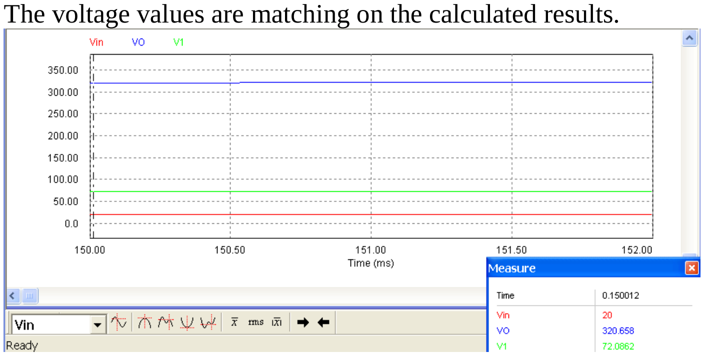


Figure 14. Simulation results of a Re-lift circuit

B. Simulation results of a Re-lift additional circuit

We obtain the voltage values V_{in} and V_O of a Re-lift additional circuit (with n = 2, $\alpha = 2$ and $\gamma = 2$) to be 20 V and 800 V respectively. The simulation results are shown in Figure 15. The voltage values are matching on the calculated results.

Figure 15. Simulation results of a Re-lift additional circuit

IX. Experimental Results

A test rig was constructed to verify the design and calculation results, and compare with PSim simulation results. We still choose $V_{in} = 20$ V, all inductances are 10 mH, all Capacitances are 2 μF and R = 30 kΩ. The duty cycle is k = 0.5 and f = 50kHz. The component of the switch is a MOSFET device IRF950 with the rates 1000V/5A/2MHz. We measured the values of the input and output voltages in following converters.

A. Experimental results of a Re-lift circuit

After carefully measuring a Re-Lift circuit (with n = 2 and $\alpha = 2$), we obtained the input voltage value of $V_{in} = 20$ V (shown in Channel 1 with 5.0 V/Div) and output voltage value of $V_O = 320$ V (shown in Channel 2 with 50 V/Div). The experimental results are shown in Fig. 16, which are identically matching on the calculated and simulation results, which are $V_{in} = 20$ V and $V_O = 320$ V shown in Fig. 14.

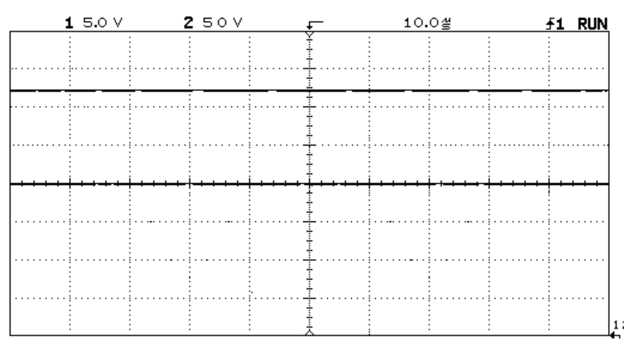


Figure 16. Experimental results of a Re-lift circuit

B. Experimental results of a Re-lift additional circuit

After carefully measuring a Re-Lift additional circuit (with n = 2, $\alpha = 2$ and $\gamma = 2$), we obtained the input voltage value of $V_{in} = 20$ V (shown in Channel 1 with 5.0 V/Div) and output voltage value of $V_O = 800$ V (shown in Channel 2 with 100

V/Div). The experimental results are shown in Fig. 17, which are identically matching on the calculated and simulation results, which are V_{in} = 20 V and V_O = 800 V shown in Fig. 15.

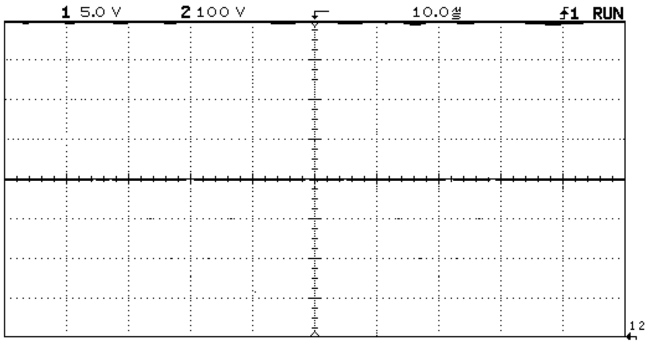


Figure 17. Experimental results of a Re-lift additional circuit

X. ACKNOWLEDGEMENT

This project is financially supported by the Intelligent Energy Distribution Systems project (No. 072133 0038), Agency for Science, Technology, and Research (A*STAR), Singapore is gratefully acknowledged. The author heartily acknowledge the financial support from the A*STAR (Singapore).

XI. CONCLUSION

A new method to enhance the voltage transfer gain of DC/DC converters – Split Capacitors applied in Positive Output Super-Lift Luo-Converters has been successfully created. It largely increases the voltage transfer gain in power series. Very high output voltage is easily obtained. Simulation and experimental results verified the design and calculations. This series Luo-Converters will be applied in industrial applications with very high output voltage.

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