Real-Time Simulation of Interleaved Converters with Decentralized Control

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Abstract. This paper presents a decentralized control algorithm for interleaved converters for high reliability application. In previous literature, a master control provides information on the system configuration in order to generate the different carriers. The whole premise of the proposed algorithm is that each module only communicates with its two immediate neighbors which reduce communication latency. Using only the neighbors proper interleaving of the carriers and balancing the converter leg currents is achieved. Carriers from each converter automatically adjust their phase, as modules are added or removed dynamically. Such implementation offers a completely decentralized control which makes it fully modular. Results of the controller are presented using a real-time simulator.

Key words

Real-time simulation, multilevel converter, decentralized control, interleaved converter, Control

1. Introduction

In the recent years, multilevel converters have been proven to be more efficient than classical converters. Multilevel converter offers lower total harmonic distortion (THD) and reduced stress on their components. Unfortunately, those gains often come at the cost of more complex control algorithm. Furthermore, if the number of modules varies during operation, due to faults or to increase efficiency, gains and controllers often need to be modified accordingly. In this paper, a decentralized control algorithm is proposed for converter using interleaved carriers [1, 2]. Interleaved carriers are widely used in multilevel converter, whether it is for multilevel voltage source converter (VSC) [2, 3]or multilevel current source converter (CSC) [4]. One argument for using multilevel converter is an increased reliability due to the redundancy of the modules. This implies that modules can be added or removed with little impact on the system.

When using interleaved carriers, this can only be done if the phase for each carrier is calculated according to the number of modules in the system. If this is not considered, harmonic are generated due to missing level in the converter output. Implementation of decentralized technique was proposed in [5-11] for analogic circuits. Carriers are interleaved using information from the carrier of its two immediate neighbors. In[6, 8], decentralized control is achieved by having each module observing the difference of the carrier waveform of its neighbors module and adjusting its own position is well suited for analog implementation using operational amplifier, but it might face difficulties when using digital signal processing (DSP) due to their lower bandwidth. In [11], a different analogic method is used. Carriers are interleaved using a geometrical approach. Each module observes the carriers of their neighbors, when the neighbor's carriers cross each other's, then the module changes the sign of the slope of its triangular carrier. Again, bandwidth plays an important role in the proper interleaving of the carriers. Furthermore, special cares must be taken during initialization of the slew rate otherwise all carriers converge to a constant value. The method proposed in this paper is inspired from the two methods previously mentioned. Using information from the neighbor modules, carriers are interleaved. All modules are connected in a ring, so that they all have two neighbors. If one module needs to be removed, it is only bypassed, ensuring that each module always have at least two different neighbors. A common modulation index is used for every module and is then modified locally to ensure proper current sharing.

This paper is divided as follows. In section II, the self-interleaving of the carriers is presented, as well as the key points of its numerical implementation. Generalized control algorithm for the newly proposed method is presented in section III. Section IV demonstrates application of the method in real-time simulation for a boost converter using six interleaved modules. Simulation

results during initialization, steady-state, and step response are also presented. Finally conclusion is presented in section V.

2. Self-interleaving carriers

The main interest of this new method is its modularity and its decentralization. Each modules works toward the same goal, but only information from the immediate neighbor is available. In this particular application, knowing phase of the carrier of its neighbor, θ_{n-1} and θ_{n+1}, the phase for the nth module, θ_n, can be determined. This is done through an iterative process where θ_n is corrected in regard to θ_{n-1}. The angular distance between the module and its two neighbors, $\Delta\theta_{n-1}$ and $\Delta\theta_{n+1}$, should be the same. Fig. 1 shows how θ_n^k is corrected to obtained θ_n^{k+1}.

At iteration k, θ_n^k is represented by dash lines, where $\Delta\theta_{n-1}^k$ and $\Delta\theta_{n+1}^k$ are very different. At iteration k+1, represented by solid line, θ_n^{k+1} has been reposition in regard to θ_{n-1}^k. This is achieved by computing the average value between the two
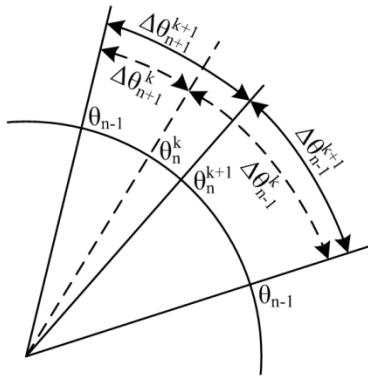

Fig. 1 Iterative computing of θ_n.

angular distances, and θ_n is reposition relatively to θ_{n-1}, shown in (1).

$$\theta_n^{k+1} = \theta_{n-1}^k + \overbrace{\frac{\theta_{n-1}^k - \theta_{n+1}^k}{2}}^{\Delta\theta_{n-1}^{k+1}} \quad (1)$$

If θ_{n-1} and θ_{n+1} have reached their final value, θ_n final value is instantaneously reached too. Naturally, final values can only be reached after a few iterations since θ_{n-1} is computed based on θ_{n-2} and θ_n, and so on. Furthermore, this method will only converge if phase for at least one module is fixed. The computed phase for each module is then used to change the index of a table where the carrier is stored, as it will be discussed in the next section.

A. Numerical implementation

This method is meant to be implemented in hardware with limited resources, and therefore should be efficiently implemented. Fig. 2 shows the schematic of this implementation.
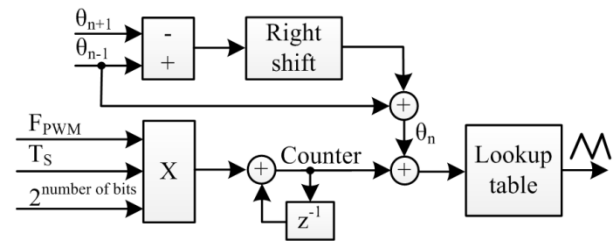

Fig. 2 Schematic for carrier generation.

This is a very classic method to generate signal within digital signal processing (DSP) or in field programmable gate array (FPGA). Output of a lookup table is updated using a counter. Adding a value to this counter is translated into a phase shift of the signal generated by the lookup table. Modifying the increment of the counter changes the frequency of such signal. In order to implement this design, the first thing to consider is the depth of the lookup table where the carrier will be store. This not only determines the minimum angle between two interleaved carriers but also the accuracy of the pulse width modulation (PWM). Using a maximum of 12 bits, a precision of 0.0879° is obtained, as shown by the equation (2).

$$\Delta\theta_{min} = \frac{360°}{2^{number\ of\ bits}} = \frac{360°}{4096} = \mathbf{0.0879°} \quad (2)$$

Using a fixed-point representation for the angle has a great advantage; once it reaches its maximum value, it will return naturally to 0. Just like angle, that returns to 0° once it reaches 360°. Furthermore, the operation required to compute (1) can now be reduced to one subtraction, shifting the result once to the right, dividing it by 2, and one more addition. Finally, for all these operations, overflows are tolerated as they are the appropriate behavior when dealing with angles.

Increment of the counter is determined by the desired carrier frequency, the time-step of the system, and the depth of the lookup table. This expression is given by (3).

$$Increment = F_{PWM} \times T_S \times 2^{number\ of\ bits} \quad (3)$$

Where FPWM is the carrier frequency and TS is the time-step of the system. The minimum frequency is reach when the value of Increment in (3) is equal to 1. Because of clock uncertainty, the module doing the counter should be centralized, and count value is passed down to each module, like the modulation index is. This is presented in the following section.

3. Control algorithm

The main objective of this paper is the decentralization of the controller. Therefore, interaction between the modules and the main controller, or master module, should be kept to a minimum. Fig. 3 a) shows the block diagram of master module and Fig. 3 b) the one for the other modules.
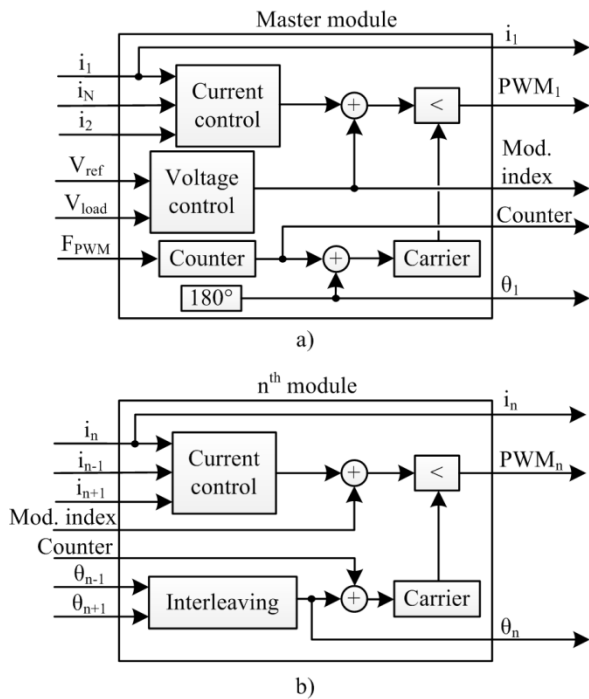
Fig. 3 Block diagram of control a) for the master b) for every other modules.

The master module is in charge of generating the common modulation index and the counter value. The common modulation index is obtained using a PI controller to regulate the load voltage to its reference voltage. As for current control, it is regulated based on the value of its neighbor module, the 2nd and the Nth. Its current as well as its phase is communicated to its neighbor. All the modules are connected in a ring, sharing the phase of their carrier and the current resulting from their modulation index two their two neighbors. Even though the same modulation index is used for all modules, the resulting current can varies due to circuit disparities (different leaking inductance, different conducting losses etc.). For this reason, each module applies a correction to the common modulation index. This controller is shown in Fig. 4.
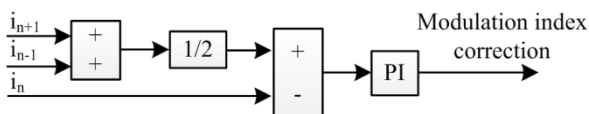

Fig. 4 Decentralized current control.

The current reference is obtained by calculating the instantaneous average value of the current from the two neighbor modules. The error between this reference and the current of the module is sent to a PI controller. The output of the PI controller is added to the common modulation index, which is then compared with the self-interleaved carrier to generate the PWM for one of the converter. Dynamic and stability of the controller is demonstrated using real-time simulation.

4. Real-time simulation results

A six-leg interleaved boost converter is used to demonstrate the proposed control [12, 13]. Such converter offers high efficiency in DC/DC application. Simulation

results were obtained using real-time simulator from OPAL-RT technologies Inc. The controller and the communication for each module was simulated using Intel microprocessors (CPU) with a sampling rate of 20µs. PWM was also generated on CPU using interpolation technique, from RT-EVENT, allowing to generate switching event within a sampling rate. Finally the converter is simulated using FPGA, with eHS from OPAL-RT [14, 15], with a simulation time-step of 200ns. Simulated circuit is shown in Fig. 5 and circuit parameters are given in table I.

TABLE I CIRCUIT PARAMETERS

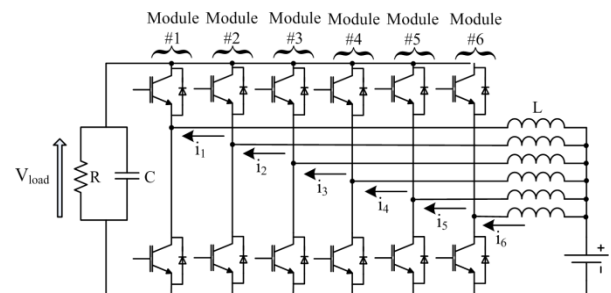| Rated power	1	MW
Rated voltage	1	kV
Conducting losses	1	mΩ
Line inductance (L)	500	nH
Load capacitor (C)	640	µF
Load resistance (R)	1	Ω
Carrier frequency	8	kHz
Simulation time-step	200	ns

Fig. 5 Converter schematic.

A. Self-aligning carriers

One of the advantages of the proposed method is in the self-aligning carriers. The behaviour of the method is demonstrated in Fig. 6.In Fig. 6, the initialization of the method is shown for 3, 6 and 21 carriers. θ_1 is always forced to 180° and the other phases rapidly converge toward their steady-state. The number of iterations required to reach steady state is only dependent of the number of carriers. For 3 carriers, steady-state is reached in 6 iterations. It takes 9 and 121 iteration respectively for 6 and 21 carriers. Naturally, more carriers require more time to reach steady-state. Nonetheless, this is part of the initialization of the system, and PWM should only be applied once steady-state is reached. Cases where carriers are removed and added to the system is shown in Fig. 7

As it is shown in Fig. 7, when adding or removing carriers, steady-state is rapidly achieved.
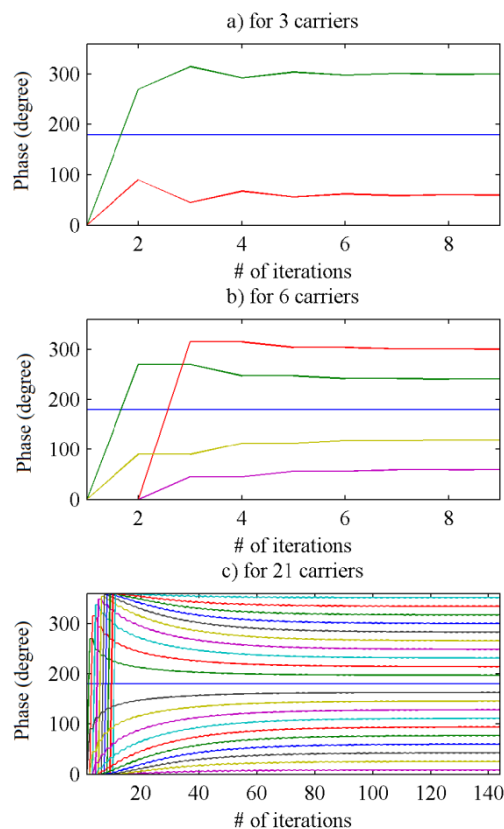
a) for 3 carriers

b) for 6 carriers

c) for 21 carriers

Fig. 6 Settleling time for a) 3 carriers b) 6 carriers c) 21 carriers.
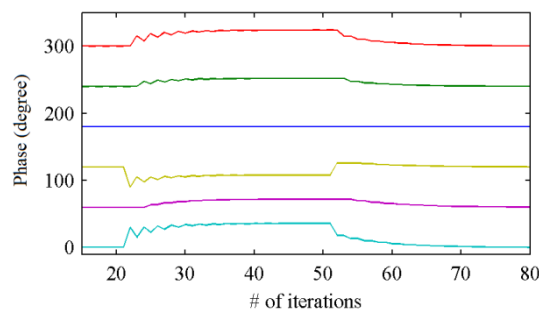

Fig. 7 Going from 6 carriers to 5, and from 5 back to 6.

B. Converter initialization

In this test, the converter is start-up without any prior initialization. This demonstrates controller stability under harsh condition. Note that carriers are not yet interleaved at start-up, but since only 6 carriers are used, with a simulation time-step of 20µs, it only require a total of 180µs to achieve steady-state, which has little impact on the overall initialization. Fig. 8 a) shows the six current, which are perfectly interleaved and Fig. 8 b) shows the load voltage.

Steady-state is reached in a 10 ms, load voltage is regulated and all six current have the same amplitude, ensuring proper power dissipation. This can be observed more closely in Fig. 9 for the 6 currents in steady-state.
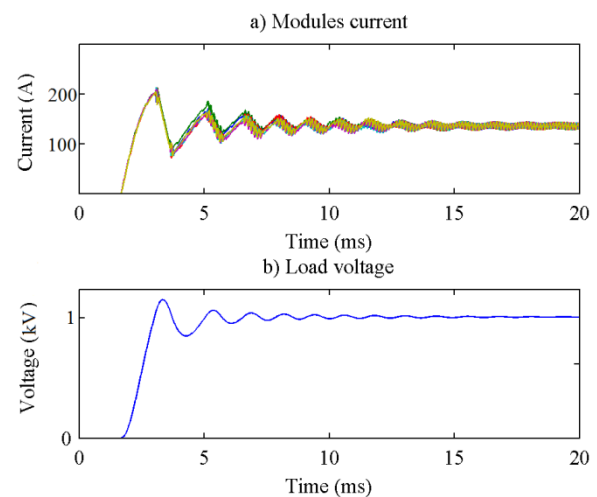

a) Modules current

b) Load voltage

Fig. 8 Initialization of the converter a) current modules b) load voltage.

By measuring the time between the peak values of two currents in Fig. 9, we can ensure that the carriers are properly interleaved; with a frequency of 8kHz, using 6 carriers, there should be a time interval of 20.833µs. Since the controller has a sampling time of 20µs, current should be sampled at a faster rate to observe this phenomena. OPAL-RT simulator offers an 8 channel oscilloscope to monitor simulation executed on FPGA. A sampling rate on 200ns was used for Fig. 9.
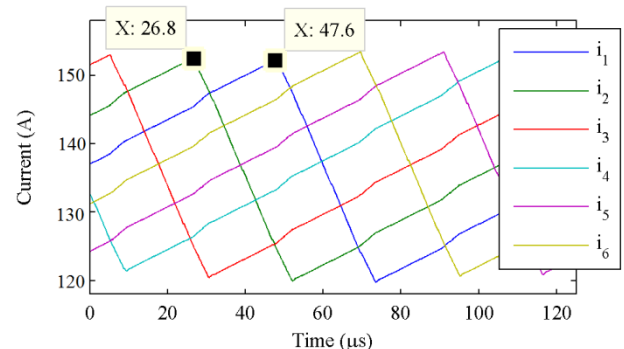

Fig. 9 Zoom on modules current in steady-state.

C. Current regulation

To show the impact of the current controller in each module, a variation of 10% is applied to the conducting losses and inductances of the converter. In Fig. 10, current control is deactivated until 50ms and is then turned ON.
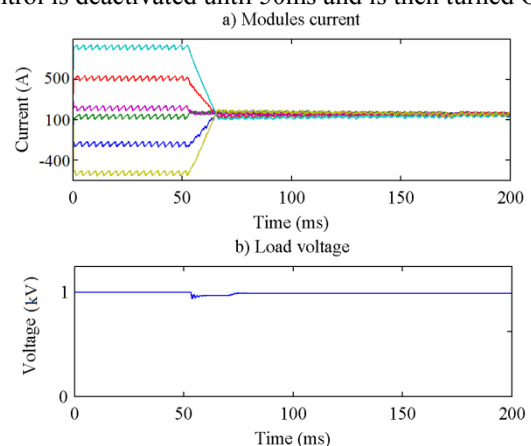

a) Modules current

b) Load voltage

Fig. 10 Effect of current control

In the case where all components are ideal, current control algorithm would not be required. But by adding a variation to the different components, we make sure of the right behaviour of the current control loop.

D. Reference step

In this test the output reference is step-up from 1kV to 1.2kV in Fig. 11 and it is then step-down from 1.2kV back to 1kV in Fig. 12.In both cases, desired reference is achieved.
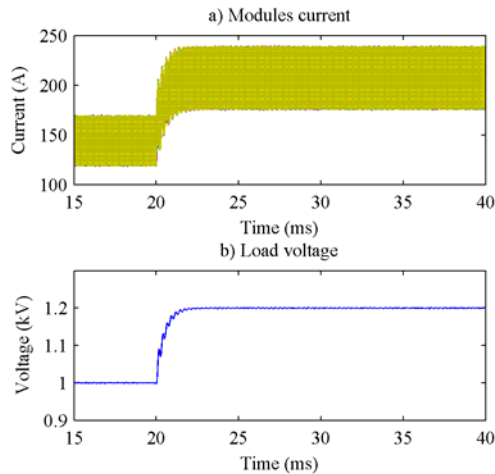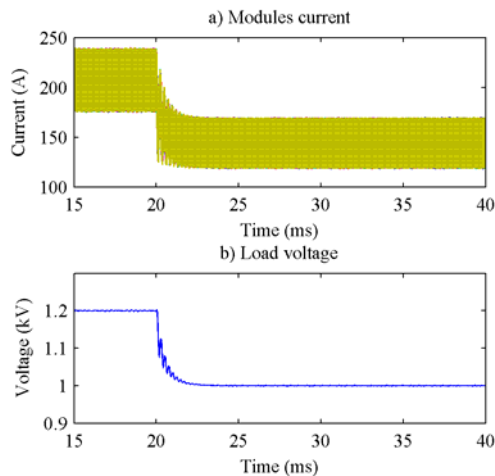

Fig. 11 Reference step-up.

Fig. 12 Reference step-down.

E. Module step

This time, one module is removed and then one module is reintroduced. Fig. 13 shows the different carriers being rearranged when one module is removed.
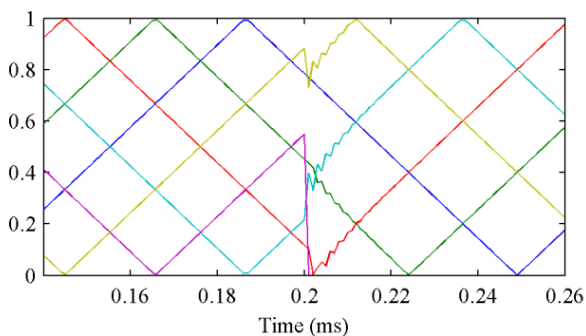

Fig. 13 Carriers reorganisation from 6 to 5.

Voltage regulation is now achieved using only 5 modules. When carriers are removed, a step-up on the current is observed like in Fig. 14 a). This has little to no impact on the voltage output, shown in Fig. 14 b)
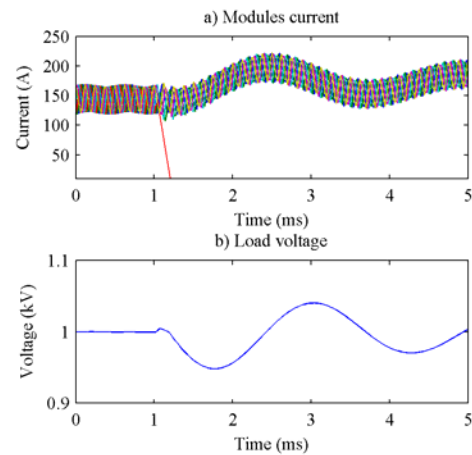

Fig. 14 Impact of removing one module for a) the modules current b) the load voltage.

Likewise, a step-down on the current is observed when a module is reintroduced while no variation is observed on output voltage, Fig. 15 a) and b) respectively.
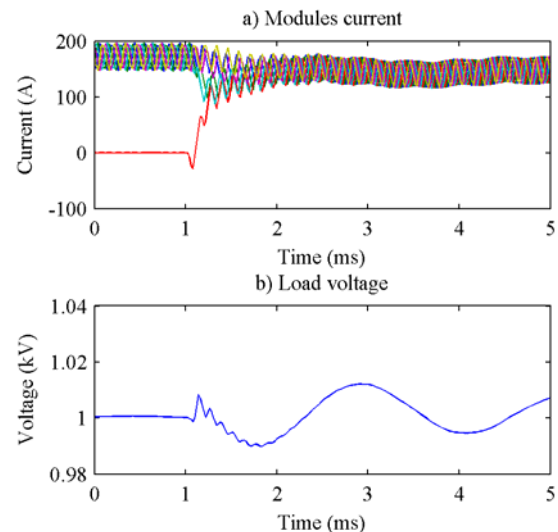

Fig. 15 Impact of reintroducing a module for a) the modules current b) the load voltage.

We can notice that when a module is removed, the currents stay more grouped than when the module is reintroduced. This is because the reference for each module is obtained by the average of its neighbor. When reintroducing a module, its current is zero, which pulls on its neighbor.

F. Load step

In this final test, a step is applied to the load; it varies from 2Ω to 1Ω.
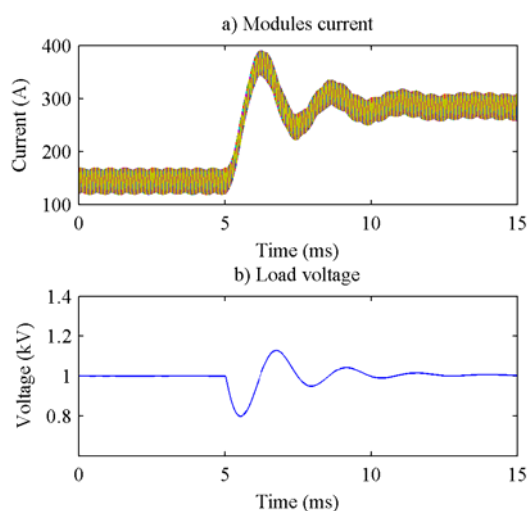
Fig. 16 Impact of a load variation on the a) modules current b) load voltage.

Once again no major variations are observed on the currents and voltage, as shown in Fig. 16. The voltage drop observed is due to the controller reaction time. It takes 2.5ms for the controller to compensate the drop. Considering a sampling time of 20μs, the reaction time is well within expectation.

5. Conclusion

In this paper, a numerical implementation of a decentralize control self-interleaving carriers was presented. Details of the implementation were given, and the key aspects were pointed out. Decentralized current control was also presented and its importance has been demonstrated using real-time simulation. Various test cases were done to demonstrate the performance of the proposed control algorithm. The use of real-time simulation proved that the proposed algorithm could easily implement in real-application. Finally, using sub-microsecond sampling time, high accuracy of interleaving the carriers was shown using the current. In future work, the decentralized control will be implemented in many small DSP, with each of them interfaced with the real-time simulator in order to verify the communication protocol before using it on the real converter.

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