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Three-Phase Transformerless Inverter for Photovoltaic Grid Connected System with Zero Common Mode Noise

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Abstract. The pervasion of transformerless grid connected photovoltaic (PV) inverters has triggered the concerns of many researchers since it can induce power quality problems. In these types of applications, the generation of common mode (CM) leakage current is one of the major factors that affects the reliability of the overall design. In single-phase systems, the concept of the common ground between the PV negative terminal and the neutral point of the grid is the only topology that "totally" cancels this CM noise. However, none of the existing three-phase inverter techniques is able to totally remove it. Therefore, this paper proposes a three-phase PV inverter based on the concept applied in the single-phase system in order to achieve, for the first time, a zero CM noise in three-phase grid-connected PV applications. The proposed inverter is simulated with a PV array, appropriate modulation technique, corresponding inverter controller, and a three-phase Y-connected alternating current (AC) grid voltage. The simulation of the overall system is done using Matlab/Simulink software. As compared with results of existing three-phase topologies, this is the only three-phase transformerless PV inverter technique that offers generation of multilevel output, total elimination of leakage current flow, simple inverter structure, and uncomplicated modulation technique.

Key words. Common Mode Noise, Leakage Current, Power Quality, Tranformerless Photovoltaic Inverter.

1. Introduction

One of the major factors that affects the performance of the grid-connected PV systems is the generation of CM noise. Being a power quality issue that can perturb the reliability of the PV systems, the problem of CM noise must be investigated carefully especially in a world where integrity is necessary.

Grid-connected PV inverters are used as a connection point between the PV source and the grid. They are divided into two categories: inverters with/without isolation. The galvanic isolation is provided by either an enormous line frequency (LF) transformer in the AC part or a high-frequency transformer in the direct current (DC) part. However, these isolation transformers are immense and difficult to implement. In addition, they add extra losses to the system, which cause the overall efficiency to decrease [1]. Therefore, the need of reducing the PV inverter cost, increasing its efficiency, and minimizing its complexity, sheds light on the importance of the transformerless PV inverter [2]. Despite the several advantages of transformerless inverters, the absence of the source of isolation (i.e. transformer) causes the generation of a CM leakage current, which flows through the parasitic capacitance of the PV panel [3]. This undesirable CM noise can add losses to the system, cause electromagnetic interference (EMI), increase the output harmonics, and lead to safety problems [4].

The level of leakage current varies according to the selected inverter topology and its appropriate modulation technique. In single-phase system, three different methods can address the issue of the CM noise [5]:

1) Decoupling the PV side from the grid side
2) Clamping the middle point of the splitting DC capacitors
3) Attaching the neutral point of the grid and the negative terminal of the PV source to a common ground

The H-bridge single-phase topology was modified gradually from H5 and HERIC versions using the first method, to the full bridge DC bypass (FB-DCBP) model based on both the first and the second methods. This topology succeeded in lowering the level of leakage current to an acceptable value, however, it led to high conduction losses, extra switches, and a higher inverter cost [2], [5], [6], [7]. The neutral point clamped (NPC) single-phase topology has two modified versions: the active NPC (ANPC) and the Conergy NPC. Based on the second method, this topology and its modified versions were able to suppress the CM leakage current to a very low level, however, they require higher input DC-link voltage [8], [9], [10], [11]. As for the single-phase topology based on the virtual DC bus concept, it was able to totally delete the CM noise by applying the method used in the third way. However, this topology is not suitable for high power applications because very high levels of current stress can

be added to the system under certain conditions [12]. Relying on the concept applied in the virtual DC bus topology, A. Kadam & A. Shukla propose in a multilevel half bridge topology that is also able to totally suppress the CM noise in addition to the capability of producing a multilevel output [13].

On the other hand, many three-phase inverter topologies were provided to solve the problem of the CM leakage current in a three-phase system such as: three-phase full bridge (FB) topology [3], [14], three-phase FB with split capacitor (3FB-SC) topology [14], three-phase FB with one extra switch either in the upper or lower part [15], H8 three-phase topology [16], three-phase NPC topology [14], three-phase cascaded H4 topology [17], [18], three-phase cascaded H5 topology [17], [18], and the three-phase embedded-switch inverter (ESI) topology [19]. These topologies were modified and developed by adjusting either the inverter structure or the modulation technique. A summary of the aforementioned topologies with their resultant level of leakage current is shown in Table I.

Table I. - Single-Phase and Three-Phase Topologies with their Corresponding Leakage Current Level

Single-Phase Topologies	Leakage Current Level	Three-Phase Topologies	Leakage Current Level
H5	Low	3-phase FB	Very High
HERIC	Low	3-phase FBSC	Very Low
FB-DCBP	Very Low	3-phase FB (with extra switch)	Low
NPC	Very Low	3-phase H8	Low
ANPC	Very Low	3-phase NPC	Very Low
Conergy NPC	Very Low	3-phase cascaded H4	Very High
Virtual DC bus	Zero	3-phase cascaded H5	Very Low
Multilevel half bridge	Zero	3-phase ESI	Low

None of the existing three-phase topologies was able to "completely" remove this CM noise. Therefore, this paper aims to benefit from the outcome of the successful topology in a single-phase system and extend it in a way to be applied upon a three-phase system.

This paper analyses and explains in details the proposed three-phase transformerless inverter operating in two different modes. A theoretical analysis is given in order to prove how this three-phase topology is able to totally remove the CM noise. The proposed inverter is simulated with a PV array, appropriate modulation technique, corresponding inverter controller, and a three-phase Y-connected AC grid voltage. The case of a three-level inverter is examined in order to verify the topology's capability of generating a multilevel output voltage. Finally, the simulation results are presented to validate the correct performance of the proposed topology and confirm the goal of this paper in removing completely the CM noise in a three-phase system.

2. Identification of CM Noise in Transformerless PV Inverter

The CM noise is a type of EMI. It represents the flow of leakage current from a high $\frac{dv}{dt}$ node to the ground through the parasitic capacitance [20]. For evaluating the leakage current issue, it is important to differentiate the concepts of common mode to differential mode.

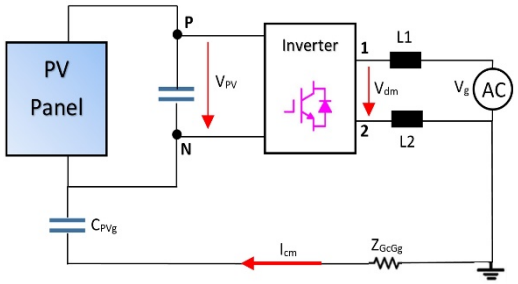

Fig.1. Model of a single-phase transformerless PV inverter

Fig. 1 shows a general model of a single-phase transformerless PV inverter system where the following parameters are taken into consideration:

1) C_{PVg}: stray capacitance
2) Z_{GcGg}: series impedance between C_{PVg} and ground
3) L_1 *and* L_2: form the line inductor
4) V_{PV}: voltage of the PV source
5) V_g: voltage of the grid
6) I_{cm}: common-mode current
7) V_{dm}: differential-mode voltage

Given any circuit, the common mode voltage is defined as the average of the voltages from each output terminal to a common reference [21]. For the system in Fig. 1 it is suitable to choose the common reference at terminal N, which is the negative terminal of the PV array. Thus, the inverter CM voltage is as follows:

$$v_{cm} = \frac{v_{1N}+v_{2N}}{2} \quad (1)$$

The voltage across the output terminals of the inverter is characterized by the differential mode voltage as follows:

$$v_{dm} = v_{1N} - v_{2N} \quad (2)$$

The additional CM voltage is derived from v_{dm} as follows:

$$v_{d-to-c} = v_{dm} \cdot \frac{L_2-L_1}{2(L_2+L_1)} = (v_{1N} - v_{2N}) \frac{L_2-L_1}{2(L_2+L_1)} \quad (3)$$

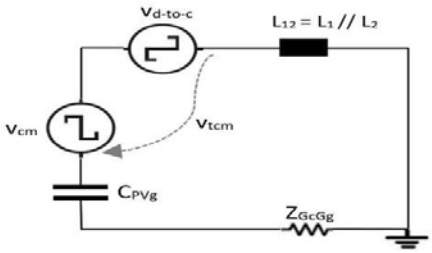

Fig.2. Equivalent CM circuit of a transformerless PV inverter

As shown in Fig. 2, the total CM voltage is obtained as follows:

$$v_{tcm} = v_{d-to-c} + v_{cm}$$
$$= (v_{1N} - v_{2N})\frac{L_2 - L_1}{2(L_2 + L_1)} + \frac{v_{1N} + v_{2N}}{2} \quad (4)$$

The total CM voltage must be kept constant without variation in order to block the generation of leakage current. Relying on the circuit in Fig. 2, it is obvious to conclude that one of the following two conditions must be satisfied in order to remove the leakage current [6]:

1) *Case of* symmetrical *inductor layout* $L_1 = L_2$: having a zero value of v_{d-to-c}, v_{cm} must kept constant in order to have a constant value of the total CM voltage v_{tcm}.
2) *Case of asymmetrical inductor layout* $L_1 \neq L_2$: parameters of the circuit should be chosen in an appropriate way to assure that the sum of v_{cm} and v_{d-to-c} (v_{tcm}) is constant.

3. Elimination of CM Noise in the Proposed Three-phase Transformerless Inverter Topology

Based on the multilevel half bridge topology presented in [13], a three-phase inverter is proposed in this paper, as shown in Fig. 3.

Three single-phase inverters of the multilevel half bridge topology are connected in a way to operate as a three-phase system. Based on the successful concept applied in a single-phase system, the negative point of the PV panel is directly attached to the neutral node of the Y-connected three-phase grid voltages. Benefiting from this successful concept, this three-phase proposed topology is the first one that is able to "*totally*" cancel the CM noise caused by the flow of leakage current. This idea can be proven graphically and theoretically. Of note, the CM noise is studied separately in each phase similarly to the case of a single phase inverter.

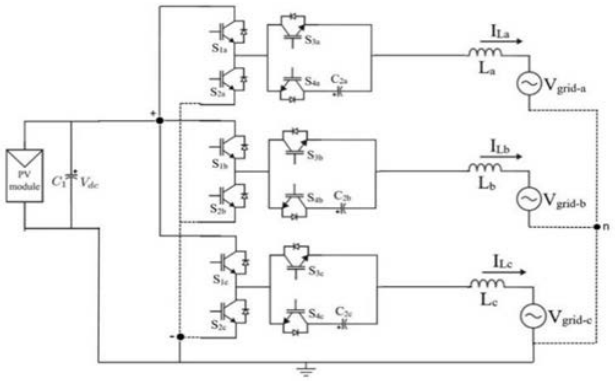

Fig.3. Proposed three-phase transformerless inverter

A. *Graphically*

Referring to the general CM circuit of a single-phase transformerless PV inverter shown in Fig. 1, it can be graphically proven that the stray capacitance is bypassed by directly attaching the PV negative node to the neutral node of the grid as illustrated in Fig. 4.

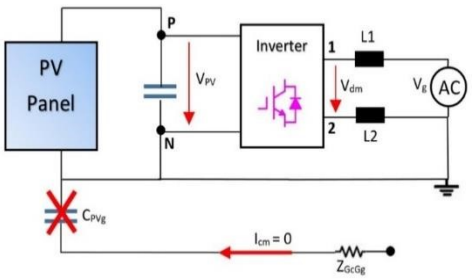

Fig.4. Bypassing the stray capacitance with the selected topology

B. *Theoretically*

The cancelation of leakage current can be also proved theoretically by showing that the total CM voltage is removed. In this proposed topology, the inverter has an asymmetrical inductor distribution where L_2 is equal to zero leading to a null voltage at terminal 2 (V_{2N} = 0). Consequently, the following equations are obtained:

$$v_{cm} = \frac{v_{1N} + v_{2N}}{2} = \frac{v_{1N}}{2} \quad (5)$$

$$v_{d-to-c} = (v_{1N} - v_{2N})\frac{L_2 - L_1}{2(L_2 + L_1)} = -\frac{v_{1N}}{2} \quad (6)$$

$$v_{tcm} = v_{cm} + v_{d-to-c} = \frac{v_{1N}}{2} - \frac{v_{1N}}{2} = 0 \quad (7)$$

Therefore, the leakage current is totally canceled since no variations will occur in this zero total CM voltage.

4. Mode of Operation of the Proposed Three-Phase Topology

The proposed three-phase topology shown in Fig. 3 consists of three single-phase inverters. Each phase is controlled separately in a way to have an overall system that functions as a three-phase inverter. The operation mode is the same in each phase except that there is a 120-degree angle shift between each of them. Therefore, for simplicity reasons, the mode of operation is studied in this paper in one of the phases and then can be similarly applied for the others.

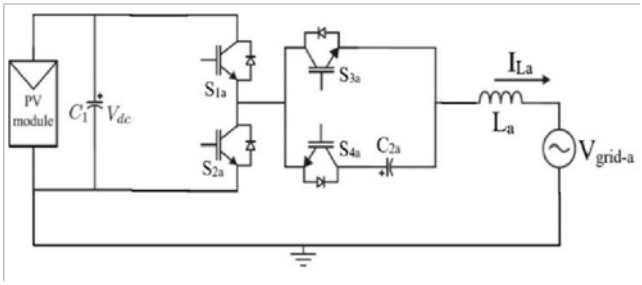

Fig.5. Phase "a" structure of the three-phase proposed topology

Before further proceeding, it is worth noting that this paper analyses the case of a three-level inverter of this multilevel topology. As shown in Fig. 5, the inverter in phase "a" consists of two parts:

1) S_{1a}, S_{2a} and C_1 forming the first half bridge
2) S_{3a}, S_{4a} and C_{2a} forming the second half bridge

Similar to the single-phase system explained in [13], this three-level proposed topology can work in two modes:

1) *Mode 1*: C_{2a} is charged to half of the value of the DC input voltage ($\frac{Vdc}{2}$)

2) *Mode 2*: C_{2a} is charged to the same value of the DC input voltage (V_{dc})

Based on the estimation done in [13], the value of the module capacitor in each phase can be evaluated by applying a few steps. The equation of the output average power is expressed as follows:

$$P(t) = \sqrt{2}V_{grid}\, sin(wt + \Theta_v)\, \sqrt{2}I_{grid} sin(wt + \Theta_i) \quad (8)$$

Where $P(t)$ is the average output power, V_{grid} is the grid voltage, I_{grid} is the grid current, w is the grid frequency in rad/s, Θ_v is the grid voltage phase angle, and Θ_i is the grid current phase angle. After doing some trigonometric substitutions, the following power equation is obtained:

$$P(t) = P_{PV}.[cos(\Theta_v - \Theta_i) - cos(2wt + \Theta_v + \Theta_i)]$$
$$= P_{PV}.[cos(\Theta) - cos(2wt + \Theta_v + \Theta_i)] \quad (9)$$

Where P_{PV} is the power of the PV array and θ is the phase shift between the voltage and current. The integral of the power equation given in (9) gives the stored energy in the module capacitor over a half cycle as follows:

$$\int_0^{\frac{1}{2f}} P(t)dt = \frac{1}{2f}.P_{PV}.cos(\Theta)$$
$$= \frac{1}{2}C(u_{max} - u_{min}) = Cu\delta u \quad (10)$$

Where f is the grid frequency, C is the module capacitance, u is the nominal voltage of C, and δu is the voltage ripple of C. In equation (10), the second term of the integral is neglected because it does not affect the voltage ripple. After equating the equations in (10), the formula of the module capacitor is obtained:

$$C = \frac{P_{PV}cos(\Theta)}{2fu\delta u} \quad (11)$$

A. First Mode

Charging C_{2a} to half of the value of the DC input voltage leads to three-level output voltage: $\frac{Vdc}{2}$, $-\frac{Vdc}{2}$ and 0. The corresponding switching states are shown in Table II.

Table II. - Switching States of the Inverter Operating in Mode 1

S1	S2	S3	S4	V_0
1	0	0	1	$\frac{Vdc}{2}$
0	1	0	1	$-\frac{Vdc}{2}$
0	1	1	0	0

B. Second Mode

In this mode, the voltage rating of the power switches is halved because C_{2a} is charged to the same value of the DC voltage leading to a three-level output voltage as follows: V_{dc}, $-V_{dc}$ and 0. The corresponding switching states are shown in Table III.

Table III. - Switching States of the Inverter Operating in Mode 2

S1	S2	S3	S4	V_0
1	0	1	0	V_{dc}
1	0	0	1	0
0	1	1	0	0
0	1	0	1	$-V_{dc}$

5. Simulation and Results

Matlab/Simulink software is used to simulate the proposed grid connected three-phase transformerless PV inverter due to many reasons: it has wide and variant tool boxes in grid-connected PV applications, helps simulate different maximum power point tracking (MPPT) algorithms, allows to monitor and control any inverter unit, and can plot any needed data. To validate the functionality of the proposed topology, the three-phase inverter shown in Fig. 3 is simulated in Matlab/Simulink with a PV array, grid AC voltage sources connected in Y-connection, and an inverter controller.

The PV array was used as an input DC voltage. Trina Solar TSM-250PA05.08 was the chosen PV module in Simulink. In order to work correctly, the PV panel must be fed by two inputs: the irradiance (W/m^2) and the temperature ($_0C$) as illustrated in Fig. 6. The PV array was selected to operate at a temperature equal to 25 ^{0}C.

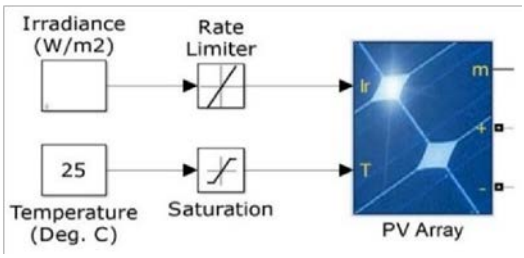

Fig.6. PV array structure in Matlab/Simulink

As for the inverter controller, it includes MPPT block, a DC voltage regulator, a current controller, and a phase-locked loop (PLL) block.

The MPPT controller balances the grid requirements and the power supplied by the PV panels. It allows the PV panel to operate at an appropriate voltage level in order to maintain maximum power transfer at different atmospheric situations. In this paper, the incremental conductance (IC) technique was utilized due to its simplicity and ability to track the MPP without the need of complex techniques based on neural networks [22].

The control part of the inverter is based on the synchronous Park's transformation [23]. A proportional integral (PI) controller is usually used with this type of control due to its satisfactory performance. The transfer function of the PI controller is given as follows:

$$G_{PI} = K_p + \frac{K_i}{s} \quad (12)$$

Where K_p and K_i represents the proportional and integral gains respectively.

During the simulation, this inverter controller generates three voltage references. Each phase has its own pulse width modulation (PWM) block which is fed by the appropriate reference signal generated from the inverter controller.

The generated reference signals are shifted by 120 degree with respect to each other. In that way, three-phase balanced grid voltages will be obtained. As discussed in [13], the PWM technique differs between mode 1 and mode 2. In mode 1, the conventional sine PWM (SPWM) technique is applied to generate the switching gate pulses in each phase. In mode 2, a control strategy given in [13] is applied in each phase individually in order to generate the appropriate switching gate pulses.

After setting up the overall model shown in Fig. 3, selecting the suitable value for the module capacitors, choosing the best MPPT technique for this system, tuning the inverter controller in an effective way, and adding the appropriate modulation techniques, the system is ready to be simulated and evaluated in both mode 1 and mode 2.

A. First Mode

In mode 1, the PV array has a DC input value of 400V and the capacitor C_2 is charged to half of the DC voltage (i.e. 200V) in each phase. The plots of the output voltage V_0 and the voltage across capacitor V_{C2} are generated for each phase (a, b and c) using the scope blocks in Matlab/Simulink.

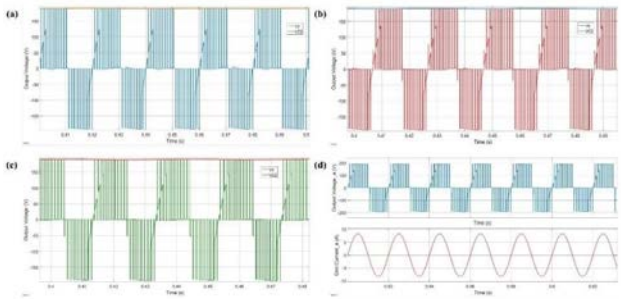

Fig.7. Output voltage and voltage across capacitor C2 in mode 1 (a) phase a, (b) phase b, (c) phase c; (d) Output voltage and grid current in phase a (mode 1)

A three-level output voltage is generated in each phase varying between: 200V, 0V, and -200V. The output voltage V_0 depends on the voltage across C_2 which is naturally balanced. In other words, the highest output voltage that can be reached is equal to $\frac{V_{dc}}{2} = \frac{400}{2} = 200$V which is the voltage across C_2. Thus, the results of the output voltage and the voltage across capacitor C_2 of each phase shown in Fig. 7 (a), (b) and (c) validate the theoretical reasoning done in section 4 regarding the mode of operation of this proposed three-phase inverter. Note that when the inverter is operating in mode 1, it acts similarly to the NPC inverter, which is a half-bridge topology. Acting as a half-bridge inverter, this topology when operating in mode 1 requires an input DC voltage, which is the double of that across C_2. Thus, the voltages of the power switches will require higher ratings leading to an increase in the cost of the inverter.

The inverter of this PV system is operating at unity power factor (UPF) (i.e. no injection of reactive power). The UPF operation is done by tuning the inverter controller in a way that allows the reference current to be synchronized with that of the grid. Being controlled separately, each grid current is synchronized with its corresponding output phase voltage as shown in Fig. 7 (d). This result is the same way validated for phase "b" and "c".

B. Second Mode

In mode 2, the PV array has a DC input value of 200V and the capacitor C_2 in each phase is charged to the same value of the DC voltage (i.e. 200V). The plots of the output voltage V_0 and the voltage across capacitor V_{C2} in phase "b" are shown in Fig. 8 (a).

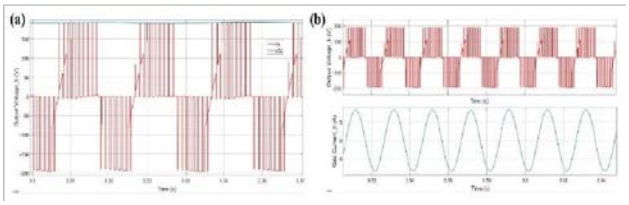

Fig.8. (a) Output voltage and voltage across capacitor C_2 in phase b (mode 2); (b) Output voltage and grid current in phase b (mode 2)

A three-level output voltage is generated in each phase varying between: 200V, 0V, and -200V. The output voltage V_0 also depends on the voltage across C_2, which is not naturally balanced in this case. As shown in Table III, there exist two switching states that lead to a zero output voltage. In the first zero state, S_1 and S_4 are turned ON to charge the capacitor C_2. In the second zero state, S_2 and S_3 are turned ON to conserve the net charge of the bypassed capacitor C_2. In this way, the capacitor becomes balanced.

Similarly to mode 1, the inverter is also operating at UPF in mode 2 as illustrated in Fig. 8 (b) where the output phase "b" voltage is synchronized with the grid current.

Note that the results in Fig. 8 (a) and (b) are the same way validated for the other remaining phases "a" and "c"; the only difference is that they are delayed by 120 degrees with respect to each other (i.e. balanced output voltage).

6. Conclusion

Comparing to others existing three-phase transformerless inverter topologies, the method presented in this paper is the first one that is able to ensure a "zero" CM noise in a three-phase system. The PV panel, the three-phase proposed inverter, the selected modulation technique, the inverter controller and the three-phase Y-connected AC grid voltage were connected together and simulated in the two different operation modes of the inverter. As compared with the results of existing techniques, this proposed inverter can be considered as a promising topology in three-phase applications since it shows satisfactory performance, has simple inverter structure, can generate multilevel

output, implements simple modulation technique and is the only three-phase topology that ensures a total elimination of the leakage current flow.

Future work can consider the assessment of losses and efficiency of this proposed inverter. These two criteria can be evaluated in terms of conduction losses, switching losses, and levels of stress on switches. Moreover, this presented topology can be tested in the laboratory on a hardware prototype in order to further validate its functionality and performance.

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