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Compensation of Voltage Harmonics for LCL-filtered Inverters in Islanded Microgrids

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Abstract. In a microgrid (MG), it is possible to have some sensitive loads that require high voltage quality. In this paper, a new technique is proposed for selective compensation of main voltage harmonics in islanded MGs. The proposed technique is capable of adjusting the compensation percentage in proportion with the existing disturbance in the sensitive load bus (SLB) and sharing the compensation workload among DGs in proportion with their nominal power. This compensation, is performed by controlling of the interface inverters of distributed generation (DG) units with LCL filters. Also, to decrease the asymmetry among phase impedances of MG and mitigate the voltage distortion after the output LCL of filters, a novel structure is proposed to generate selective virtual impedance. At fundamental frequency, the proposed structure of the virtual impedance improves the control of the fundamental component. On the ather hand, at main harmonic frequencies, it tries to adaptively improve nonlinear load sharing among DG units and mitigate the voltage distortion after the output LCL filters. Simulation results in MATLAB/SIMULINK environment show the efficiency of the proposed approach in improving load load sharing and decreasing voltage harmonics.

Key words

Distributed generation, Microgrid, Load sharing, Voltage harmonics compensation.

1. Introduction

A microgrid (MG) is defined as a controllable network which comprises distributed generation (DG) units, energy storage systems, and distributed loads. An MG can be used in two modes: connected to or independent of the main grid (islanded) [1]. The huge increase in utilizing nonlinear loads at distribution voltage levels has made the voltage and current harmonics a usual power quality problem in MGs. These kinds of problems might have unacceptable effects such as interruption in the operation of adjustable speed drives (ASDs) and protective relays, motors and the overheating of transformers, and improper functioning of power factor correction capacitors [2].

In the control system of each DG, there exist controllers of fundamental component of the power, along with controllers of current, voltage, and virtual impedance loop. The features used for controlling the fundamental components of powers, have only the capability of sharing the positive sequence of the fundamental component of the load current among DGs. However, other components of the load current for example the harmonic components are shared depended on the impedances between the location of load and each DG (involving the impedances of DG and line). On the other hand, in the power circuit of each DG, an inverter with an LC filter is placed after the dc link. Furthermore, an inductor is usually added after the LC filter (here, called L_0), which its value is equal to the value of the inductor of LC. In fact, it could be said that often there is an LCL filter (L_0+LC) after the inverter. So we can make sure that always there is an impedance between DGs that limits their circulating current [3]. The disturbance voltage drop across L_0 (caused by harmonic currents) causes the voltage after this inductor to be disturbed and since the loads are usually placed right after or at slight distance from this inductor, such a disturbance may cause malfunction of sensitive loads.

Several methods have been presented in [4-8] for improving nonlinear load sharing among DGs. These methods are based upon exerting a virtual impedance on the currents path of harmonic components. A different control strategy has been proposed in [5] in order to harmonic power sharing in an islanded MG. The proposed control strategy uses negative virtual harmonic impedance for compensating the effect resulted from line impedance on harmonic power delivery. In [4], it has been proposed that the harmonic current of any order to be used for creating a voltage drop which had the ability to lead the current by 90 degrees. In this way, it can be possible that a virtual inductance to be created at harmonic frequencies. However, since the impedance value of a virtual resistance has no dependency on frequency, it is commonly preferred to a virtual inductance; from the other point of view, it helps damp the oscillations of the system; however, at high frequencies an inductance will bring about a large impedance value, which leads to the disturbance in the output voltage of DGs. In connection with this point, in [8], fixed harmonic resistances have been utilized.

As it is proposed by [4-8], using fixed values for virtual impedance cannot cause a suitable nonlinear load sharing in MGs which are particularly asymmetric with respect to the load distribution or lines impedance. Also, no solution has been presented for mitigating the voltage distortion after the output LCL filters.

In this paper, a new structure is presented for the virtual impedance, to adaptively improve the nonlinear load sharing among DGs and mitigate the voltage distortion after the output LCL filters at harmonic frequencies. In the presented structure, for different harmonic frequencies, virtual resistances with variable values are implemented. The amount of the nonlinear load supplied by each DG is the measure for determining the value of harmonic resistances of that DG. As a result, a significant decrease in the effect of the asymmetry of MG impedances is realized. Furthermore, in order to compensate for the disturbance voltage drop across L_0, a virtual capacitive impedance with a value equal to the impedance of the inductor is created against the harmonic current. This improves the quality of the voltage at the output of the LCL filter.

However, it is noteworthy that suitable sharing of a nonlinear load among DGs leads to a distortion in outputs of the DG and finally an increases in SLB harmonics. Until now, numerous approaches have been proposed for controlling MGs with the aim for compensating the voltage and current harmonics. Generally speaking, these approaches are based upon either independent control of the interface inverter of DG or central controller for compensating the distortions. With regard to this, in [9], a single phase DG has been regarded as a shunt active filter. That is to say, the DG injects harmonic currents for improving the voltage quality. A control technique established upon the selective compensation of voltage harmonics has been proposed in [8] for an MG, which had been connected to the main grid. In [10-13], some other techniques have been presented for the local control of DGs, in which the concept of resistive behavior has been utilized for compensating the voltage harmonics. The authors of [12] have presented another local control technique to be applied in islanded MGs. Their solution has utilized a load compensator, besides to the power controllers and inner control loops of voltage and current. The droop characteristics based upon harmonic reactive power has been implemented in [13] for sharing the compensation workload among DGs. In connection with this point, the authors of [14] have presented a method for sharing the compensation workload of DGs making use of the free capacity related to the interface inverters. In [15], a different control approach has been proposed to coordinate the interface inverters of DGs and the active power filters for compensating the voltage harmonics in MGs. A control algorithm has been presented in [16] for compensating the voltage and current harmonics.

In most of the methods mentioned, the process of voltage harmonics compensation has been conducted at the output bus of the DG. However, the power quality at the SLB is very important due to the fact that sensitive loads are connected to it. Additionally, when DGs try for local compensation of voltage harmonics at the output bus of their own or a bus nearby, harmonic distortion might be increased at other buses of the system (for example at the SLB). Accordingly, by direct compensation of the SLB voltage harmonics, perfect power quality for sensitive loads is certain [8], [17].

In the present work, a new technique is presented for the local control of DGs for selective compensation of the SLB voltage harmonics. It has the capability for adjusting the compensation percentage proportional to the existing level of distortion at the SLB. In addition, this controller delivers a perfect sharing of compensation workload, by considering the nominal capacity of DGs through improving the nonlinear load sharing.

2. Control system of DGs in MG

The details of the scheme proposed for control system of DG_k together with its power stage are shown in Fig. 1. As can be seen in this figure, the voltage harmonics are compensated at the local control level. The power stage of each DG is composed of a dc link, an interface inverter of voltage source type and an LCL filter. Since the approach proposed in this paper is focused on controlling DG interface inverters, it is assumed that in the simulations, a nearly constant voltage is always supplied at the dc link by the inverter. As can be seen in Fig. 1, the potential fluctuation of the dc link voltage is taken into account by a feed-forward loop in generating the control signals of the inverter. The local DGs control system is designed in *αβ* reference frame, and the Clarke transformation is used for transmitting variables from the *abc* frame to *αβ* frame.

It should be mentioned that in this paper, the harmonics voltage measurement technique of SLB is compensated. The details of SLB's 5^{th} and 7^{th} harmonic voltage extraction are shown in the measurement block of Fig. 1.

A. Proposed structure for selective virtual impedance

As it is mentioned, for controling the active and reactive powers of the fundamental component, the system impedance is supposed to be predominantly inductive. Accordingly, the virtual impedance is integrated to the system at fundamental frequency to cause more inductive DG output impedance and eventually more inductive total impedance in the system. Furthermore, the addition of virtual resistance facilitates damp the fluctuations in MG [4], which otherwise, can be done using a real resistance at the cost of increase in losses. Due to that, for avoiding a decreased efficiency, the virtual resistance obtained by a lossless control loop is preferable [18] and in addition, its value has to be selected in such a way that the system impedance stays inductive.

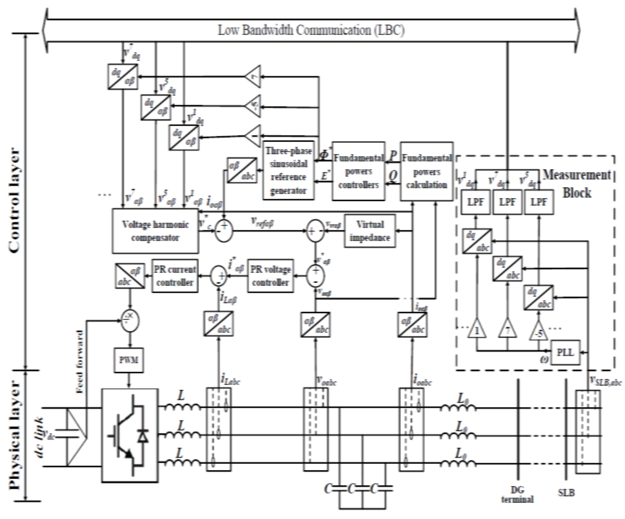


Fig. 1. Details of control system used for controlling DGk to compensate voltage harmonics.

On the other hand, in MGs, the impedance of distribution lines has a significant impact on the accuracy of power sharing among DGs. Therefore, by generating a virtual impedance at the fundamental frequency, the amplitude and phase of DGs' output impedance can be adjusted such that the effect of the asymmetry of the line impedance on the accuracy of power sharing among DGs is minimized [19].

Also, the harmonic frequencies due to nonlinear load sharing and voltage distortion after the output LCL filters can be improved by a virtual impedance. Therefore, the basic structure of the virtual impedance in [19], is expanded by adding a virtual resistive-capacitive impedance at main harmonic frequencies as shown in Fig. 2.

In Fig. 2, to compensate the harmonic voltage drop across L_0, a capacitive vitual impedance with a value of L_0 is generated against the main orders of the harmonic current. Also, $R_{v,harm}$ represents the virtual resistance at harmonics frequencies. The value of $R_{v,harm}$ is adaptively determined based on the amount of the nonlinear load supplied by each DG to improve nonlinear load sharing among DGs of MG. The non-fundamental apparent power (S_n), which can be called harmonic power, is considered as the power generated by each DG to supply the nonlinear load. According to Fig. 2, $R_{v,harm}$ is determined by using Equation (1).

$$R_{v,harm} = K_v . S_n \qquad (1)$$

where, K_v is a small positive constant, determined based on nominal power of DGs, i.e. the greater the power of a DG, the smaller its K_v. S_n is calculated based on IEEE 1459-2010 standard [20] by Equation (2).

$$Sn = S.\sqrt{(THD_I)^2 + (THD_V)^2} \qquad (2)$$

where S, THD_I, and THD_V represent the apparent power of the fundamental component, current THD, and output voltage THD, respectively.

According to Equation (1), as S_n increases, the value of $R_{v,harm}$ increases, which is a limiting factor for S_n, since the values of the resistance among DGs and the load increase at harmonic frequencies. Therefore, a virtual impedance is obtained which is composed of separate virtual impedances at fundamental and harmonics frequencies.

B. Proposed structure for selective compensation of voltage harmonics

Fig. 6 shows the details of the proposed selective harmonics compensator block of Fig. 1 for DG_k. As mentioned before, the main harmonic voltages of SLB are compensated by using this block.

As can be seen, the compensation reference for each voltage harmonic (v^{*h}_c) is separately generated and then, all of the compensation references are added together. Finally, the obtained value is multiplied by the ratio of the nominal power of the inverter of DG_k to the sum of nominal powers of all DGs ($\sum_{k=1}^{n} S_{0,k}$) so that the total compensation reference (v^*_C) for DG_k is generated and a part of the voltage controller reference is built. By doing so, the compensation workload is shared among DGs in proportion with their nominal powers. According to Fig. 6, v^*_C is generated by Equation (3).

$$v_C^* = v^h_{\alpha\beta}.Gh^h.(HD^h_{I,\max} - HD^h_I).\frac{S_{0,k}}{\sum_{i=1} S_{0,i}} \qquad (3)$$

where, $v^h_{\alpha\beta}$ is the SLB voltage h^{th} harmonic in $\alpha\beta$ reference frame. Gh^h is the gain of the voltage h^{th} harmonic compensation, which is determined based on the existing level of disturbance at the SLB. As can be seen in Fig. 3, firstly v^1_α, v^5_α, and v^7_α are used to calculate the harmonic disturbance indices (HD^5, HD^7). Then, these indices are compared with their reference values; finally, the outputs of these controllers are multiplied by v^5_α, v^7_α, k^5_G and k^7_G, respectively, to calculate G^5_h and G^7_h. k^h_G is a positive constant which is the same for all DGs. By increaseing k^h_G, the h^{th} harmonic of the SLB voltage is more compensated. Also, it should be noted that using very high values for k^h_G can make the control system unstable. The saturation block in the proposed control structure is aimed at preventing the compensator from acting if HD^h is less than the reference value. By adjusting G^h_h, the DGs can be adjusted in a way that by injecting harmonic currents in the opposite phase, voltage harmonics are generated in the opposite phase of $v^h_{\alpha\beta}$ so that they can decrease harmonic disturbance at the SLB.

In Equation (3), HD^h_I is the distortion index of h^{th} harmonic related to the DG output current. The calculation process of this index is shown in Fig. 3. As it is obvious, first, the components of fundamental and h^{th} harmonics of the current in α axis (i.e., I^1_α and I^h_α) are taken out, and average values (that is, I^1_α and I^h_α) are then calculated and used for obtaining the HD^h_I. Since in this work the electrical system is considered to be balanced, making use of β component for finding HD_I will provide the results that are similar. In other respects, when the system is unbalanced, to calculate HD, it is needed to extract positive and negative sequences of harmonics, which is not the purpose of this paper. $HD^h_{I,max}$ is the maximum value of HD^h_I which is taken to be 1, here. That is to say, the amplitude of the fundamental component in the system is always larger than that of the current harmonic component. However, a larger value of $HD^h_{I,max}$ may be used, if needed. In this technique, HD_I is supposed as an index for the amount of the contribution of each DG to the compensation with the result that the SLB voltage harmonics compensation is fulfilled by injecting harmonic current of DGs and therefore increasing HD^h_I. Hence, taking into account ($HD^h_{I,max}$-HD^h_I) in Equation (3) leads the compensation workload to be shared among DGs. This is to the fact that increasing workload is equivalent to increasing HD^h_I, and consequently, decreasing ($HD^h_{I,max}$-HD^h_I). It is demonstrated that there exists an intrinsic feedback in this approach for compensation. The notion used for sharing compensation workload is comparable to sharing powers of fundamental component among DGs in an islanded MG.

3. Simulation results

The studied system is shown in Fig. 4. As mentioned before, the MG has two DGs and the nominal power of DG_1 is twice of DG_2. The rated values of the phase voltage and frequency of the MG are considered to be equal to 230V and 50 Hz. The power stage of each DG consists of a dc link, an inverter and an LC filter. Also, an inductor is added to the output of each DG so that an LCL filter is formed. A balanced three phase load with Y connection (with the impedance of Z_L) and a full wave three phase diode rectifier are connected to the SLB as linear and nonlinear loads, respectively. Based on the data provided in Table 1, it can be seen that the value of the impedance Z_{11} is considered to be twice of the impedance Z_{12}, so that an asymmetric state is modeled for the MG.

In order to investigate and analyze the performance of control systems of DGs in compensating the voltage harmonics and improving nonlinear load sharing among them, the simulation is carried out four steps:

In the first step (0sec≤ t <1.5sec), only the resistive-iductive virtual impedance of the fundamental component is active and no compensation is carried out. In the second step (1.5sec≤ t <3sec), the capacitive virtual impedances are added for 5^{th} and 7^{th} harmonics, in order to improve the quality of v_{out1} and v_{out2}. In the third step (3sec≤ t <4.5sec), the resistive virtual impedance is activated for 5^{th} and 7^{th} harmonics but there is no compensation. In the fourth step (4.5sec≤ t <6sec), the SLB voltage harmonics compensation is activated.

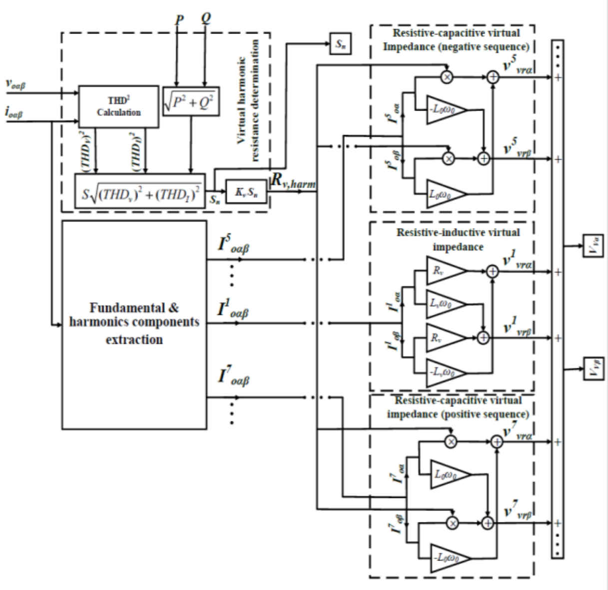


Fig. 2. Block diagram of proposed selective virtual impedance.

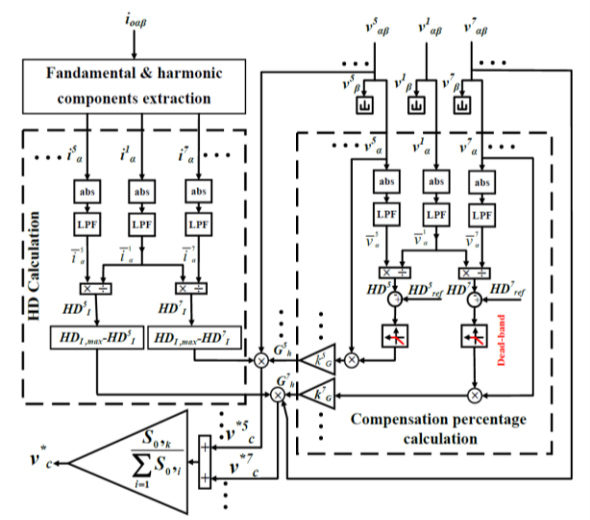


Fig. 3. Proposed selective harmonic compensation block for DGk

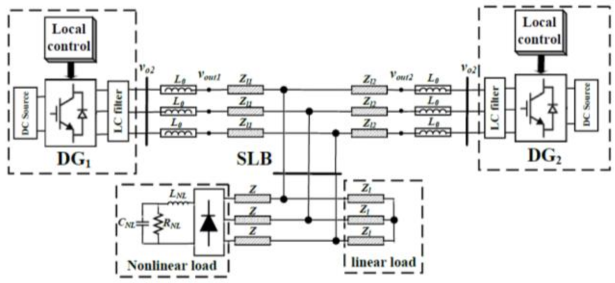


Fig. 4. Overall structure of islanded MG used for simulation.

Table I. Parameters of power stage of electrical system used for compensation of voltage harmonics.

Distribution line of DGs	Z_{l1}, Z_{l2} (Ω-mH)	0.2-3.6, 0.1, 1.8
Outpot inductor of DGs	L_{01}, L_{02} (mH)	1.8
Distribution line of nonlinear load	Z (Ω-mH)	0.1-1.8
Linear load	Z_l (Ω-mH)	50-20
Nonlinear load	$C_{NL}(\mu F)$, $R_{NL}(\Omega)$, $L_{NL}(mH)$	0.084, 150, 235

Table II. Parameters of control system of DGs used for compensation of voltage harmonics.

Active and reactive power controllers		
DG_1 , DG_2	$m_{pp}(rad/W)$	10^{-5}, 2×10^{-5}
	m_{ip} $(rad/W.s)$	10^{-4}, 2×10^{-4}
	n_{pQ} (rad/W)	10^{-1}, 2×10^{-1}
Virtual impedance		
DG_1 , DG_2	$R_V(mH)$	0.25, 0.5
	L_V (mH)	2.5, 5
	K_v	0.004, 0.008
Voltage and current controllers	k_{pV}, k_{pI}	1, 5
	k_{rV1}, k_{rI1}	100, 1000
	k_{rV5}, k_{rI5}	50, 100
	k_{rV7}, k_{rI7}	175, 100
	$\omega_{CV}/\omega_{cI}(rad/s)$	2
Harmonic compensation	K^5_G, K^7_G, HD^5_{ref}, HD^7_{ref}	12.5, 35, 0.5%,0.5%

A. *First step of simulation*

The voltage waveforms of three phases of v_{o1}, v_{o2}, v_{out1}, v_{out2} and the SLB in different steps of simulation are shown in Fig. 5. As it has been expected, v_{o1} and v_{o2} are nearly sinusoidal in the first step and it shows the efficiency of the voltage control in tracking the reference value generated by the droop control. However, it is observed in Figs. 5 and 6 that v_{out} and v_{out2} are disturbed due to the voltage drop across L_0. Furthermore, in these two figures, it can be seen that the SLB voltage has significantly disturbed. In fact, due to the harmonic voltage drop on distribution lines of DGs, the SLB voltage has been subjected to harmonic disturbances.

Fig. 7 shows that before adding harmonic virtual impedances in the first step, S_n is shared between DGs in almost inverse proportion with their line impedances. This means that the amount of the S_n supplied by DG_2 is more than that of the amount supplied by DG_1 whereas the nominal power of DG_2 is half of the nominal power of DG_1. The output current of DGs are shown in Fig. 8. As can be observed, in the first step, the total current supplied by DGs is not proportional to their nominal powers.

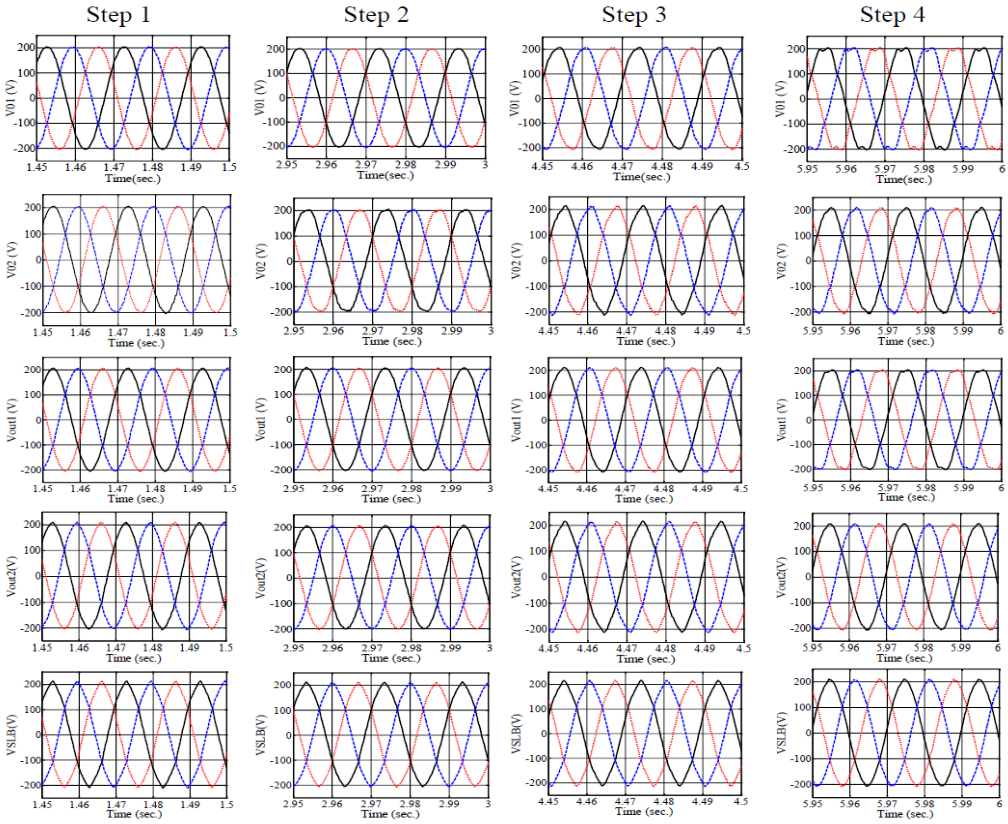
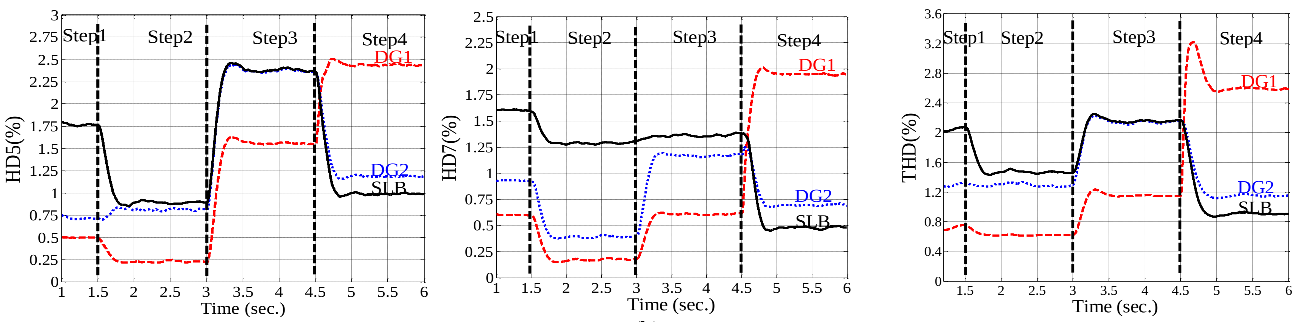


Fig. 5. Waveforms of three phase voltages at different simulation stages: first row: v_{o1}, second row: v_{02}, third row: v_{out1}, fourth row: v_{out2}, fifth row: v_{SLB}



(a) (b) (c)

Fig 6. Voltage harmonic distortions (fundamental component=100%): output of LCL filters

B. Second and third steps of simulation

It is observed in Fig. 5 and 6 that introduction of capacitive virtual impedance in the second step improves the quality of v_{out1} and v_{out2}, and the voltages of v_{o1} and v_{o2} are increased in return.

In the third step of simulation, the harmonics virtual resistances are added to the basic control structure of DGs at t=3s. These resistances are placed on the path of harmonics currents to improve the nonlinear load sharing between DGs. In Fig. 7 it can be seen that once these resistances are added, the nonlinear load sharing between DGs has significantly improved but still it is not proportional to the nominal power of DGs.

On the other hand, according to the results of Figs. 5 and 6 for the second period, adding virtual resistances at harmonic frequencies results in an increase in output voltage distortion of DGs and consequently an increase in the voltage distortion at the SLB.

C. Fourth steps of simulation

In the fourth step, the voltage harmonics compensation unit in local controllers of DGs, is activated. According to Fig. 6 (a and b), it is clear that the HD^5 and HD^7 of the SLB voltage are significantly decreased. It leads to significant reduction of the SLB voltage *THD* according to Fig. 6 (c). The improvement in the voltage quality at the SLB can also be observed in Fig. 5. Also, it can be seen in Figs. 5 and 6 that the voltage harmonics compensation is accompanied with an increase in DG_1 voltage distortion. In this regard, it must be noted that the impedance of the distribution line of the DG_1 is fairly greater than its corresponding value in DG_2 and considering its nominal power, the amount of the harmonic load supplied by this DG is greater than one supplied by DG_2. Consequently, the voltage drop across the line of the DG_1 and its harmonic virtual resistances cause the increase in the SLB voltage distortion before compensation. After compensation, the output voltage distortion of this DG is increased in order to provide an almost sinusoidal voltage at the SLB after harmonic voltages across the distribution line and virtual resistances. On the other hand, due to the small values of the impedance of the distribution line of the DG_2 and nonlinear load supplied by it, as it is observed in Figs. 5 and 6, the change in harmonic distortion of this DG as a result of activation of compensation, is similar to the SLB.

Furthermore, it is shown in Fig. 7 that during compensation of SLB voltage harmonics, the S_n of DGs has increased. This increase is mainly because the main harmonic currents of DGs are increased so that compensation of voltage harmonics becomes possible.

Also, since the nominal power of the DG_1 is twice of DG_2, it must have a greater share in compensation. Therefore, the results of the fourth step of the simulation show greater increase in the S_n and harmonic distortion of the output voltage and current of DG_1 compared to DG_2.

On the other hand, it can be seen in Figs. 7 and 8 that after SLB voltage harmonics compensaion, nonlinear load sharing between DGs has been significantly improved and this power is shared between DGs almost in proportion with their nominal powers. This improvement in nonlinear load sharing between DGs shows the effectivenss of the proposed structure for harmonic virtual resistances and the efficiency of the solution selected for workload sharing.

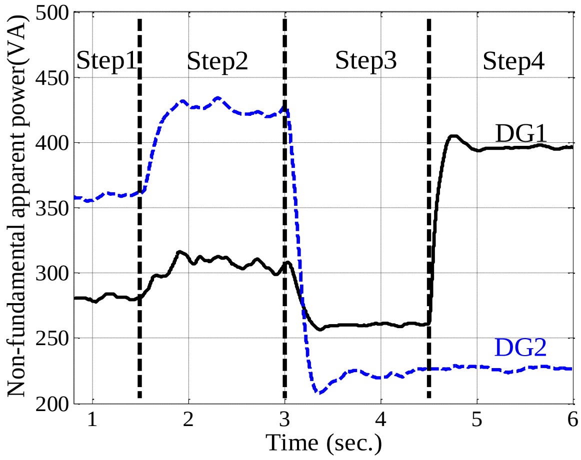


Fig. 7. Variation curves of non-fundamental apparent power

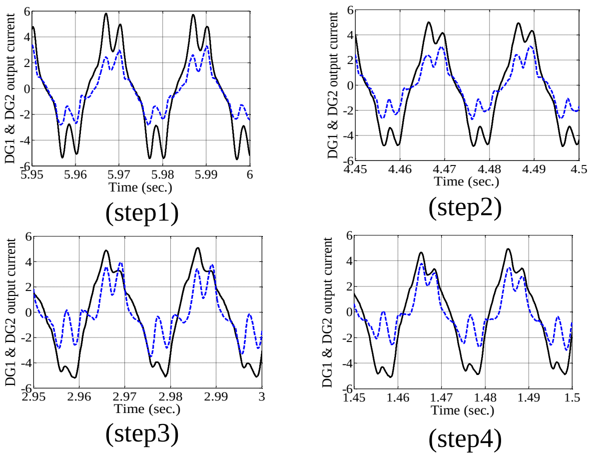


Fig. 8. Waveforms of phase-a output current of DGs at different simulation stages. (DG1: solid line, DG2: dashed line)

4. Conclusion

In this paper, a new structure has been proposed for the selective virtual impedance in islanded MGs. The proposed structure is able to adaptively share the powers of fundamental and nonfundamental (nonlinear load) components among DGs and mitigate the voltage distortion after the output LCL filters. Simulation results show that proper nonlinear load sharing among DGs has increased the output voltage harmonics of DGs and SLB. This can cause problems for sensitive loads connected to the SLB. Therefore, a new approach has been proposed for compensating main voltage harmonics at the SLB using the local DG control systems which is able to adjust compensation percentage in an adaptive way, in proportion with the existing amount of the distortion at SLB. In addition to properly sharing compensation workload, the proposed technique properly decreases the voltage harmonics at the SLB. The results showed that by using the proposed approach, the quality of the SLB voltage is remarkably improved; also, the powers of fundamental and non-fundamental (nonlinear load) are proportionally shared between DGs.

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