

## Analysis of the Advanced Static Var Compensator Performance using ATPDraw

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**Abstract** — This paper presents a study on the operational performance of the Advanced Static Var Compensator (ASVC) in different situations of the supply network, observing mainly the time response of the control loop in situations of momentary and balanced voltage sags and swells. It also verifies the operation of the ASVC in the regulation of the voltage magnitude in the AC bus. For this, it will be performed certain simulations of an electrical system using the software ATPDraw and it will be also presented all the theory involved in the modeling of the compensator in question.

### Key words

FACTS, parallel compensation, voltage regulation, ASVC, ATPDraw.

### 1. Introduction

The Electrical System (SE) is intended to guarantee the energy supply with quality and in an uninterrupted way, that is, the electrical network must meet several requirements of frequency, magnitude, low THD<sub>V</sub> and a continuous supply of electric energy. In order for this objective to be achieved, a number of devices are required, which together make up the generation, transmission and distribution systems. Among these devices, there are those that operate to control the voltage level in the buses of the system, thus, providing that the limits permitted according to the Brazilian requirements are met.

In this context, the first publications about FACTS (Flexible AC Transmission Systems), a technology that uses high-power and high-speed Gate Turn-off Thyristor (GTO), have emerged in the 80's. Thus, it was possible to develop several devices, highlighting the ASVC (Advanced Static Var Compensator), which is intended for the compensation of reactive power [1].

In general, the ASVC power circuit is a frequency inverter powered by a pre-charged capacitor and, through a transformer, the inverter is connected to the system bus on which is desired to perform the compensation, as shown in Fig. 1. Therefore, the compensator has the following purpose: to regulate the voltage of the bus in which it is connected to and maintain constant the voltage in the terminals of the capacitor

in the input of the frequency inverter.

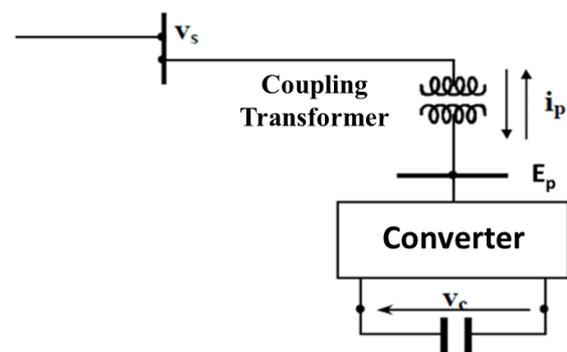


Figure 1. Schematic drawing of an ASVC

At where:

$v_s$  - AC system voltage on the ASVC coupling point

$i_p$  - branch current between the ASVC and the CA system

$E_p$  - voltage at three - phase ASVC converter terminals

$v_c$  - voltage at the ASVC capacitor terminals

In order for the compensator to achieve the described objectives, it is necessary to create a measurement and control system of the electrical quantities involved ( $v_s$ ,  $E_p$ ,  $i_p$ ,  $v_c$ ), since the ASVC must be able to identify the bus voltage level and the voltage in the capacitor terminals and to verify that the measured values are adequate. That is, the control system should work as a closed loop. This makes the process virtually instantaneous and more reliable. To do so, it is necessary to calculate the active and reactive power that the AVSC injects to or absorbs from the AC system through the theory of instantaneous power and to transform the three-phase quantities through the vector theory. In this context, references [2] and [3] approach the various ASVC power flow control strategies.

Therefore, the purpose of the present article is to analyze the behavior of an electrical system in which the ASVC is connected to. That is, it will be studied the ability of the compensator to control the voltage level in a bus by removing and inserting load. To do this, the power circuit and the ASVC control loop were implemented in the ATPDraw software, as well as the electrical system in which the compensator is connected.

## 2. ASVC Vector Analysis

The representation of the electric quantities related to the ASVC can be based on the vector theory, since it allows the simplification of the analysis of the compensator behavior and control, as presented in [4]. According to this theory, three-phase voltages and currents can be represented by vectors in the  $dq$  stationary system and in the synchronous reference system  $\alpha\beta$  [1], [5] - [7], as shown in Fig. 2.

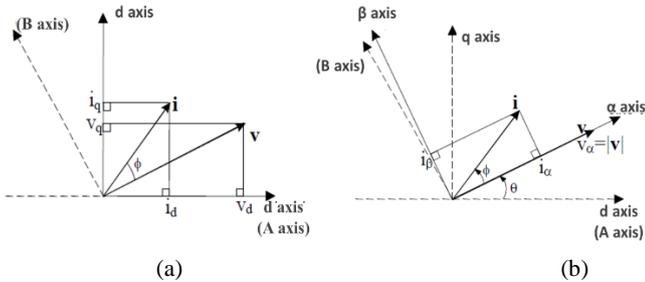


Figure 2. Decomposition of the voltage and current vectors of the stationary reference system (a) and synchronous system (b).

Fig. 3 shows the decomposition of the electric quantities related to the ASVC operation.

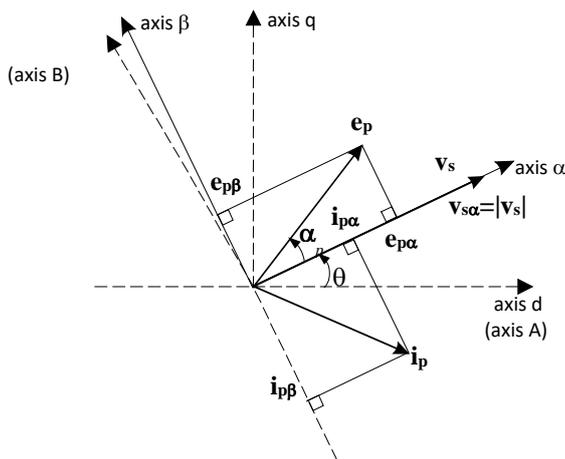


Figure 3. Decomposition of voltages and currents vectors of the ASVC in the stationary and synchronous reference systems.

According to the vector theory, the active and reactive power flow between the AC system in which the compensator is connected and the ASVC itself are shown in (1) and (2):

$$p = \frac{3}{2}(v_{sd}i_{pd} + v_{sq}i_{pq}) = \frac{3}{2}|v_s||i_p|\cos\phi \quad (1)$$

$$q = \frac{3}{2}(v_{sd}i_{pq} - v_{sq}i_{pd}) = \frac{3}{2}|v_s||i_p|\sin\phi \quad (2)$$

whereby:

$\phi$  - angle between the vectors  $v_s$  e  $i_p$ .

From Fig. 3, we can see that:

$$i_{p\alpha} = |i_p|\cos\phi \quad (3)$$

$$i_{p\beta} = |i_p|\sin\phi \quad (4)$$

Thus, substituting (3) in (1) and (4) in (2), we can say that to control the flow of active and reactive power of the ASVC should control its currents  $i_{p\alpha}$  and  $i_{p\beta}$  respectively, as shown by (5) and (6).

$$p = (3/2)v_s|i_{p\alpha} \quad (5)$$

$$q = (3/2)v_s|i_{p\beta} \quad (6)$$

## 3. ASVC Modeling Using Vector Theory

Based on Fig. 1 and considering that the coupling transformer impedance is only reactive, the analysis will be carried out regarding the power flow between the ASVC (with terminal voltage  $E_p$ ) and the bus (with voltage  $v_s$ ), considering the following situations.

### A. Voltage $E_p$ in phase with the voltage $V_s$ of the AC system

When  $E_p$  and  $V_s$  are in phase, the  $i_{p\alpha}$  component of the  $i_p$  current is zero. Thus, based on equation (5), it can be stated that the active power circulating between the ASVC and the CA system is also zero. That is, the compensator does not absorb or inject active power into the system.

In this case, the analyses are reduced only to the magnitudes of the voltages in question, which are made through the phasor diagrams presented in Fig. 4.

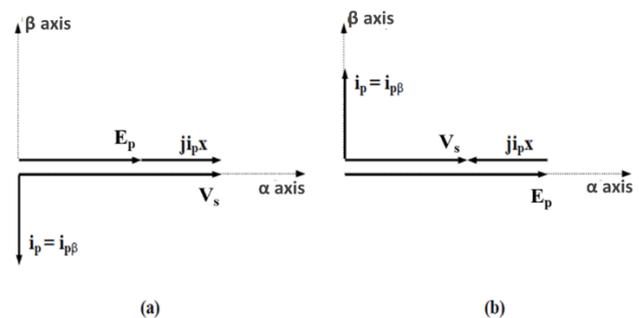


Figure 4. Phasor diagram for the ASVC absorbing (a) and generating (b) reactive power.

As shown in Fig. 4 (a), when  $|E_p| < |V_s|$ , the component  $i_{p\beta}$ , that is responsible for the reactive power flow, is inductive, since it lags the voltage  $V_s$  by  $90^\circ$ .

However, according to Figure 4 (b), when  $|E_p| > |V_s|$ , the reactive component of the current,  $i_{p\beta}$ , leads  $V_s$  by  $90^\circ$ , with a capacitor-like behavior. Therefore, ASVC provides reactive power to the AC system.

Therefore, it is verified that when there is no phase difference between  $E_p$  and  $V_s$ , the reactive power flow between the advanced static compensator and the AC system depends only on the magnitude of the voltage  $E_p$  with respect to  $V_s$ .

### B. Voltage $E_p$ leading the voltage $V_s$ of the AC system

If the voltage  $E_p$  leads  $V_s$ , then the component of the current  $i_p$ , responsible for the active power,  $i_{p\alpha}$ , is negative, as shown in Fig. 5. Therefore, based on equation (5), it is noted

that active power is also negative. This represents that the active power flows from the converter to the AC system, ie, the ASVC supplies active power, causing the capacitor voltage  $V_c$  shown in Fig. 1 to be reduced.

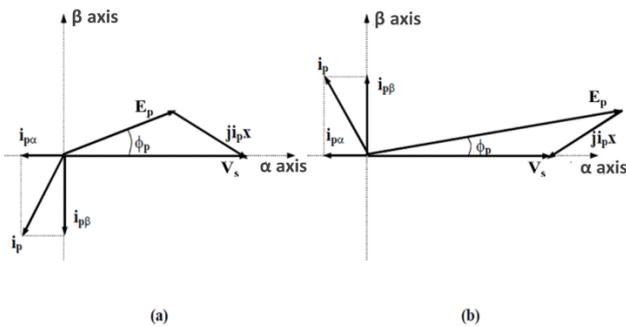


Figure 5. Phasor diagram for the ASVC providing active power: absorbing (a) and generating (b) reactive power

In relation to reactive power, the analysis is similar to the previous case, that is, if  $|E_p| < |V_s|$ , then  $i_{p\beta}$  lags  $V_s$  by  $90^\circ$ , according to Fig. 5 (a), and the reactive power is absorbed from the AC system. In contrast, when  $|E_p| > |V_s|$ , then  $i_{p\beta}$  leads  $V_s$  by  $90^\circ$ , according to Figure 5 (b), therefore, reactive power is injected into the AC system.

C. Voltage  $E_p$  lagging the voltage  $V_s$  of the AC system

Finally, when the voltage  $E_p$  lags  $V_s$ , the  $i_{p\alpha}$  component is positive, as shown in Fig. 6.

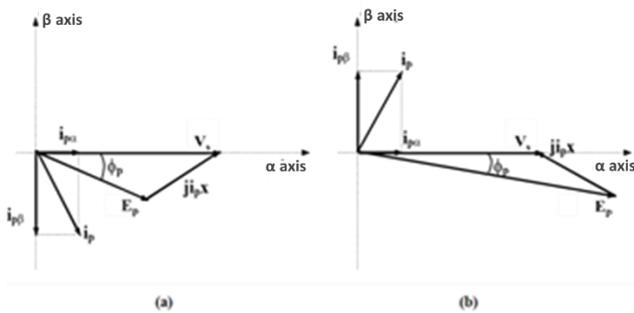


Figure 6. Phasor diagram for the ASVC absorbing active power: absorbing (a) and generating (b) reactive power.

In this way, the active power is also positive, and it is absorbed by the ASVC to maintain the voltage in the DC link capacitor at a constant value.

In relation to the reactive power, the flow direction is determined in the same way as the other cases, ie, depending only on the  $E_p$  and  $V_s$  absolute values. Finally, through the analyses made in section 3, it is possible to conclude:

<b>ASVC</b>	
$P > 0$	→ consumes active power.
$P < 0$	→ provides active power.
$Q > 0$	→ provides reactive power.
$Q < 0$	→ consumes reactive power.

#### 4. ASVC Control System

For the implementation of the ASVC and the electrical system studied, the ATPDraw software was used, and the control and measurement systems were implemented through the MODELS, provided by the software. Thus, it was possible to program a Proportional and Integral controller, defining the switching sequence of the frequency converter and consequently the magnitude and phase of the voltage  $E_p$ , regulating, therefore, both the voltage  $V_s$  of the AC system and the DC voltage at the terminals of the capacitor.

A. Regulating the voltage  $V_s$

To perform the control of the voltage value  $V_s$  of the AC system, the ASVC will act as a reactive compensator, that is, when the voltage  $V_s$  is lower than a reference value, the ASVC must inject reactive power, thereby reducing the line voltage drop and increasing the value of the voltage  $V_s$ . This is possible, only if  $|E_p| > |V_s|$ , thus the higher the voltage  $E_p$  in relation to  $V_s$ , the greater the  $i_{p\beta}$  magnitude (shown in section 3), that is, the higher the reactive power injected into the AC system.

Otherwise, in the case that the voltage  $V_s$  takes values above the reference, then the ASVC must behave as an inductor bank, consuming reactive power, and thus increasing the line voltage drop. This is possible, only if  $|E_p| < |V_s|$ , so, the lower the voltage  $E_p$  in relation to  $V_s$ , the greater the magnitude of  $i_{p\beta}$ , with  $i_{p\beta} < 0$ , that is, the greater the reactive power absorbed by the AC system.

Therefore, to change the reactive power flow and consequently to control the voltage of the AC system, the magnitude of the voltage  $E_p$  at the output of the converter must be changed. It works since it has been verified through the vector theory that the reactive power circulating between the system and the ASVC depends only on the relationship between the absolute values of the voltages  $V_s$  and  $E_p$ .

The output voltage waveform of the converter is obtained from a Sinusoidal Pulse Width Modulation (SPWM) control, i.e. the output pulses of the converter are obtained by comparing a high frequency triangular wave with a sinusoidal waveform of amplitude "k", which has the same frequency as the AC system. Therefore, for the ASVC control to perform a change in the  $E_p$  module, a change in the value of k is necessary, and this is possible due to the use of a proportional-integral controller (PI).

B. Regulating the voltage  $V_c$  at the terminals of the capacitor

In addition, the control system also monitors the voltage  $V_c$  at the terminals of the capacitor. That voltage ( $V_c$ ) starts at a certain value, however, during the compensation process, the capacitor tends to charge or discharge, in this way, the control system has as objective to maintain this parameter in a constant value. For this, the control loop acts on the phase angle of the voltage  $E_p$ , consequently on the active power flow. Thus, the control of such variable is obtained in a similar way to the control of the voltage  $V_s$ , through a second controller PI-2, as follows: when the voltage at the capacitor terminals begins to reduce, the ASVC must apply a voltage  $E_p$

that lags the voltage  $V_s$ , absorbing active power of the system. However, when the DC voltage of the capacitor becomes greater than the desired value, the voltage that the compensator will apply at its terminals ( $E_p$ ) will lead the voltage  $V_s$ , injecting active power into the system.

## 5. Characterization of the Simulated System

In order to study of the ASVC performance, the electric system shown in Fig. 7 was used, where the compensator is connected to the B1 bar, since preliminary studies indicated that this bar is less reliable from the voltage point of view.

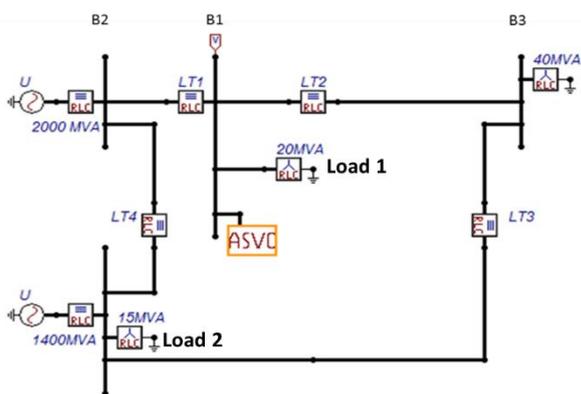


Figure 7. Simulated electric system.

The parameters used in the simulation are shown in Table 1.

Table 1. ASVC simulation data

INPUT DATA	VALUE	UNIT
Primary voltage of the connection transformer	69	[kV]
Secondary voltage of the connection transformer	3,3	[kV]
Percentage resistance of the connection transformer	0,5	[%]
Percentage Reactance of connection Transformer	8	[%]
Nominal power of the connection transformer	50	[MVA]
Capacitance of DC Capacitor	128	[mF]
Converter switching frequency	1,8	[kHz]

In this paper, 4 cases will be simulated, in which the load at the bar B1 is switched on and switched off in order to cause sags and swells in the voltage level of the bar under analysis.

## 6. Results and Discussions

### • Case 1- Voltage sag without the presence of ASVC

In this case, the electric quantities related to the AC system will be analyzed when the B1 bus is submitted to a voltage sag. For this, the system shown in Fig. 7 without

the ASVC was simulated with ATPDraw. Thus, Fig. 8 shows the voltage at bar B1 for intervals 1 (1.5 to 2 seconds) and 3 (3 to 4 seconds), in which only the load 1 of 20 MVA with power factor of +0.92 is connected to bus B1. In interval 2 (3 to 4 seconds), to create a momentary under voltage, another load of 30 MVA with power factor +0.92 was connected to the same bus B1, in addition to the previous load.

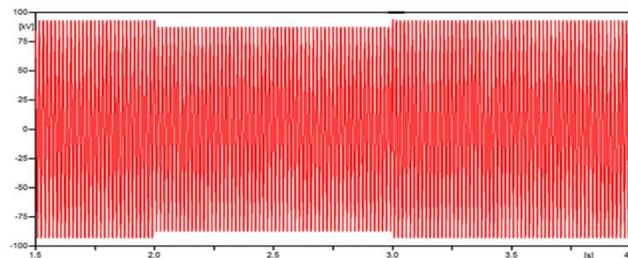


Figure 8. Line voltage in bar B1 - Case 1

Fig. 8 shows a significant voltage sag during interval 2, due to the input of the 30 MVA load. This momentary under voltage is also seen in Fig. 9.

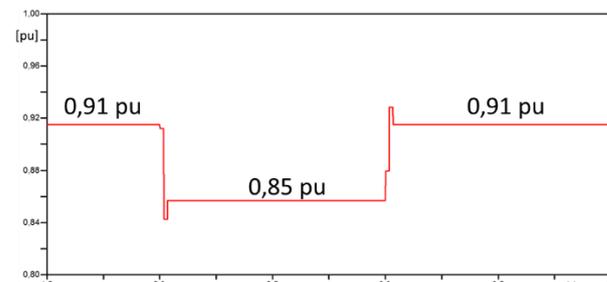


Figure 9. RMS voltage in bar B1 with  $V_{base} = 69kV$  - Case 1

### • Case 2 - Voltage sag with the presence of ASVC

On this occasion, the load of 30 MVA will again be connected to the bus B1 during the interval 2, as in case 1, however, in this case the ASVC is present in the system and functions as a voltage controller in the bus in question. For this simulation, the compensator control system is configured to maintain the voltage at the value of 1 pu (69 kV), as shown in Fig. 10.

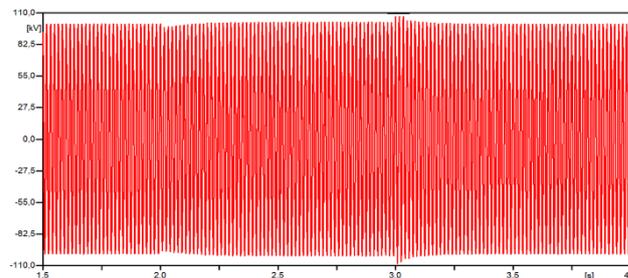


Figure 10. Line voltage in bar B1 - Case 2

It is noteworthy that the ASVC regulates the voltage of bus B1 satisfactorily, with the highest variation of RMS voltage occurring in the transient periods, with values of 0.97 pu at 2 seconds and 1.044 pu at 3 seconds, as Fig. 11 indicates. However, when compared with the previous

case, without the presence of the compensator, this voltage variation presents negligible values.

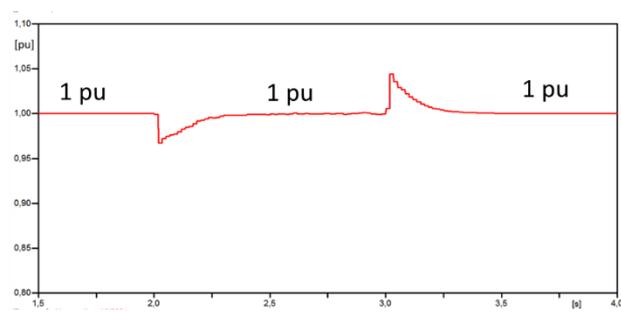


Figure 11. RMS voltage in bar B1 with  $V_{base} = 69kV$  - Case 2

To control the voltage in bus B1 the ASVC behaves as a capacitor, injecting reactive power into the system, however, as the load in interval 2 is considerably higher than in the others, then the reactive power flow between the compensator and the AC system is also larger, as shown in Fig. 12.

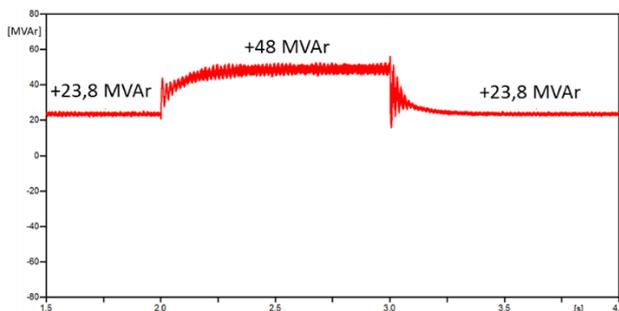


Figure 12. Reactive power flow between the ASVC and the CA system - Case 2

In addition to the control of the voltage in the bus B1, the ASVC also maintains the voltage  $V_c$  of the capacitor terminals in a constant value, as shown in Fig. 13, with small variations of  $\pm 0,005$  pu in 2 and 3 seconds, that is, during the switching of the loads.

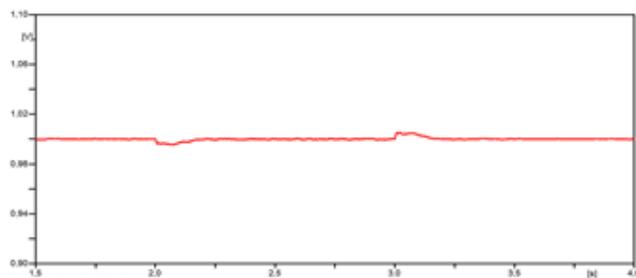


Figure 13. Voltage  $V_c$  at the capacitor terminals,  $V_{base} = 15 kV$  - Case 2

- *Case 3 - Voltage swell without the presence of ASVC*

A momentary rise in the voltage was also simulated. For this, the following switching sequence was performed: between 1.5 and 2 seconds the load 1 of 20 MVA was connected to the bus B1, causing a voltage sag of 1 pu. Between 2 and 3 seconds the load 1 was removed from the bus and another load of 50 MVA with power factor -0.4 (capacitive) was added in the same bus B1, causing the bus

voltage to rise to a value higher than 1 pu. Finally, after 3 seconds the load 1 is connected again and the previous load of 50 MVA is removed, reducing again the voltage in bus B1. Fig. 14 shows the voltage for the three intervals described. It should be noted that the compensator is not connected to the system.

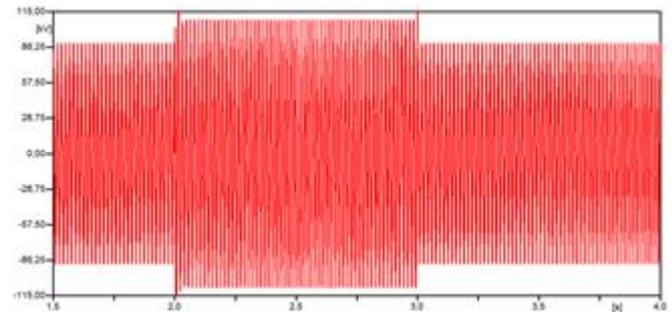


Figure 14. Line voltage in bar B1 - Case 3

Since the ASVC is not connected to bus B1, the RMS value of the voltage reaches a value higher than 10% of the nominal voltage, as shown in Figure 15.

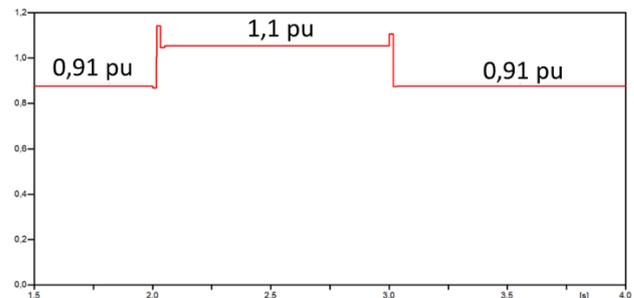


Figure 15. RMS voltage in bar B1 with  $V_{base} = 69kV$  - Case 3

- *Case 4 - Voltage rise with the presence of ASVC*

Finally, in this case, the voltage regulation will be analyzed by the ASVC in face of the voltage rise described in case 3. Thus, the voltage in bus B1, after connection of the compensator, is shown in Figure 16.

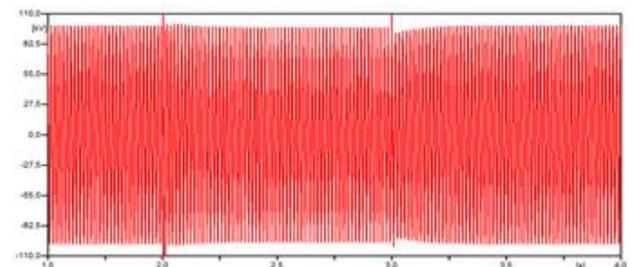


Figure 16. Line voltage in bus B1 - Case 4

The compensator considerably decreases the transient voltage effect, reaching a value of 1.07 pu at 2 seconds and 0.93 pu at 3 seconds, as shown in Figure 17. Except for transient periods, the voltage at bar B1 remains constant, with a value of 1 pu, even after the connection of the capacitive load between 2 and 3 seconds.

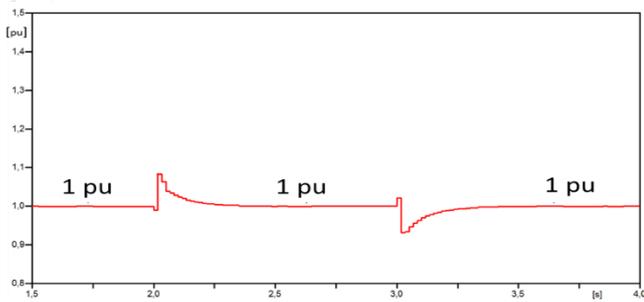


Figure 17. RMS voltage in bar B1 with  $V_{base} = 69\text{kV}$  - Case 4

The control system monitors the voltage level of bus B1 through the injection and absorption of reactive power by the ASVC, so in intervals 1 and 3, the ASVC injects 23.8 MVAR of reactive power, behaving like a capacitor bank with the goal of increasing the voltage in relation to case 3. In the interval 2, as there is a voltage rise, then the ASVC absorbs 22.4 MVAR, thus changing the profile of the reactive power in relation to the previous case. In this case, the compensator behaves as an inductive load connected to the bus in question, avoiding the raising of the voltage. The voltage regulation can be seen in Fig. 18.

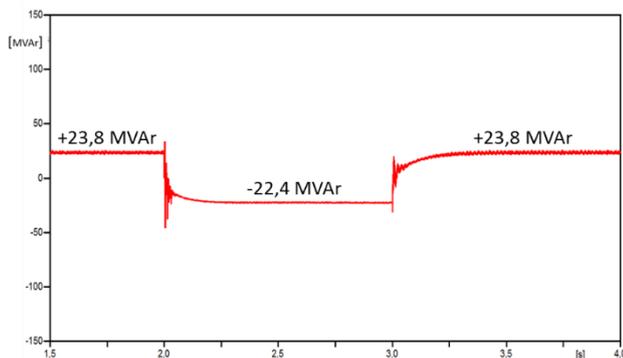


Figure 18. Reactive power flow between the ASVC and the CA system - Case 4

Finally, Fig. 19 shows the voltage  $V_c$  at the terminals of the ASVC capacitor, which presented the greatest variation in 2 and 3 seconds ( $\pm 0,007$  pu), the moments that occurred changes in the load connected to the bar B1. However, due to the control system, the value of 1 pu was maintained under the steady state.

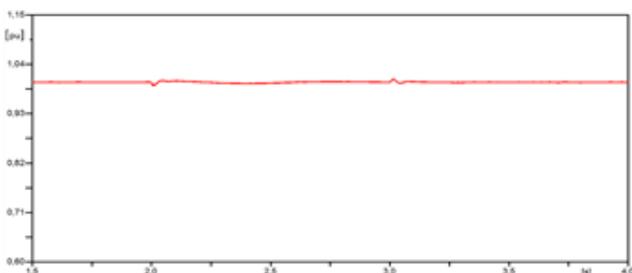


Figure 19. Voltage  $V_c$  at the capacitor terminals,  $V_{base} = 15\text{ kV}$  - Case 4

## 7. Conclusions

Through the computational simulations, the ability of the ASVC to control the voltage level of the AC system was verified, and through graphs, it was noted that the

compensator provides adequate control of both the AC system voltage and the DC capacitor voltage. Then, the behavior of the ASVC was simulated and investigated in situations that affect power quality, both with a momentary voltage sag and swell, and again it could be seen that the compensator controls the AC voltage of the system. In addition, it is noted that the ASVC monitors the voltage through the reactive power injection (when the voltage is below the desired) and the reactive power absorption (when the voltage is higher than desired). Finally, it is verified that the voltage  $V_c$  at the terminals of the capacitor remains constant, showing that the control loop is reliable.

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