18th International Conference on Renewable Energies and Power Quality (ICREPQ'20)
Granada (Spain), 1st to 2nd April 2020
Renewable Energy and Power Quality Journal (RE&PQJ)
ISSN 2172-038 X, Volume No.18, June 2020

Cascaded Multilevel Converter as a Voltage Compensator

J. Iwaszkiewicz[1], A. Muc[1]

[1] Department of Electrical Engineering
Gdynia Maritime University, Poland
Morska St. 81-87 (Poland)
e-mail: j.iwaszkiewicz@we.umg.edu.pl, a.muc@we.umg.edu.pl

Abstract. The paper presents a laboratory prototype of the three-phase voltage compensator with an energy storage based on supercapacitors. The system described is able to protect an isolated grid, e.g. in industry, against short voltage interruptions, dips and sags. An idea of a control method as well as a digital controller has been discussed. Experimental results are also included.

Key words. supercapacitor, voltage dips and sags, multilevel inverter, synchronization

1. Introduction

Low efficiency of existing electrical grid causes too big energy losses and lower power quality at all levels of the grid. As a result, the energy flow at the grid is unperfect.
It is estimated that 90 % of grid disturbances are provoked by voltage sags and interruptions of duration less than one second. But even such short interruptions of power supply cause significant losses of manufacturing process and disturb operations of information systems.
An efficient and necessary way to improve the energy flows at the grid and to reduce losses caused by the voltage sags and interruptions is a wide and intensive use of power electronics-based energy/power flow controllers. They have to be implemented as fast, multilevel, high precision inverters equipped with high efficient energy storing devices such as e.g. high voltage, high power supercapacitors. The supercapacitors have parameters extremely adequate for requirements of the grid [1, 2]. Stacked and prismatic supercapacitors are used as energy sources in standard applications.

The public grid is a vast system susceptible to interruptions. This forces the need to protect sensitive receivers on the power outage, because even brief disturbance may cause them to malfunction. Traditionally for this purpose uninterruptible power supplies (UPS) are used. These devices are equipped in chemical batteries as electric energy sources. These means allow to maintain power during the interval of several minutes to several hours. In case of short-term voltage disturbances caused by processes such as, for instance, a short circuit, compensators become an alternative to UPS devices.

A three-phase voltage compensator assembled of a cascaded multilevel converter equipped in supercapacitor store has been presented in [3]. The paper described the main idea and topology of the line-interactive compensator. The cascaded inverter has been used in order to improve the compensator performance in comparison to usually used two-level inverters. The compensator built of such inverters did not resolve satisfactory a problem of distorted waveforms in generated voltage. In [4] the authors presented some improvements in the synchronization mechanism which have been inserted in order to assure a proper sag detection. The paper summarizes theoretic and circuit consideration presented in [3, 4] and supplements the subject in successive remarks and experimental results.
The principle of the compensator performance allows to classify it as a special kind of active filtering devices or off-line dynamic voltage restorers (DVR). DVRs that use only supercapacitors (electric double layer capacitors, EDLC) as an energy store do not need any service applied usually to energy storage devices based on batteries. Typically, the DVR uses transformers connected in series and injecting relatively high losses to the grid [5]. There are also proposals of transformerless compensators. An interesting proposal of such an energy storage system has been presented in [6].
The compensator circuit in question was based on a cascade multilevel PWM converter using star configuration. The expected characteristics of the compensator suggest that it should be considered as a cascaded multilevel inverter, characterized by off-line mode of operation and ability of 100% voltage regeneration regardless of sag depth.

2. Construction of the laboratory model

The novel three-phase compensator laboratory model has been built as a standalone and integrated device and tested in the Electrotechnical Institute laboratory as a result of a special research project COST/255/2009. The compensator consisted of three independent one-phase multilevel cascaded inverters and an energy store based on high voltage stacked supercapacitors type EDLCs.
Three identical single-phase compensators are star connected as shown in Figure 1. Each single-phase

compensator is formed as a cascaded multilevel inverter built from two or three H-bridges units which are independently supplied. This allows to utilize lower rated voltage of semiconductor switches in order to receive output voltage waveforms of higher amplitudes. Another advantage is concerned to the number of possible voltage steps in the output waveform.

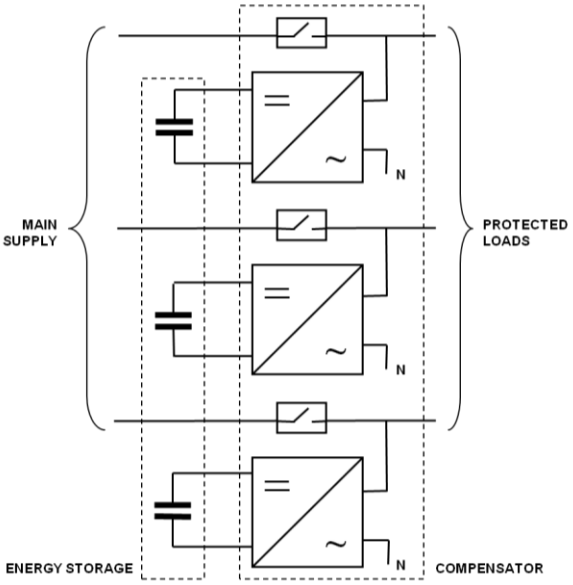


Fig.1. Block diagram of the three-phase voltage outages compensator

To realize a compensation process or active filtering it is possible to use transformer less connection between the compensator device and the voltage power grid [6].
The energy exchange process between the network and the supercapacitor provides the cascade inverter consisting of two H-bridge inverters connected in series and supplied by two DC/DC intermediary circuit converters (P_1 and P_2). The key $K_{1,2,3}$ denotes a very fast switch placed between phase line and protected network. The switch is able to disconnect the load from the mains. The load consists of three impedances $Z = R + j\varphi L$ connected to outputs $L_{1,2,3o}$. Symbols L and R denote parameters of the load. Most of time the switch K is closed allowing energy flow from the mains to load and to the compensator. It must be disconnected at the specific instant of voltage interruption or dip when the compensator takes over to power sensitive loads.

3. The laboratory model construction

Experimental tests have been executed on a more complicated compensator circuit. A block diagram of the circuit is presented in Figure 2. The compensator has been developed by adding two DC/DC converters. Their task is to maintain the standardized and controlled level of the voltage supplying the particular H bridges of the compensator. Additionally, three capacitors: C, C_1, C_2 have been connected. The capacitor C is a filtering element while C1 and C2 are energy stores.

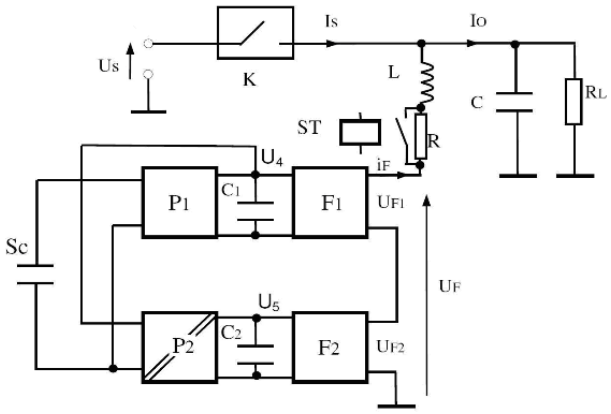


Fig.2. The simplified block diagram of the one phase of the three-phase voltage outages compensator.

The compensator consists of three identical converters. Each converter is parallel connected to the appropriate phase of the protected network and operates independently. The schematic diagram of one phase of the compensator is presented in Figure 3. The balance of currents in the point of common coupling of the network, load and compensator is as follows: $I_S + i_F = I_O$ where I_S i_F, I_O denote network, compensator and load currents respectively.
Every phase of the compensator is equipped in one block of supercapacitors forming an energy store. In order to supply each H bridge separately a high frequency transformer has been used. The main energy storage in each phase is accomplished by high voltage supercapacitor Sc: 2 F/300 V, manufactured by Russian enterprise ECOND. The energy storage capacity of this component is approximately 90 kJ.

The adopted compensator topology requires the usage of mutually isolated power converters (blocks P_1 and P_2) and inverter bridges F_1 and F_2 forming the asymmetrical multilevel inverter operating as an inverter or a rectifier charging the supercapacitor $\mathbf{S_C}$. The converters have been realized using electro insulated IGBT modules IPM 200 A / 1200 V manufactured by Mitsubishi. The single module contains two power switching elements with power diodes and gate circuits. For the cores of inductive components i.e. transformers and reactors the amorphous magnetic material with high saturation induction (type 2605SA1, Metglas) in the form of a slot-shaped CC has been chosen. As an AC switch K the thyristor electroinsulated module with rated current 125 A (Crydom) has been used. The converters F_1 and F_2 are connected to the grid through LC filter circuit and a resistor R in series for pre-charging electrolytic capacitors C_1 and C_2. The voltages U_4 and U_5, supply constituent inverters F_1, F_2. the switch.

In the control part of the compensator an integrated controller card with a CPU unit based on a signal processor TMS320F2812 (Texas Instruments) is used.
The controller is coupled with the transistor modules using fiber-optic cables. Due to the short operating time semi-adiabatic cooling processes protecting semiconductor switches was not necessary.
Figure 4 presents a view of the three-phase compensator construction: front and back side of the device in Figure 4a and the three-phase electric energy storage which is shown

in Figure 4b. It has been located in separate compartment and connected to the compensator by the cable line.

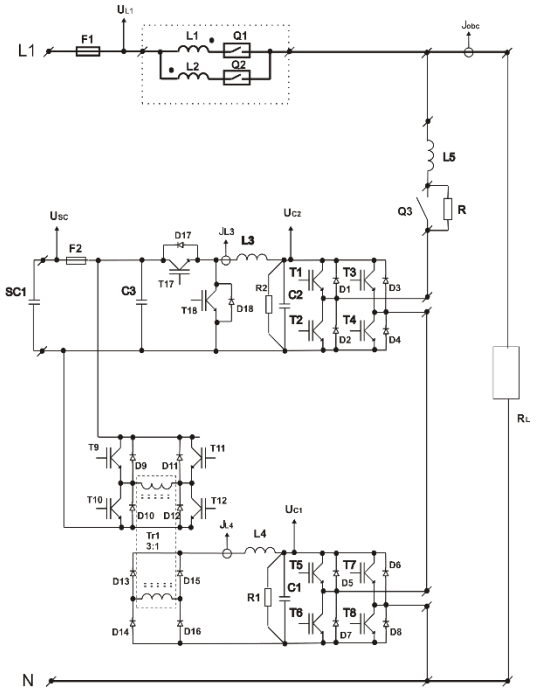


Fig.3. Schematic diagram of the one phase of the compensator.

a)

b)

Fig.4. A view of the three-phase compensator construction: a) front and back side, b) supercapacitors.

4. Identification of voltage dips

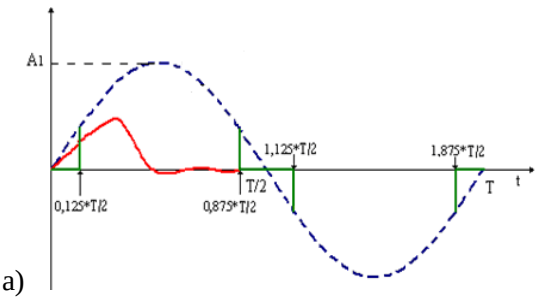
Fast switching devices or other sudden unexpected disturbances provoke habitually short failures or power outages in the network. These failures may appear at the moment of load on/off switching or as result of short circuits and they are of the stochastic nature. Generally (more than 90 %) these failures have a shape of voltage dips or short interruptions. In order to compensate them effectively they must be immediately detected or even if possible anticipated. The rapid diagnostics of the failure state is the elementary condition of the effective compensator performance what makes it possible to "rebuild" the voltage. However, methods faster than depicted in [7, 8] were not used because of independent controllers in each phase.

If detection of dips occurs when the network frequency and the time base (frequency) generated by the control circuit are synchronized than it is possible to determine the actual first harmonic voltage A_1 of the input signal $u_s(t)$. According to the formula (1) the amplitude A_1 is given:

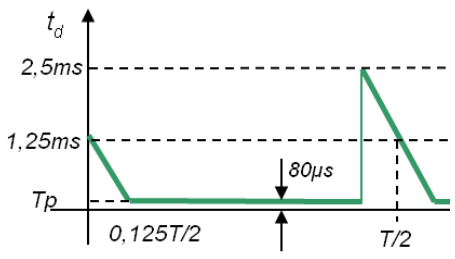
$$A_1 = \left| 2 \cdot \sum_{n=0}^{N-1} u_s(n) \cdot \sin(2\pi n / N) \right| \qquad (1)$$

where: $u_s(n)$ – n-th sample of the $u_s(t)$, n – sample index, N – number of input samples or frequency components of the discrete Fourier transform (DFT).

The idea of the actual and reference voltage comparison ("prediction") in an interval T is illustrated in Figure 5. The method of predicted voltage dips identification was described in details in [3]. The reference voltage sinewave is created as a predictive alternating voltage synchronized with the mains voltage that is with its fundamental harmonic. The comparison process occurs only in selected intervals of the period T. It is important that comparison results during short zero crossing intervals are not taken into consideration. The intervals in question have been adopted experimentally and set on the value of ± 1,25 ms that is ± 0,125 T (50 Hz). Analysing deviations of the instantaneous voltage outside zero crossing intervals results in that, in the worst case, a delay compensator response to a dip will be in maximum t_{opmax} = 2.5 ms (2 0,125 T/2, T = 20 ms). Nevertheless, the likelihood of such events during process comparison is small and the delay will relatively be comparable with the assumed cycle of sampling (e.g. T_p = 80 μs typically for 12,5 kHz). A parameter which better describes the possible delay of dip detections is the expected value. In the presented method this value could be estimated at approximately 0.39 ms as the average delay time waveform of variability shown in Figure 5b.



a)



b)

Fig.5. The detection mechanism: a) comparison of the real and predicted signals in the interval T (one period) and marked zones of measurement insensitivities; b) a way to estimation of average delay of the dip detection.

In the case of strong deformation of voltage waveform in the network the above described method may result in detection of dips even though the rms voltage is acceptable. In this case the predicted signal should take into account the most likely form of the forecast. Inclusion of an appropriate reference signal distortion can be obtained taking into account the higher harmonic components. The amplitudes of these components can be calculated using the conversion formula (1).

Effective dips detection, fast and highly immune to noise, requires the use of specialized algorithms, including the synchronization mechanism (described below) by FFT or wavelet transform. The main difference between the wavelet transform and DFT is that the first one operates in the time domain while the FFT in the frequency domain and uses variable window sizes to capture voltage changes. But practical implementation to the detection process is still difficult.

In [3] the dip detection mechanism was performing in two ways: exploring patterns of instantaneous value deviation and the r-m-s value of the measured waveform.

5. Synchronization with the mains voltage

In order to minimize transients after power outage of the main supply a replacement supply source (loss compensated) must have an amplitude and phase of the voltage compatible with pre-distortion waveform. Compensator controller provides synchronization of the internal reference voltage signal generator with voltage occurring during proper operation of the main power supply by means of phase locked loop (PLL). The applied software method of synchronization with the mains voltage is based on the use of DFT transforms signal us(t) into two orthogonal components of the formula:

$$\boldsymbol{U_s(m) = \sum_{n=0}^{N-1} u_s(n)\left[cos\frac{2\pi nm}{N} - jsin\frac{2\pi nm}{N}\right]}$$

$$\boldsymbol{U_s(m) = ReU_s(m) + jImU_s(m)} \quad (2)$$

where:

$U_s(m)$ – m-th component of the DFT,

m – output component index in frequency domain,

$u_s(n)$ – n-th sample of the input signal,

n – input sample index,

N – number of input samples or frequency components in the DFT.

If the signal $u_s(t)$ is an odd function of time and the period of input signal is T = Tp•N (Tp – sampling period, N – constant) then the real components of DFT will be zeroes:

$$\boldsymbol{U_s(m) = -j\sum_{n=0}^{N-1} u_s(n) sin\frac{2\pi nm}{N}} \quad (3)$$

In case of synchronization lack, when $T \neq Tp \bullet N$, where T is the period of the signal $u_s(t)$, the real component Re (U_s(m)) and imaginary component Im (U_s(m)) have nonzero values. The equation (3) describes the synchronization state of the odd components of the signal $u_s(t)$ with the sampling system. The compensator should synchronize the sampling system with the first harmonic of the grid voltage for m = 1. The angle between the vector $u_s(1)$ and the real axis is described by the formula:

$$\varphi(1) = arctan\frac{ImU_s(1)}{ReU_s(1)}. \quad (4)$$

The synchronization state can be obtained by changing the sampling period T_p in such a way that $(T - T_p \bullet N) \rightarrow 0$. Then the angle defined by formula (4) tends toward $\pi/2$. A simplified angle control system is shown in Figure 6. Only the real component of DFT is calculated and in this way the time-consuming calculation of the function *arctan*(φ) is omitted.

The output signal $S(t)$ is a synchronized time base common to all signal processing blocks of the digital controller, including dependent computational blocks generating control signals for transistor switches of the converter.

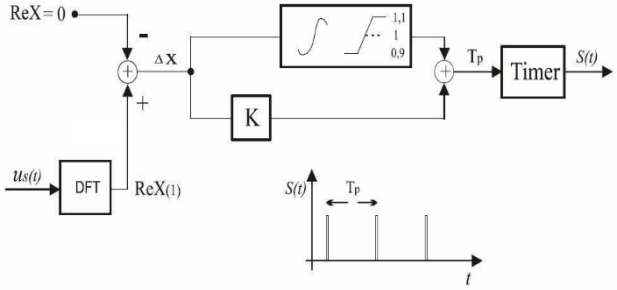


Fig.6. A simplified synchronization circuit (limited integration in the integrating element).

6. Power generation using cascade multilevel inverter

The cascade inverter allows for the generation of stepped output voltage [9, 10]. If the PWM method is not applied the instantaneous value of the output voltage is

$$\boldsymbol{U_F = U_g(nT_p)}. \quad (5)$$

The available voltages based on the DC link voltages U_4 and U_5 of the component inverters shown in Figure 5 are as follows: (U_5), (U_4 - U_5), (U_4), (U_4 + U_5), (- U_5), (-U_4 + U_5), (-U_4), (-U_4 -U_5), 0. The intermediate voltage values (between 0 and ± U_5) are obtained by using pulse width modulation (PWM) of the output stepped voltage.

During the dip occurrence the compensator should generate the desired reference voltage with amplitude and frequency according to the following equation:

$$U_{ref} = A_{1ref} sin\left(2\pi\frac{nT_p}{T}\right) \quad (6)$$

where A_{1ref} – referenced value of the first harmonic amplitude and T – network voltage period.

The calculation of the stepped voltage is possible in many ways. The final stepped voltage waveform depends on the ratio of voltages U_5/ U_4. The authors of work [9, 10], analysing the symmetrical three-phase cascade inverter (with equal voltage sharing in DC link circuits and without auxiliary DC converters as in the presented construction), pointed out the possibility of lowering the carrier frequency in proportion to the number of component inverters by using an unipolar sine-wave PWM modulation with a phase shift. An example of the voltage stepped waveforms in case the ratio U_5/ U_4 is ½ is presented in Fig. 7.

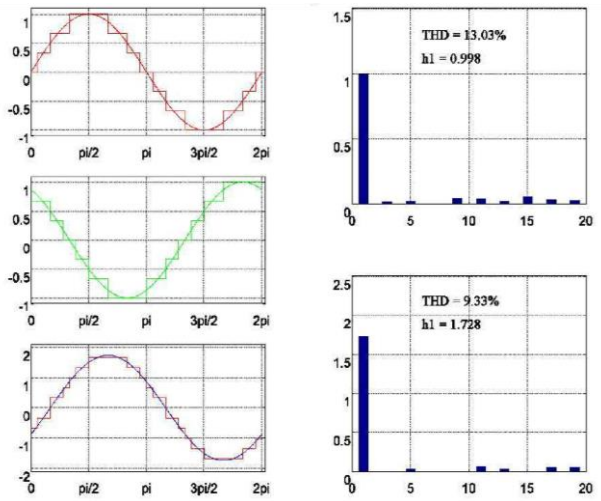


Fig. 7. Phase and phase-to-phase voltage and their spectra for the voltage ratio U_5/U_4 =1/2.

7. The voltage balance of the cascade converters

The simplified structure of one phase compensator is shown in Figure 3. For the asymmetrical cascade solution, it has been assumed that the ratio of converters DC link voltages is:

$$U_4/U_5 = 3. \quad (7)$$

This expression is derived directly from the principle of creating the stepped waveform in multilevel inverter with uniform gradation of the output voltage. This voltage balance for capacitors C_1 and C_2 is held in every working state by P_2 converter (Fig.2) approximating an idea depicted in [4]. When converters P_1 and P_2 are disconnected the balance between the voltages U_4 and U_5 is determined by the ratio of time constants of intermediate circuits R_1C_1 and R_2C_2.

Considering the condition (7) the calculation implementation in the microcontroller provides for inverters switching with carrier frequency ensuring the short-term output voltage U_F amplitude changes not exceeding $2U_5$. This limits the voltage stress for cascade inverter output semiconductors and determines the dimensions of the filter. Additionally, in standby state, while waiting for the voltage disturbance, the condition $U_5+U_4 > A_1$ should be executed, to assure the appropriate relationship between the grid voltage amplitude A_{1z} and the intermediate circuit voltage calculated according to equation (1). To achieve this the voltage U_5 is regulated using the inverter's F_2 zero vector and isolated converter P_2. In Figure 7 an example of current flow path during charging for positive polarization of the grid voltage is presented.

8. Description of the compensator algorithm

The operation of the compensator requires realization of multiple concurrent real-time control tasks. Six basic states of operation have been distinguished in the control algorithm:

STOP off – no mains power,

CHARGE C2 device is powered and supply voltage (U_s) is nominal. Capacitor C_2 is charged to the voltage $U_5 = 0.33A_1$, where A_1 is the first harmonic amplitude of the mains voltage,

CHARGE C1 device is powered and supply voltage (U_s) is nominal. Capacitor C_1 is charged to the voltage $U_4 = 0.8A_1$,

WAIT CHARGE Sc standby – waiting for dip or voltage outage, charging the supercapacitor S_c in given compensator's phase. The charger raises and maintains the level of the supercapacitor voltage at $U_{sc} = U_{p2} = 300$ V,

INVERTER based on the energy stored in supercapacitor Sc, the phase voltage is generated using the cascade inverter. The device enters this state after the identification of voltage dip or power failure.

In addition to the grid voltage measurement, waveforms synchronization, compensating voltage generation and regulation of energy flows between the grid, energy storage and load, the controller also supports communication with higher level control system using local or wide area network.

9. Experimental results

The stepped waveform of the cascaded inverter during experimental tests is presented in Figure 8. The referenced waveform of the voltage is denoted as u_Z while the phase voltage – u_{wy}. The control error is denoted as du and it determines the difference between the network and stepped voltage: $du = u_Z - u_{wy}$. The phase-to-phase voltage of the cascaded converter is also presented as the waveform E.

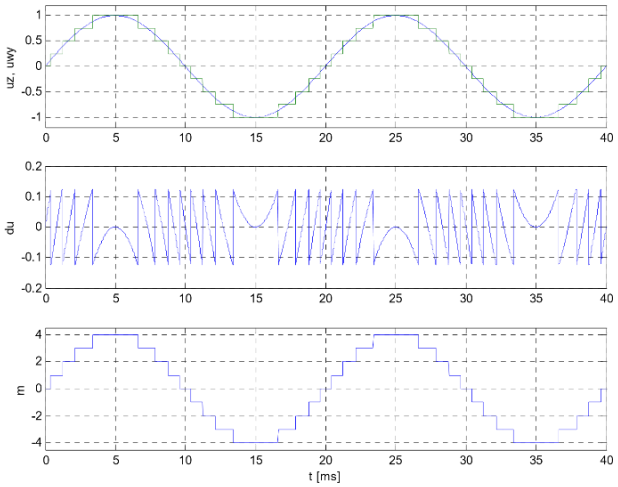


Fig. 8. The referenced voltage u_Z, – u_{wy}, the control error du and the phase-to-phase voltage – E.

During laboratory tests a low frequency PWM was added to the stepped voltage of the converter. The oscillogram presented in Figure 9 illustrates the PWM operation together with a stepped modulation, which form the output voltage waveform of the compensator.

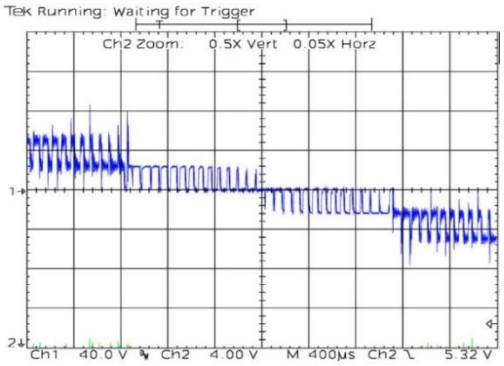


Fig. 9. The magnified view of the output waveform of the cascade inverter showing voltage modulation.

Next Figure shows the voltage waveforms illustrating the operation of the compensator in response to grid voltage disturbances.

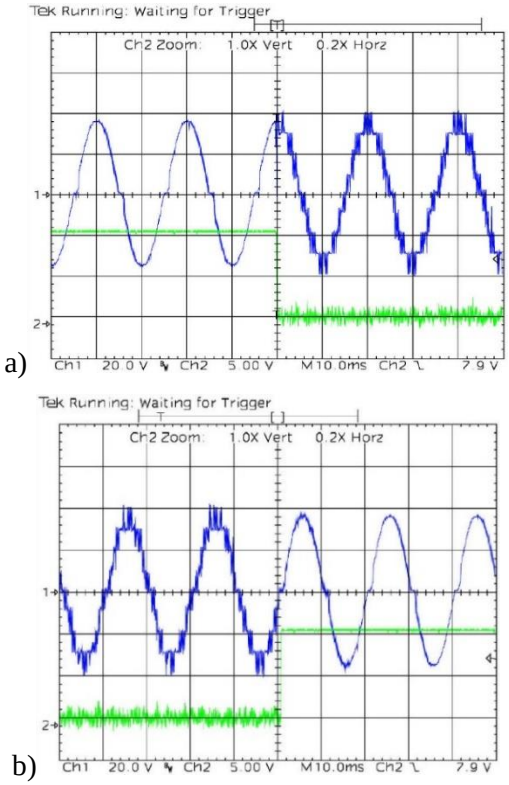


Fig.10. Laboratory test waveforms showing the start (a) and the end (b) of the voltage generation by the cascade inverter.

Figure 9 shows the voltage waveforms illustrating the process of the compensator reaction in response to grid voltage disturbances. The fast switching from network to supercapacitor storage supply is shown in Figure 10a and back switching after restoring the network voltage is shown in Figure 10b. The slight deformation of the obtained voltage around zero crossing points is caused by the properties of the thyristor switch K at low voltage.

10. Conclusion

A great and still escalating number of non-linear loads and growing share of energy from distributed resources result in decreasing the reliability of the public power grids. Therefore, the issues related to the improvement of the quality and reliability of the electrical energy supply are particularly important.

The presented compensator model allows for compensating dips and short-term interruptions in a three-phase four-wire grid. The device consists of three one phase cascade multilevel voltage converters. The high voltage stacked supercapacitors are used as energy storage for the compensator.

The usage of such an energy storage device has many advantages, but till now is not practically implemented in energetic supply systems, mainly because this technology is not widely known yet and high voltage supercapacitors are still very expensive.

The observed rapid progress in supercapacitors' technology will undoubtedly lead to mass production of these components with better parameters and much lower price, which will allow the wide usage of supercapacitor based compensators for protection of the sensitive processes and devices against interruptions or voltage dips in supply networks or for suppressing disturbances in networks with disruptive sources.

References

[1] Special Research Project COST/255/2006, Electrotechnical Institute, Report *IEl/OG, 2009,* Poland.

[2] D. Casadei, G. Grandi, C. Rossi, "A Supercapacitor-Based Power Conditioning System for Power Quality Improvement and Uninterruptible Power Supply", Proceedings of the 2002 IEEE International Symposium on Industrial Electronics, ISIE 2002.

[3] J. Iwaszkiewicz, P. Bogusławski, A. Krahel, E. Łowiec, „Three-phase Voltage Outages Compensator with Cascaded Multilevel Converter" – Archives of Electrical Engineering, Vol. 61, September 07, 2012, Poland, No. 3, pp. 325-336.

[4] J. Iwaszkiewicz, J. Perz, L. Wolski, M. Perez Donsión, "A Case Study Control on High Power Compensator of the Power Grid Irregularities for Industrial Appliances", International Conference on Renewable Energy and Power Quality ICREPQ'13, Bilbao, 20-22 March 2013, Spain.

[5] M. Newman, D. Holmes, J. Nielsen, F. Blaabjerg, "A Dynamic Voltage Restorer (DVR) With Selective Harmonic Compensation at Medium Voltage Level", IEEE Transaction On Industry Applications, Vol. 41, No. 6, November/December 2005.

[6] L. Maharjan, S. Inoue, H. Akagi, "A Transformerless Energy Storage System Based on a Cascade Multilevel PWM Converter With Star Configuration", IEEE Transactions on Industry Applications, Vol. 44, No. 5, September/October 2008.

[7] C. Fitzer, M. Barnes, P. Green, "Voltage Sag Detection Technique for a Dynamic Voltage Restorer", IEEE Transaction On Industry Applications, Vol. 40, No. 1, January/February 2004.

[8] B. Bae, J. Jeong, J. Lee, B. Han, "Novel Sag Detection Method for Line-Interactive Dynamic, Voltage Restorer", Power Engineering Letters, IEEE Transactions on Power Delivery, Vol. 25, No. 2, 2010.

[9] J. Iwaszkiewicz, J. Perz, "Mathematical Approach to THD Optimisation in Multilevel Convertors", International Conference on Renewable Energy and Power Quality ICREPQ'06, Palma de Mallorca, Hiszpania, 2006.

[10] J. Iwaszkiewicz, J. Perz, "A Novel Approach to Sine-wave Approximation in Multilevel Converters", The IEEE Industry Applications Society Workshop on Renewable Energy Based Units and Systems (REBUS), St. Petersburg, Russia, 2006.