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# Analysis of Three-Phase Four-Wire Shunt Active Power Filter Topologies Implemented Using Single-Phase Full-Bridge Inverters

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**Abstract.** This paper presents a comparative analysis involving two different topologies of three-phase four-wire shunt active power filters (SAPFs), such that load current harmonic suppression, as well as load reactive power compensation are carried out, resulting an effective power factor improvement. Both SAPF topologies use three single-phase full-bridge (1P-FB) inverter units. In the first, named 3FB-C-DC-Bus topology, the 1P-FB inverters share a common DC-bus voltage, while in the second, named 3FB-I-DC-Bus topology, each 1P-FB inverter unit has an independent dc-bus. Independent current control strategy is adopted for computing the current references of each inverter unit, meaning that the grid currents can be individually controlled. In other words, the three-phase system can be treated as three independent single-phase systems. Apart from accomplishment of static and dynamic performance evaluations, which are performed by means of computational simulations, the amount of passive and active devices needed to build both the SAPF structures is also measured and evaluated. As a result, the best decision for choosing the structure with the best cost-effectiveness is allowed.

## Key words

Shunt Active Power Filters, Full-Bridge Inverters, Power Quality.

## 1. Introduction

In recent years, power quality has become an important concern among consumers and power supply companies due to the proliferation of power electronics devices, resulting in the increase use of nonlinear loads [1]. Such loads have contributed to worsen the power quality in the electrical power systems due to the high level of harmonic current components drained from the utility grid, occasioning distorted utility voltages. Furthermore, in three-phase four-wire systems, even when balanced nonlinear loads are connected to the grid, the third order harmonic current component and its multiples (zero sequence components) go through the neutral conductor, resulting in a potentially harmful condition [2]-[4].

In order to mitigate the aforementioned problems, shunt active power filters (SAPFs) have been employed [4]. In particular, SAPFs are able to suppress load harmonic currents, as well as compensate both reactive power and load unbalances [5],[6]. As a consequence, considering an ideal operation condition, the grid currents become sinusoidal, balanced and in phase with the grid voltages, such that an effective power factor correction is achieved.

Three single-phase full-bridge (1P-FB) inverters sharing a common dc-bus voltage have been employed to construct a shunt active power filter (SAPF), as shown in Fig. 1 (a) [4],[6]. In this paper, this SAPF configuration is called 3FB-C-DC-Bus topology.

In [7], two different control strategies have been employed to perform the active power-line conditioning. In the first strategy, load unbalance compensation could be obtained, while in the second the active conditioning has been achieved by controlling the 1P-FB inverter units individually per-phase. On the other hand, although the 3FB-C-DC-Bus filter topology allows load unbalance compensation, three coupling transformers are mandatorily required to isolate the utility grid of the active filter, in order to avoid short circuits.

To overcome this inconvenient, each 1P-FB inverter unit can be individually controlled by means of its own dc-bus voltage. As a consequence, the use of the coupling transformers is not required, as shown in Fig. 1 (b). In this paper this SAPF configuration is called 3FB-I-DC-Bus topology.

This paper presents a comparative analysis involving the 3FB-C-DC-Bus and the 3FB-I-DC-Bus topologies, where the independent current control strategy (ICCS) is adopted for computing the current references of each inverter unit. In this case, the three-phase system can be treated as three independent single-phase systems, such that the grid currents can be individually controlled.

Furthermore, the advantages and disadvantages related to the SAPFs topologies are highlighted.

This paper is organized as follows: In Section 2 the SAPF topologies are described. The algorithms used to generate the inverters current references, which are based on the synchronous reference frame (SRF) are presented and discussed in Section 3. Computational simulation results are presented in Section 4, in order to evaluate the static and dynamic performances of the SAPFs. In this section is also presented a comparison based on the amount of passive and active devices needed to build both the SAPF structures. Finally, the conclusions are presented in Section 5.

## 2. SAPF Topologies

The power circuits of the three-phase SAPF topologies studied in this paper are shown in Fig. 1.

Fig. 1 (a) presents the 3FB-C-DC-Bus filter topology, which is composed of three 1P-FB inverter units, a dc-bus capacitor, three filtering inductors and three single-phase coupling transformers. As can be noted, the 1P-FB units share the same dc-bus, whose voltage must be maintained controlled at a constant value by using a voltage control loop. As aforementioned, the transformers are needed to avoid short circuit between the utility grid phases. An important aspect to be considered is the adoption of independent current control involving the three phases. In this case, each inverter unit has its own current control loop and proper algorithm to compute the compensation current references.

Fig. 1 (b) presents the 3FB-I-DC-Bus filter topology, which is composed of three 1P-FB inverter units, three dc-bus capacitors and three filtering inductors. As can be noted, since the 1P-FB units do not share the same dc-bus, three control loops are needed to maintain the dc-bus voltages controlled. Thus, the 1P-FB inverters are connected to the grid by means of only coupling inductors. In this case, isolation transformers are not required. Similar to the 3FB-C-DC-Bus topology, ICCS is employed, where each inverter unit has also its own current loop, as well as proper algorithm to compute the compensation current references. On the other hand, two additional voltage control loops are needed.

As can be noted, since independent current controls are employed in both SAPF structures, only harmonic currents are removed from the neutral conductor. Thus, if load unbalance exists, only the current component at fundamental frequency goes through the neutral wire.

## 3. Generation of Current References and Control Strategies

In this section, the algorithms used to generate the compensation current references, as well as the dc-bus voltage and ac current control loops are presented.

*A. SRFs Currents References*

The SRF-based algorithm has been firstly conceived to be employed in balanced three-phase systems. Since independent current control strategy is adopted in this work, such that the three-phase system is being treated as three single-phase systems, the conventional SRF-based algorithm must be properly adapted to compute the compensation current references for each inverter unit. Therefore, each SAPF topology will employ three independent single-phase SRF-based algorithms to perform suppressing of load harmonic currents and compensation of load reactive power. In this case, the compensation of the load unbalances at fundamental frequency is not taken into account.

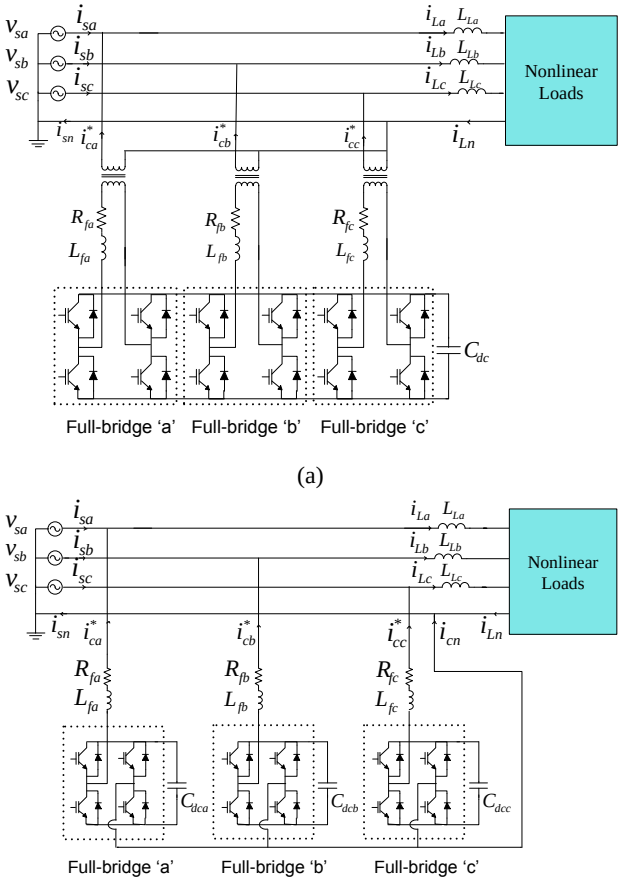



Fig. 1. SAPF Topologies: (a) 3FB-C-DC-Bus SAPF topology; (b) 3FB-I-DC-Bus SAPF topology.

Figs. 2 (a) and (b) present the SRF-based algorithms adopted in the 3FB-C-DC-Bus and 3FB-I-DC-Bus topologies, respectively. Firstly, the single-phase SRF-based algorithm consists in creating a fictitious three-phase system, which can be represented into the two-phase stationary reference frame ( $\alpha\beta$ -axes) [8]. For this purpose, the load currents ($i_{L(a,b,c)}$) are measured and treated as three fictitious currents in the $\alpha$ coordinates ($i_{\alpha(a,b,c)}$). After that, $\pi/2$ radians phase delay is added to $i_{\alpha(a,b,c)}$, creating three new fictitious currents in $\beta$ coordinates ($i_{\beta(a,b,c)}$), as represented by (1). After that, $i_{\alpha(a,b,c)}$ and $i_{\beta(a,b,c)}$ are transformed into the SRF *dq*-

axes as given in (2), where $\cos\theta$ and $sin\theta$ represent the coordinates of the synchronous unit vector, which are estimated by means of a phase-locked-loop (PLL) system for ensuring the synchronism between the compensation currents and the utility grid voltages [9]. The single-phase PLL system used in this work has been described in detail in [10].

$$\begin{bmatrix} i_{\alpha(a,b,c)} \\ i_{\beta(a,b,c)} \end{bmatrix} = \begin{bmatrix} i_{L(a,b,c)}(\omega t) \\ i_{L(a,b,c)}(\omega t - \pi/2) \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} id_{(a,b,c)} \\ id_{(a,b,c)} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{\alpha(a,b,c)} \\ i_{\beta(a,b,c)} \end{bmatrix} \quad (2)$$

The *dq* currents ($id_{a,b,c}$ and $iq_{a,b,c}$) are composed of dc and ac components, where the fundamental load currents are represented by dc components, whereas the harmonics currents are represented by ac components. Thereby, the dc components can easily be obtained using low pass filters (LPF) resulting in the quantities $id_{dc(a,b,c)}$, as shown in Fig. 2.

The currents $i_{dc}$ and $i_{dc(a,b,c)}$ presented in Fig. 2 (a) and (b), respectively, represent the output of the dc-bus proportional-integral (PI) voltage controllers, where *Kpv* and *Kiv* are the proportional and integral gains, respectively. Once the inverters share the same dc-bus, in 3FB-C-DC-Bus topology the dc-bus PI output must be divided by 3 resulting the current $i_{dc}$, which is added to the respective *d-axis* of the SRF-based algorithm, as shown in Fig. 2 (a). On the other hand, in 3FB-I-DC-Bus topology, the currents $i_{dc(a,b,c)}$ are the output signal of each dc-bus PI controller, as shown in Fig. 2 (b).

The quantities $i_{dc}$ and $i_{dc(a,b,c)}$ represent the active currents drained from the grid needed to maintain the dc-bus voltage at a constant reference ($V_{dc}^{*}$). In other words, $i_{dc}$ and $i_{dc(a,b,c)}$ compensate the losses related to the switching devices, and the passive filtering elements, as well.

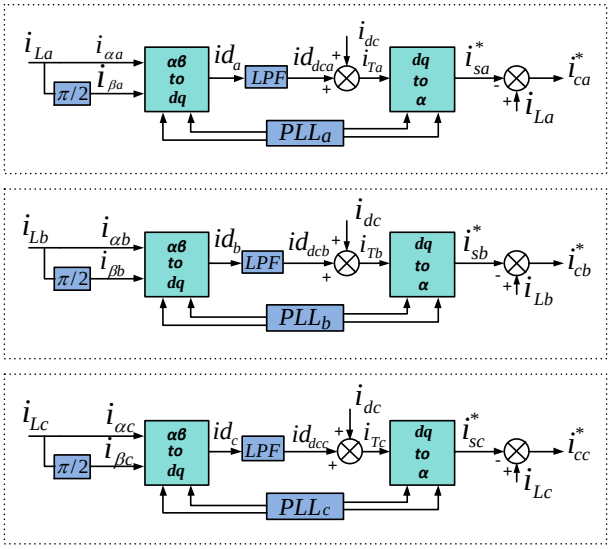
Thus, the fundamental frequency reference currents can be obtained by (3). Finally, the compensation current references ($i_{ca}^{*}, i_{cb}^{*}, i_{cc}^{*}$) are achieved by (4), where the load harmonic and reactive current components are included.

$$i_{s(a,b,c)}^{*} = (id_{dc(a,b,c)} + i_{dc(a,b,c)})\cos\theta_{a,b,c} \quad (3)$$

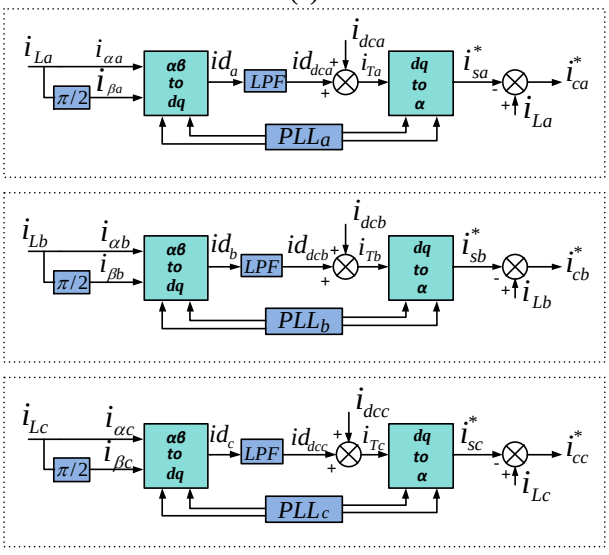
$$i_{c(a,b,c)}^{*} = i_{L(a,b,c)} - i_{s(a,b,c)}^{*} \quad (4)$$

*B. Current and Voltage Control Loops*

Figs. 3 (a) and (b) present the block diagrams of the current controllers used to control each inverter unit in the respective 3FB-C-DC-Bus and 3FB-I-DC-Bus topologies, where the current references are achieved from the SRF-based algorithms presented previously. In addition, $L_{eq(a.b,c)}$ and $R_{eq(a,b,c)}$ presented in Fig. 3 (a) are, respectively, the equivalent inductances and resistances.



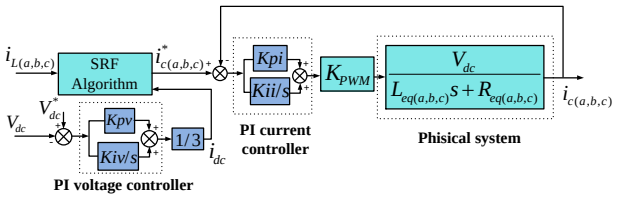

(a)



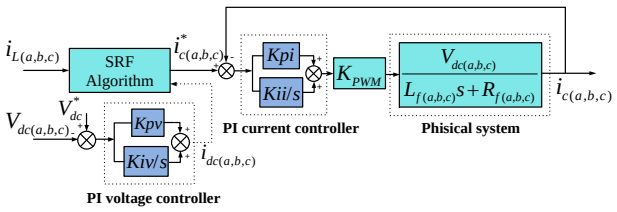

(b)

Fig. 2. Single-phase SRF-based algorithms: (a) 3FB-C-DC-Bus SRF-based algorithms; (b) 3FB-I-DC-Bus SRF-based algorithms.

The equivalent inductances $L_{eq(a,b,c)}$ are composed of the sum of the filtering inductances ($L_{f(a,b,c)}$) and the transformer leakage inductances ($L_{t(a.b.c)}$), and the equivalent resistances $R_{eq(a,b,c)}$ are the total resistances obtained by the sum of the transformer leakage resistances ($R_{t(a,b,c)}$) and the filtering resistances ($R_{f(a,b,c)}$). As can be noted in Fig. 3 (b), only the filtering inductor inductance ($L_{f(a,b,c)}$) and the resistance ($R_{f(a,b,c)}$) are taken into account to represent the physical system of the SAPFs. The PWM gain ($K_{PWM}$) is calculated considering the peak amplitude of the PWM triangular carrier signal [11].




(a)




(b)

Fig. 3. Block diagrams of the current and voltage controllers: (a) 3FB-C-DC-Bus diagram; (b) 3FB-I-DC-Bus diagram.

The per-phase closed loop transfer functions for the diagrams shown in Figs. 3 (a) and (b) are given by (5) and (6), respectively, where the PI current controllers are responsible to control the currents synthetized by the inverter units. The proportional and integral gains, $K_{pi}$ and $K_{ii}$, are determined using the modelling and design procedures presented in [12].

$$\frac{i_{c(a,b,c)}(s)}{i^*_{c(a,b,c)}(s)} = \frac{K_{PWM}\, V_{dc}(K_{pi}s + K_{ii})}{L_{eq(a,b,c)}s^2 + (K_{pi}\, K_{PWM}V_{dc} + R_{eq(a,b,c)})s + K_{ii}\, K_{PWM}V_{dc}} \quad (5)$$

$$\frac{i_{c(a,b,c)}(s)}{i^*_{c(a,b,c)}(s)} = \frac{K_{PWM}\, V_{dc(a,b,c)}(K_{pi}s + K_{ii})}{L_{f(a,b,c)}s^2 + (K_{pi}\, K_{PWM}\, V_{dc(a,b,c)} + R_{f(a,b,c)})s + K_{ii}\, K_{PWM}\, V_{dc(a,b,c)}} \quad (6)$$

## 4. Simulation Results

The topologies presented in Figs. 1 (a) and (b) are evaluated by means of computational simulation using a MATLAB/Simulink® tool, in which both topologies were considered a three-phase four-wire system feeding three unbalanced nonlinear loads whose parameters are shown in Table I. The approach used for tuning the PI dc-bus and PI current controllers is performed using the frequency response method based on Bode diagrams, where the phase margin and 0dB gain crossover frequency where adopted as project specifications. Table II presents the tuning parameters and gains of the controllers, whereas Table III summarises the parameters of the SAPF topologies.

Table I. - Load parameters.

| Phases | Unbalanced Nonlinear Loads | Load Resistances (R) | Load Inductances (L) |
|---|---|---|---|
| 'a' | Single–phase rectifier | 6.4Ω | 80mH |
| 'b' | Single–phase rectifier | 7.5Ω | 45mH |
| 'c' | Single–phase rectifier | 9.4Ω | 57mH |

Table II. – Tuning parameters and gains of the PI controllers.

| Design specifications | 3FB-C-DC-Bus | 3FB-I-DC-Bus |
|---|---|---|
| Crossover frequency (PI current controller) | ω=15707.96 rad/s | ω=15707.96 rad/s |
| Desired phase-margin (PI current controller) | *MF* = 55º | *MF* = 53º |
| Crossover frequency (PI voltage controller) | ω=150.7rad/s | ω=150.7rad/s |
| Desired phase-margin (PI voltage controller) | *MF* = 88º | *MF* = 88º |
| PI current controller gains | *Kpi* = 0.0728<br>*Kii* = 812.646 | *Kpi* = 0.0679<br>*Kii* = 812.748 |
| PI dc-bus controller gains | *Kpv* = 0.2715<br>*Kiv* = 1.4298 | *Kpv* = 0.2030<br>*Kiv* = 0.6695 |

Table III. - Parameters used in the computational simulation of the SAPFs.

| Parameters | 3FB-C-DC-Bus | 3FB-I-DC-Bus |
|---|---|---|
| Noninal voltage rms utility grid | $Vs_{a,b,c}$ = 127 V | $Vs_{a,b,c}$ = 127 V |
| Noninal frequency utility grid | $f$ = 60 Hz | $f$ = 60 Hz |
| Inductors | $L_{La,b,c}$ = 1.5mH | $L_{La,b,c}$ = 1.5mH |
| Filtering inductance | $L_{f\,a,b,c}$ = 2.5mH | $L_{fa,b,c}$ = 2.5mH |
| Filtering resistance | $R_{f\,a,b,c}$= 0.21 Ω | $R_{f\,a,b,c}$= 0.21 Ω |
| Dispersion inductance of transformers | $L_{ta,b,c}$ =115uH | none |
| Dispersion resistence of transformers | $R_{ta,b,c}$ = 0.08 Ω | none |
| Swiching frequency PWM | $f_{sw}$ = 20 KHz | $f_{sw}$ = 20 KHz |
| PWM gain | $K_{PWM}$ = 2 | $K_{PWM}$ = 2 |
| DC-bus voltage | $V_{dc}$ = 230 V | $V_{dca,b,c}$ = 230 V |
| DC-bus capacitor | $C_{dc}$ = 2115uF | $C_{dca,b,c}$= 2115uF |

The simulation results for both SAPF topologies operating with independent current control strategy are presented in Figs. 4 to 7. Figs. 4 and 5 show the load currents ($i_{La}, i_{Lb}, i_{Lc}$), the compensation currents ($i_{ca}, i_{cb}, i_{cc}$), the compensated grid currents ($i_{sa}, i_{sb}, i_{sc}$) and their respective neutral currents ($i_{Ln}, i_{cn}, i_{sn}$) for 3FB-C-DC-Bus and 3FB-I-DC-Bus topologies, respectively. As can be noted, due to load unbalanced condition, the current component at

fundamental frequency remains going through the neutral wire ($i_{sn}$), meaning that harmonic suppressing and reactive power compensation were performed.

The total harmonic distortion (THD) of grid currents are presented in Table IV. As can be noted, the THDs of the grid currents were strongly reduced.

Fig. 6 shows the dc-bus voltage for the 3FB-C-DC-Bus topology. As can be observed, the dc-bus voltage is controlled to a constant reference of 230 V and presents a voltage ripple of 360 Hz. The three dc-bus voltages of the 3FB-I-DC-Bus topology is presented in Fig. 7. They also were maintained at a reference values of 230 V but present voltage ripples of 120 Hz.

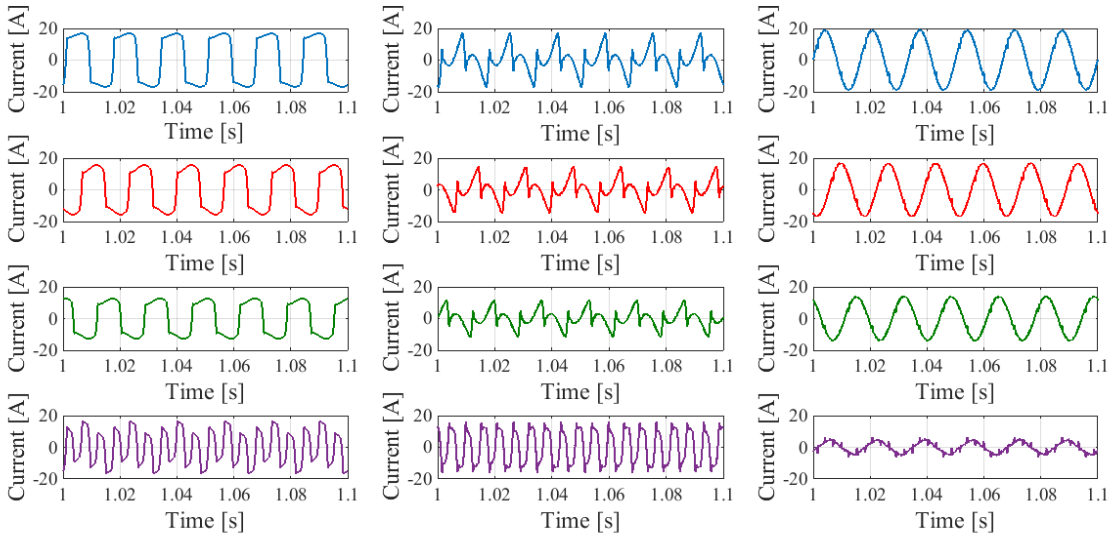



Fig. 4. 3FB-C-DC-Bus: (a) Load and neutral currents; (b) Compensation currents; (c) Grid and neutral currents.

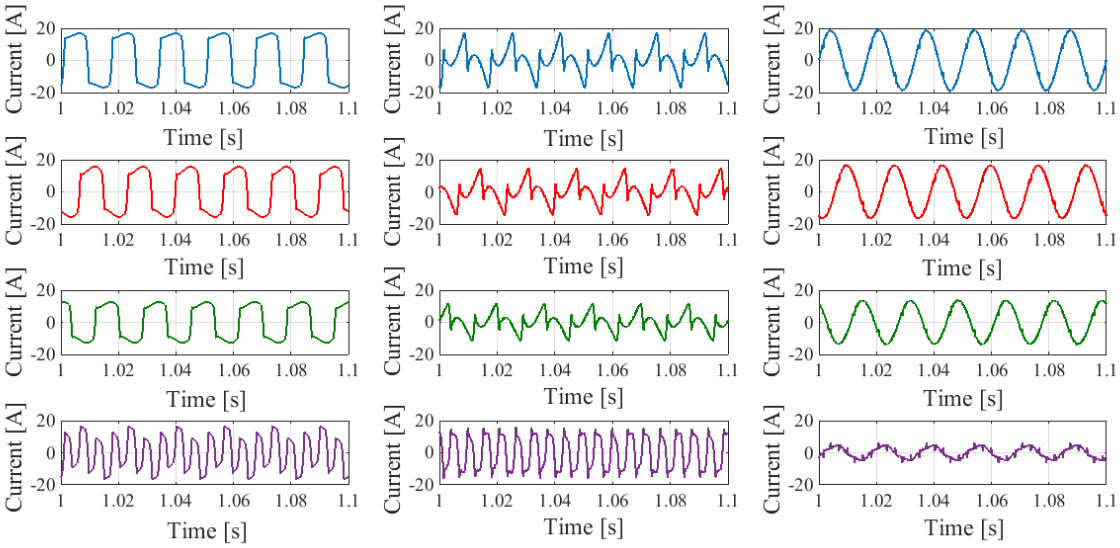



Fig. 5. 3FB-I-DC-Bus: (a) Load and neutral currents; (b) Compensation currents; (c) Grid and neutral currents.

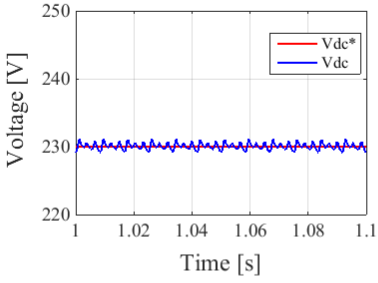
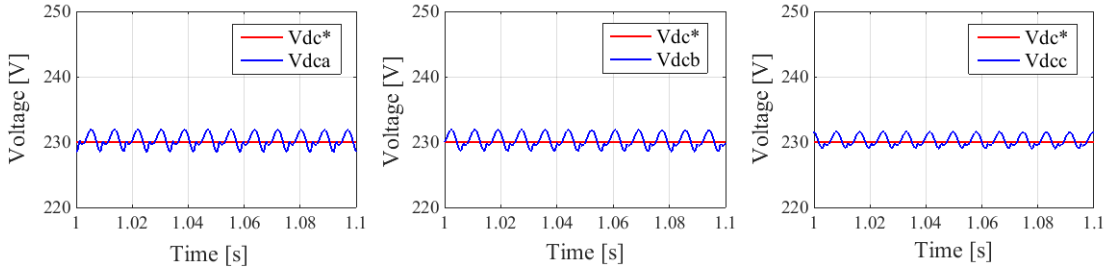



Fig. 6. DC-bus voltage of the 3FB-C-DC-Bus topology.

Table IV. - Total Harmonic Distortion of the Grid Currents.

| System | Total Harmonic Distortion (%) | | |
|---|---|---|---|
| | phase *a* | phase *b* | phase *c* |
| Without compensation | 33.99 | 30.83 | 32.23 |
| 3FB-C-DC-Bus | 4.10 | 4.18 | 4.66 |
| 3FB-I-DC-Bus | 3.88 | 4.01 | 4.49 |




(a) (b) (c)

Fig. 7. DC-bus voltages of the 3FB-I-DC-Bus topology: (a) Phase "a"; (b) Phase "b"; (c) Phase "c".

Based on the simulation results, in Table V are listed the differences observed between the two SAPF topologies. It takes into account the ability of the SAPF topologies to perform harmonic current suppression, the number of passive and active devices required to build both SAPF structures, the dc-bus voltage behavior and overall costs.

Table V. - Comparative analysis between the SAPF topologies

| Requirements | 3FB-C-DC-Bus | 3FB-I-DC-Bus |
|---|---|---|
| Number of switching devices | 12 | 12 |
| Number of coupling transformers | 3 | None |
| Number of Filtering inductors | 3 | 3 |
| Number of dc-bus capacitors | 1 | 3 |
| Harmonic suppression capability | Good | Better |
| Grid Current THD % | Less than 5% | Less than 5% |
| dc-bus voltage ripple | 1.8% | 1.9% |
| Overall cost | High (due to transformers use) | Medium |

## 5. Conclusions

This paper presented a comparative analysis between two SAPF topologies employing 1P-FB inverter units, which were named 3FB-C-DC-Bus and 3FB-I-DC-Bus. The topologies were applied to perform load current harmonic suppression and load reactive power compensation in three-phase four-wire systems. Both topologies adopted independent current control strategy for computing the current references of each inverter unit. For this purpose, single-phase SRF-based algorithms were used to generate the current references. Thus, it was possible to adopt independent control for each phase of the three-phase four-wire system. Although the 3FB-C-DC-Bus filter topology also allows to perform load unbalance compensation, three additional coupling transformers are mandatorily required, increasing the overall cost. On the other hand, once the 3FB-I-DC-Bus topology uses three independent dc-bus, if one or two 1P-FB inverter unit fail, the SAPF can continue to operate normally. Thus, whether load unbalance compensation is not required, the 3FB-I-DC-Bus topology is more attractive than the 3FB-C-DC-Bus topology, once the cost-effectiveness is better.

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