A New Concept of Power Quality Monitoring

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Abstract. The concept of power quality monitoring is related with the detection of voltage events in the mains network. The characterization of these voltage events results from standards that define several limits for their amplitudes, duration and maximum number of occurrences within a time period. In the last three decades, the loads connected to the mains network suffered great changes. The number of electronic and sensitive equipment increased considerably, and the old concepts of monitoring are not representative for these loads. This paper presents a new concept of power quality monitoring, related with the susceptibility of sensitive loads. The authors identify the sensitive loads connected to the mains network and develop a study of their susceptibility to voltage perturbations in the mains network. Seven voltage events are defined and a Power Quality Monitor prototype is presented.

Key words

Power Quality, Power Supplies, Susceptibility, Voltage Events, Electronic Equipment, Sensitive Loads.

1. Introduction

The economical impact in industrial environment as a consequence of an electrical failure, introduces the study of power quality, and power quality monitoring. The main preoccupation of producers and consumers is the avoidance of any electrical energy failure and the maintenance of the RMS mains voltage inside the range of ±10% of the nominal voltage, according to the limits defined by standard EN50160. The commercial power quality monitors consider these aspects. The events detected are typically: counting the duration and the number of occurrences of electrical failures and the deviations of the RMS mains voltage. Typically the events detected have a duration superior to one period of mains voltage, 20ms.

In the past loads like lamps, 50Hz transformers, induction motors and heating resistances, were the loads connected to the mains network. The concepts of power quality and monitoring are related with their susceptibility. The new electronic loads are much more sensitive then the ones referred. Voltage transients, with short duration (less than 10ms), in the mains voltage can damage those equipments. It is true that an electrical failure may represent a severe economical impact. However the damage on sensitive equipment, present in the production process, can have the same or worse impact, as consequence of voltage transients, particularly if this equipment remains damaged. Considering the relative economic impact of power quality failures, a different approach to power monitoring is introduced in this paper. This paper presents a study of the sensitive loads to the mains network together with the identification of the voltage events present in the mains network that are related with their susceptibility. In this paper V_I represents the mains voltage amplitude.

2. Sensitive Equipment

Nowadays a great part of the electric loads have an electronic circuit in their conception. This electronic circuit can be a controller, a power converter, etc. The interface between the mains network and these electronic circuits is usually a power supply or an AC-DC converter. In the last three decades these power supplies were built with a 50Hz transformer to reduce the amplitude of the mains voltage and to guarantee galvanic isolation, and also with a single phase rectifier and a filter capacitor to obtain output continuous current. To achieve output regulation a linear regulator was used. Fig. 1 shows this type of power supply, where I_O represents the current in the load.

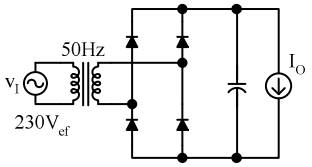

Fig. 1 Configuration of a traditional AC-DC power supply.

This solution presents the disadvantages related with the low frequency (50Hz) transformer: large dimensions, high weight and cost. In addition, due to linear regulation the overall efficiency was low (<50%). To solve these problems this type of power supply has been replaced by switch mode power supplies (SMPS). The SMPS realizes isolation with a high frequency ferrite transformer actuated with a DC-AC square wave converter, or inverter, and due to the switching process presents higher efficiency. Fig. 2 shows the basic building blocks of a SMPS.

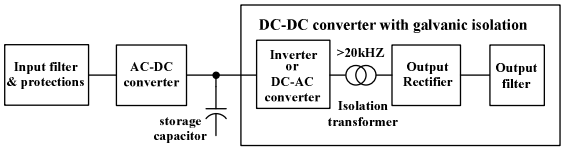

Fig. 2 Building blocks of a SMPS.

The SMPS with their good characteristics, high efficiency, low cost and weight and reduced dimensions, are extensively used in industrial, professional and domestic environment. There are still other loads as inductive motors, lamps or heating resistances that do not use a SMPS in their conception. Due to their associated inertia, these loads are not sensitive to voltage transients. The SMPS constitutes, therefore, the main and the most sensitive load that is present in the mains network. This way, the study of the susceptibility of sensitive loads to perturbations in the mains network is based on the study of the SMPS.

3. Switch Mode Power Supplies (SMPS)

This section describes the functions of the building blocks presented in Fig.2.

The DC-DC converter regulates the output voltage and guarantees the galvanic isolation between the input and output voltages of the SMPS. As an example, Fig. 3 shows a full-bridge DC-DC converter with galvanic isolation.

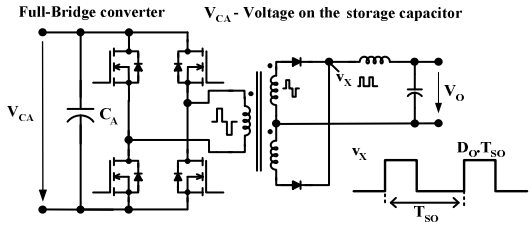

Fig. 3 Isolated full-bridge converter with output rectifier and LC filter – the power circuit topology is used in medium and high power SMPS.

For medium power (P < 500W) the switching frequency, f_C, is normally less than 100kHz. The output LC filter is designed to obtain a good attenuation at the switching frequency. In general, the output ripple voltage is less than 1% of the output voltage. This condition constrains the cutoff frequency, f_C, of the output filter. Typically, the cutoff frequency is 30 or 100 times less than the switching frequency, f_S, in order to guarantee a good attenuation. Equivalent series resistor (ESR) and equivalent series inductance (ESL) present in the output capacitor must be considered in the output filter design. Sometimes it is necessary to use a double LC filter due the effect of the ESR and ESL. Fig. 4 shows the influence of the ESR in the attenuation of a double LC output filter. The values presented in Fig. 4 result from a commercial PC SMPS, with an internal switching frequency of 66 kHz. The value of ESR is 68mΩ, measured with an impedance analyzer HP4294.

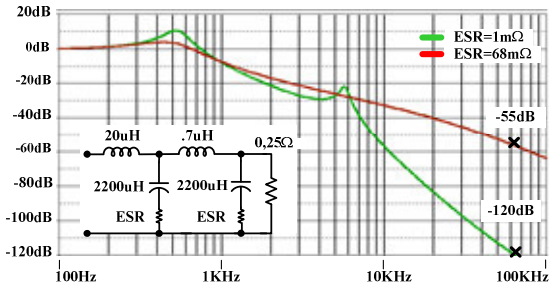

Fig. 4 Influence of ESR in the attenuation of the output filter.

The output voltage control is usually achieved by a pulse width modulator PWM and PI regulator and may be realized in voltage mode or current mode control. The current mode control presents better performance but is more expensive and is used only in high performance equipments or industrial equipments. Alternatively, the voltage mode control is the most common voltage controller used in domestic applications. Fig. 5 shows an output voltage controller working in voltage mode.

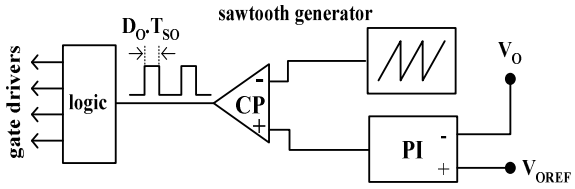

Fig. 5 Output voltage controller in voltage mode.

To guarantee the stability of the controller and the high gain at low frequency (<1kHz), the time response of the control is quite slow (0,2 - 1ms). The output duty ratio D_O adopted is normally 0,5 to 0,7, to allow a low-volt transient in V_{CA}.

Several topologies of DC-DC converters are used in SMPS. All of them present a high frequency transformer that is required in order to obtain galvanic isolation and voltage adaptation, as well. The physical size of those transformers is an important factor on the SMPS manufacturing costs. The size reduction and leakage induction minimization imply a considerable leakage capacitance between primary and secondary. The number of primary turns is minimized. Typically, the transformer has a safety security of 25% into the magnetization current.

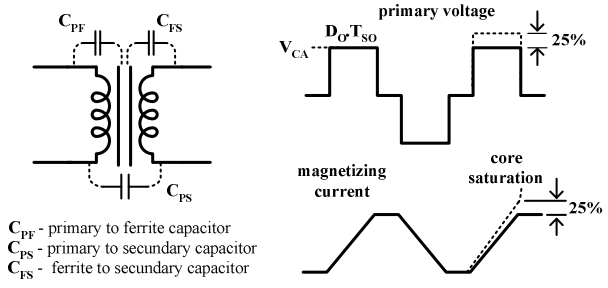

Fig. 6 Transformer leakage capacitors and core saturation.

The AC-DC conversion is usually obtained with a diode bridge and capacitive filtering, C_A. The output voltage is approximately equal to the peak voltage of the mains input. The storage capacitor is designed to guarantee a voltage interruption of 20ms up to 30ms (hold-up time or stand-on time), without any variation in the output voltage, V_O. These criteria result on a residual AC component less than 5% of the peak value in C_A. The storage capacitors are large electrolytic capacitors, performing a good filtering effect at 100Hz. Their ESR and ESL are very large. Consequently, their impedance rises for frequencies above some few kHz (1-10kHz), resulting in a very poor filtering at higher frequencies.

When the storage capacitor is discharged, and the power supply turned on, the peak value of the input current is extremely high and must be limited. Most manufacturers use a Negative Thermal Coefficient (NTC) resistor prior to the AC-DC converter (Fig.7). During the first seconds of operation the NTC warms up and its resistance decreases considerably and does not affect the SMPS efficiency (typically 1% of losses).

Some equipments complying with EN61000 standard, use a boost converter, Fig. 7, in order to perform input current waveshapping. In this case the DC voltage is 15% to 25% higher than the mains input voltage peak value (360-400V, for 230V AC input).

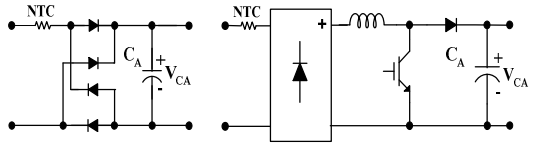

Fig. 7 AC-DC conversion in a SMPS, without and with input current waveshaping.

The use of this auxiliary converter introduces the regulation of the storage capacitor voltage, which remains almost independent of the mains voltage. The boost converter permits the operation of the SMPS in the extended range input (80-240Vrms). This converter is very insensitive to the input voltage disturbances.

The input filter (RFI filter) is intended to suppress radio frequency noise that results from transistor switching in the DC-AC converter. Typically, it presents an attenuation of 30 to 50dB, at frequencies above 1 to 5MHz and is designed to operate with noise amplitudes up to 1 to 5mV. Fig. 8 shows some topologies of RFI filters.

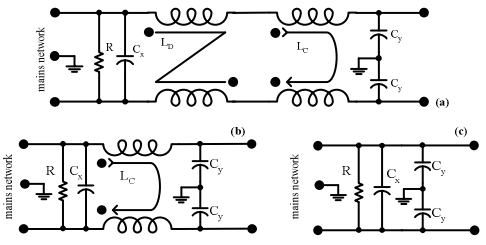

Fig. 8 Topologies of RFI filters.

The transformers formed by the inductances L_D an L_C, presented in Fig.8, are for differential mode and common mode noise rejection, respectively. The capacitors C_X and C_Y are very small, typically C_X<100nF and C_Y<10nF. These capacitors are designed to present low impedance at frequencies higher than 1MHz and to supported high voltage transients. These capacitors are subject of several tests, described in the standards IEC60384-14 and EN132400. For steady state operation, the CX and CY capacitors support 135% and 185% of V_I, respectively.

The topology of RFI filter and the components values are dependent of the noise emitted by the SMPS. As a consequence, the topologies and the components values can be different in identical SMPS. In domestic applications, the topologies (b) and (c) of Fig.8 are extensively used. The topology (a) is used more in industrial applications.

Usually, the input protections of the SMPS include over-voltage protections. Fig. 9 presents four different protections utilized in SMPS.

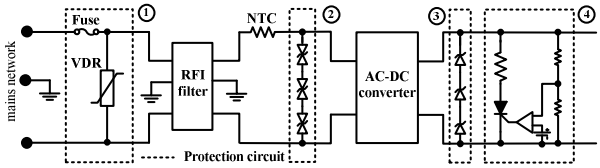

Fig. 9 Over-voltage protection circuits: (1) VDR; (2) bipolar Zener; (3) unipolar Zener; (4) voltage controller thyristor.

A Voltage Dependent Resistor (VDR), bipolar and unipolar Zener diodes (suppressor diodes) and a voltage controller thyristor circuit. The circuits have the same operation principle, when the clamping voltage, V_{CLP}, is passed, the circuit conduces and blows the input fuse for excess of current. The correct over voltage protection requires the use of the VDR and one of the other circuits. In industrial SMPS, the VDR and the bipolar Zener diodes are normally used. Contrarily, in domestic applications only the VDR is used. Fig. 10 shows the voltage and current characteristic curves of these two devices.

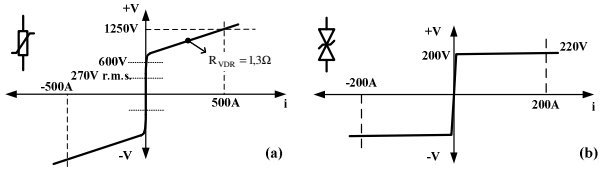

Fig. 10 Voltage and current characteristic curves: (a) 250Vrms VDR; (b) 200V bipolar Zener diode.

In SMPS the VDR presents typically a conduction voltage, V_{CON}, of 120% V_I and a clamping voltage of 185% V_I. This way, a low leakage current above some few μA (50 - 200μA) is guaranteed. This device can support energy dissipation greater than 10J to 100J. The Zener diodes have a clamping voltage well defined and present low dynamic conduction resistance, but can only

support low energy dissipation, typically less than 10J. The correct operation of these two circuits, simultaneously, requires that the Zener clamping voltage is superior to the VDR conduction voltage, to guarantee the main dissipation energy in the VDR. Normally, the Zener diodes clamping voltage is defined for 125% of V_I. The Zener diodes are connected after the NTC resistor connection, in order to perform a current limiter. The voltage controller thyristor circuit has a characteristic identical to the VDR, but with a conduction voltage well defined and presents zero leakage current. The zener diodes are more expensive than the VDR and, therefore, are less utilized in domestic SMPS. The voltage controller thyristor is the most expensive protection circuit and is only used in expensive and ultra sensitive equipments.

In a circuit that uses only the VDR, the response time is greater than 1ms, performed by the fuse action, for transients with amplitude superior to 185% VI. The use of the Zener diodes, limits the transients to 125% VI, but only if these have low energy. High energy transient blows the Zener diodes and will damage the converters.

4. Susceptibility Analysis Of The SMPS

To realize the present analysis of the SMPS, we consider the worst case: the over voltage circuit protection utilizes only the VDR; the attenuation of the RFI filter for mains voltage transients is not considered (because the topologies used are very different in identically SMPS); the AC-DC converter is a diode bridge and a capacitive filter (because this solution is extensively used and it is more sensitive than the boost rectifier).

Some power quality monitors use the CBEMA curves and detected voltage events out of the envelope. In fact, the major susceptibility problems are not related with the static rms value of the input voltage, but with the voltage transients. In the authors opinion this curves have some frailties for transient events: they do not refer neither the dv/dt present in the transients, nor the neutral to ground or phase to ground transients [1].

The presence of short duration over voltage transient between phase and neutral can provoke some several effects in the power supply: damage of the rectification diodes due the current peak present in the charge capacitor C_A; damage of C_A capacitor with excess of charge; blows the input fuse with the VDR conduction; output voltage transient or transformer saturation due the low time response of the output voltage controller. Fig. 11, shows the influence of the dv/dt present in a notch, in the input current, i_I, of the SMPS.

The damage of the rectifier diodes due to current excess is related with the dv/dt in the phase to neutral voltage. It is complex to establish a dv/dt prejudicial to the rectifier diodes, because different SMPS have several differences in these devices. This way, we consider as prejudicial to the rectifier diodes, notches with 120% of V_I and with duration of 10us to 10ms. With a detection of this event a family of dv/dt transients prejudicial to the AC-DC converter is guaranteed:

- **Notch** - phase to neutral positive notches (> 120% of V_I), during time (10us < t < 10ms) - counting the number of occurrences, n_O.

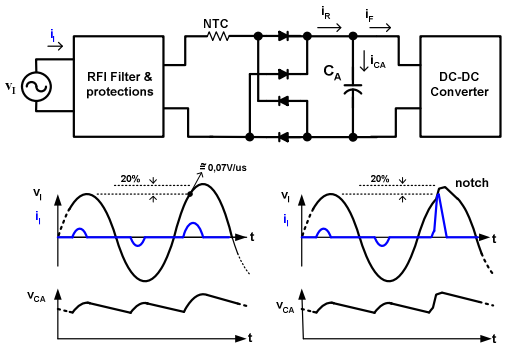

Fig. 11 Influence of the dv/dt present in a notch, in the input current, i_I, of the SMPS.

Considering the voltage controller time response, it is possible to specify the maximum dv/dv in V_{CA}, which results in a considerable transient in the output voltage (more than 1% of V_O), and in transformer saturation. State space average models are needed to this analysis.

In simulations a dv/dt in V_{CA} of 1V/us was obtained for the output voltage transient analysis, and a dv/dt of 2V/us for transformer saturation. The last corresponds to a transient that has an amplitude superior to 125% of V_I. To guarantee a detection of this prejudicial event, we consider a detection of the event - $\mathbf{v_{FN}}$ **Transient**:

- $\mathbf{v_{FN}}$ **Transient** - phase to neutral high dv/dt transients (> 1V/us) - counting the number of occurrences, n_O.

Voltage transients in phase with ground and neutral to ground can provoke several effects in the output voltage of the SMPS due to the leakage capacitances present in the isolation transformer. To make this study we create a high frequency impedance model, Fig. 12, obtained with an impedance meter HP4294 and a commercial SMPS.

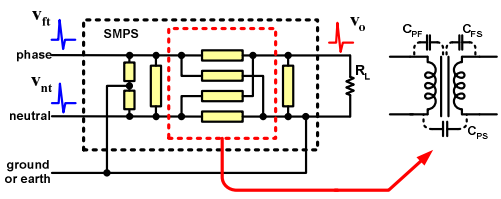

Fig. 12 High frequency impedance model.

With a frequency characterization of those impedances is possible to verify that common mode transients have more impact in the output voltage, than the transients between neutral to ground or phase to ground. The last ones can be detected with the $\mathbf{v_{FN}}$ **Transient.** In a conclusion of this analysis we consider the detection of two events:

v_{NT} Transient and **Spike**:

- **v_{NT} Transients** - neutral to ground high dv/dt transients (> 120V/us) - counting the number of occurrences n_O.

- **Spike** - neutral to ground voltage, >50V, during time (10us < t < 10ms) - counting the number of occurrences, n_O.

The objective of the detection of the event **Spike** is to guarantee a different family of dv/dt transients in neutral to ground voltage, which in the most of the cases results in voltage transients in the output voltage.

For the steady state operation, we consider more three events in the phase to neutral voltage, based on CBEMA curves and during more than 20ms: Over-Volt, Low-Volt and Failure:

- **Over-Volt** – Over voltages above 110% during more than 20ms, counting the total time, t_T, (if t_T > 30s), and the number of occurrences, n_O.

- **Low-Volt** – Low voltages under 85% of V_I during more than 20ms, counting the total time, t_T, (if t_T > 30s) and the number of occurrences, n_O.

- **Failure** – Low voltages under 40% of V_I during more than 20ms, counting the total time, t_T, (if t_T > 30s) and the number of occurrences, n_O.

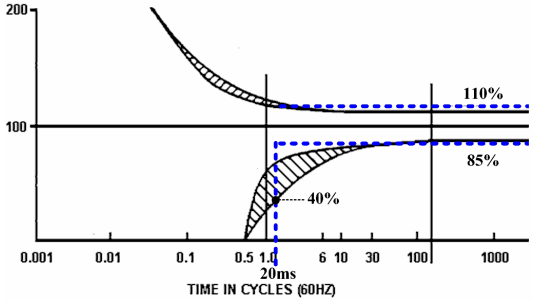

Fig. 13 Limits for steady state events.

The occurrences of voltage transients between the three points, phase, neutral and ground are related with turn on and turn off of loads in the mains network. A high voltage drop in steady state, on the distribution transformer and on distribution lines increases the probability of transient occurrences.

Fig. 14 shows a single phase mains impedance model. In the model, impedance Z_L represents the leakage transformer inductance, and impedance Z_D represents the impedance between the power transformer the customer.

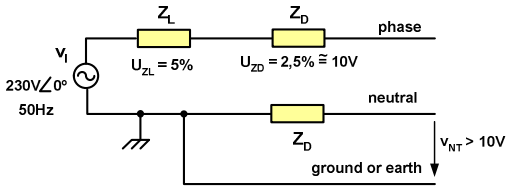

Fig. 14 Mains network impedance model.

In normal conditions of operation, the voltage drop on the earth impedance is reduced, and can be despised, therefore the voltage drop into Z_D is approximately equal to the voltage between neutral and ground. To prevent the probability of transient occurrences a detection of the High-Volt event is considered.

- **High-Volt** – voltage between neutral and ground, with an amplitude greater than 10V, during more than 20ms - counting the total time, t_T, (if t_T > 30s).

Table I presents a resume of the different events identified in this section.

TABLE I

Event	Characteristic	Register
Over-Volt	phase to neutral > 110% V_I t > 20ms	t_T & n_O
Low-Volt	phase to neutral < 85% V_I t > 20ms	t_T & n_O
Failure	phase to neutral < 40% V_I t > 20ms	t_T & n_O
Notch	phase to neutral > 120% V_I 10us < t < 10ms	n_O
Spike	neutral to ground > 50V 10us < t < 10ms	n_O
Transient	> 1V/us - phase to neutral > 120V/us - neutral to ground	n_O
High-Volt	neutral to ground > 10V t > 20ms	t_T

5. Power Quality Monitor (PQM) Prototype

One of the objectives of this study is the development of a commercial single phase power quality monitor, which can be used for any low voltage customer.

The PQM is created with four different printed circuit board's (PCB). Six digital event counters, 8bit, four digital time counters, 16bit, an analogue detection board and a main board. The digital event counter board permits to count a maximum of 99 events in a 8bit output format; the digital time counter board permits to count a maximum of 99.99 hours in a 16bit output format; the analogue board has the function to detect the events and generates a digital pulse to increment the counters; the main board makes the visualization counter selection. Fig. 15 shows the Building blocks of the PQM.

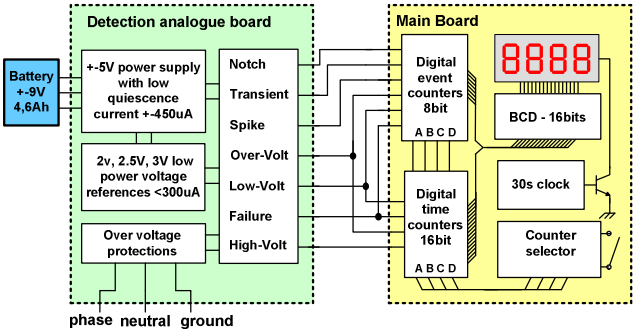

Fig. 15 Building blocks of the developed PQM.

The impedance between the PQM and the mains must be high to avoid any perturbation in the mains caused by the PQM. The PQM must, therefore, to be supplied with batteries. To provide a good standby autonomy, the total consumption of the PQM must be low. In the PQM development CMOS technology was used in all counters and main board, and the total consumption in standby mode is less than +7.5mA and -5mA. With the 4.6Ah battery the autonomy in standby mode is greater than 500 hours.

An automatic timer, with 30s of time base, turns-off the display to provide a low consumption, if the select counter is not utilized in this time period. The developed PQM prototype is presented in Fig. 16.

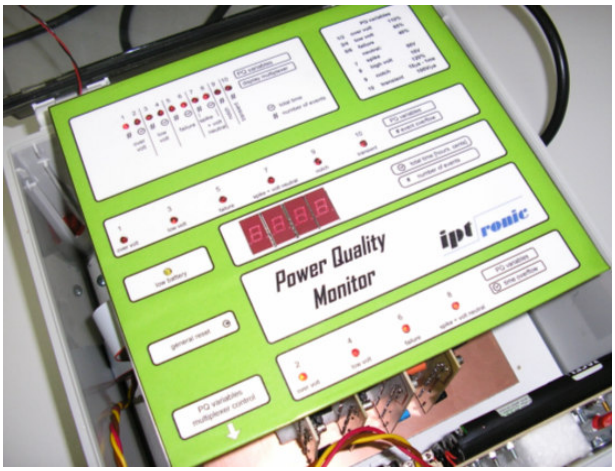

Fig. 16 Power Quality Monitor prototype.

6. Conclusions

The authors developed a systematic study of SMPS in order to understand the effects of power quality disturbances in the operation of electronic equipments. Seven voltage events related with the susceptibility of the electronic equipment to voltage perturbations in the mains network were defined. A low cost and low power, single phase Power Quality Monitor was developed to detect the identified events. Efforts are being made in order to certificate the equipment and to proceed to its commercialization.

References

[1] Victor Anunciada, Hugo Ribeiro, “Power Quality as a Reliability Problem For Electronic Equipment”, ICREPQ05.