High-voltage Gain DC–DC Boost Converter with Coupled Inductors and Interleaved for a PV System to Supply Data Centers

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Abstract. This study presents the analysis and design of a high-voltage gain dc–dc converter applied to photovoltaic systems. A Battery bank rated at 24 V is connected to the input side, and the converter is responsible for stepping the voltage up to 311 V, in order to supply a Data Center to be used at *IFRN's Campus Verde* (Federal Institute of Rio Grande do Norte's Green Campus), where there is already a photovoltaic plant connected to the AC bus. The idea of a direct current supply is to improve the quality of energy delivered to such loads. This study proposes a converter topology with interleaved operation between two boost converters with coupled inductor and duplicity of the exit module to improve the ripple of the output voltage and reduce the high voltage on the output diode of converter, respectively. The Interleaved topology between two converters with a lag of the 180o promotes the reduction of output voltage ripple as well as filter elements, since it allows the load to receive the double of switching frequency, and doubles the total output power of the circuit. The interleaving concept reduces input current ripple and the input inductance size. In addition, the dimensioning voltage is not output voltage but capacitor voltage, which is lower than output voltage, reducing costs.

Key words

Boost, Coupled-Inductor, Data Center, Interleaved, Quality of Energy.

1. Introduction

In a typical data center, less than half of the power is delivered to the computer loads, which includes microprocessors, memory and disk drives. The rest of the power is lost in power conversion, distribution, and cooling, resulting in high utility bills and a large environmental impact.

It has also been shown that the capital cost of the infrastructure of power delivery and cooling required for a data center already exceeds the purchase price of the servers. The use of higher voltage DC as an efficient energy distribution option for both types of facilities has been discussed for almost a decade. Its potential to improve utilization of distributed renewable generation and its lower costs component has also been pointed out. [1]

Most loads in a data center are DC by nature. These include telecom line cards, servers, network switches and routers, data storage and network appliances. Other loads that are inherently AC can be substituted with DC equivalents, such as high efficiency LED lighting and climate control, at the time of installation.

The advantages of a DC power supply in a data center are:

- Fewer conversion stages in the overall system resulting in higher efficiency.
- Longer battery back up without de-rating system.
- No harmonic losses and effects on distribution.
- No need for load balancing between phases
- Less environmental impact
- Simplified distribution switchgear
- Simplified maintenance
- Conditioned output power quality [2]

In Brazil, the energy distribution delivered to the Data Centers is 110 / 220V AC. All these devices have efficient rectification stage at its entrance, what enables them to be directly connected to a DC system where the operating voltage is of 156 VDC or 311 VDC depending on the location it is installed. For this voltage value to be reached, a high gain DC / DC converter must be introduced into the DC system.

The converter proposed by this study would be used in the data center of *IFRN's Campus Verde*. A photovoltaic plant has already been installed to power the campus, but in AC connected to the grid. Our proposal is that the data center should make use of the power of a DC bus of 311 Vdc, integrated to the existing system, as shown in figure 2.
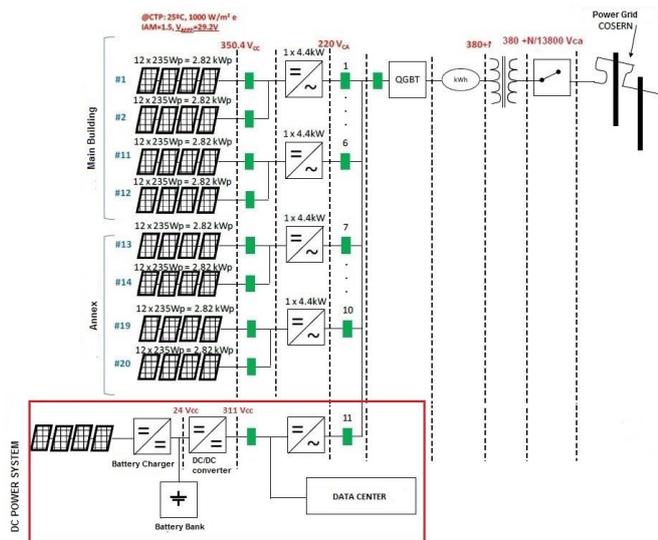
Figure 1 - Microgrid proposal of Green college campus IFRN

A topology lift high-gain converter with coupled inductors, was chosen, for being a simple topology with just a key, of lower cost that meets our needs, as shown in Figure 2. However, this topology has features that generate some problems. The first is the high peak voltage that the diode D1 is exposed forcing, in some cases, the use of more robust power diodes. The second unfavorable feature is the necessity of using a snubber of power protection for switch because the ripples of tension on it are quite high, in some cases. The third feature is the need to filter to correct the high voltage ripples in the output of the converter. To fix these problems we propose some changes in this topology.
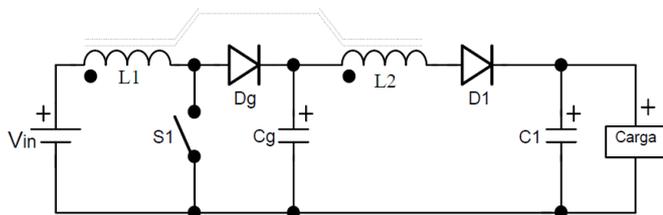
Figure 2 - Boost Converter with Inductor Coupled.

2. The Proposal: An Elevator Converter

A. Structure of the Proposed Converter

Changes were made in the structure of the original topology, as shown in Figure 3. It was decided that the voltage submitted on the terminals of the diode D1 should be divided, doubling the converter output block, i.e. the inductor, diode and output capacitor (L2, D1 and C1 respectively), thus allowing the use of fast diodes and low voltage drop, proposed in [3]. We opted for the Interleaved topology between two converters with a lag of the 180^0, proposed in [4,5], because it promotes the reduction of output voltage ripple as well as filter elements of proposal [3], since the load is under a doubled switching frequency, because the two branches of the circuit switches operate alternately and doubles the total output power of the

circuit. The interleaving concept can reduce input current ripple and input inductance size. In addition, the dimensioning voltage is not output voltage but capacitor voltage, which is lower than output voltage, reducing costs with power capacitors. [5].
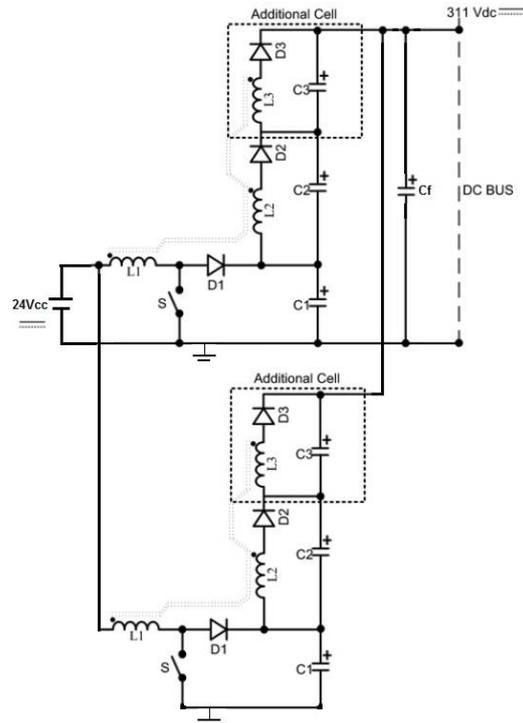
Figure 3 - Boost Converter with Inductor Coupled, intercalated and with duplicate output block.

B. Specifications of the Converter

Considering that the elevator converter is connected to the Bank of batteries that supply voltage 24 Vdc average, it is possible to build table 1, in which the specifications needed to perform the design of elevator converter are presented.

Tabela 1 - Specifications of the Converter

Parameter	Value
V_{IN}-input voltage	24V
V_{OUT}-output voltage	311V
P_{OUT}-output power	600 W
η – performance of the converter	95%
I_{IN}-input current	18, 8A
ΔV_{OUT}-voltage Ripple on the output capacitor	0.5% V_{OUT}
ΔI_{IN}-current Ripple on the input	20% of I_{IN}
F_c -switching frequency	30 KHz
ΔV_{IN}-voltage Ripple on the input	0.2% V_{IN}
D_{CE}- duty cycle	49,9%

C. Qualitative analysis of the proposed converter

The first interleaved converter and the converter proposed in [3] have the same qualitative analysis while the second converter will have an 180° phase lag in relation to the first one, so the waveforms have a 180° phase lag. As proposed in [3], the equivalent circuits that represent the converter operation for one switching cycle are shown in Figure - 4a–c and described as follows. The corresponding main theoretical waveforms are shown in Figure - 4d and represent the operation in DCM. The DCM was chosen to decrease the size of the coupled inductors. Besides, the following assumptions are made:

- Parasitic elements such as leakage inductances and series resistances are neglected.
- All capacitors are large enough to maintain the voltages across them constant.
- The current ripples are neglected.
- All semiconductors are ideal.

The following parameters are also defined in Figure - 4d:

- I_i and I_o are the input current and output current, respectively;
- I_{C1}, I_{C2} and I_{C3} are the currents through capacitors C1, C2 and C3;
- I_{L1} and $I_{L2} = I_{L3}$ are the currents through inductors L1, L2 and L3;
- V_{C1} is the voltage across capacitor C1;
- V_{L2} is the voltage across inductor L2;
- $V_g(S)$ is the gating signal applied to switch S;
- I_S is the current through switch S;
- I_{D1} is the current through diode D1;
- V_S is the voltage across switch S;
- V_{D1} is the voltage across boost diode D1; and
- V_o is the output voltage.

First stage [t0, t1] (Figure 4a): Switch S is turned on and energy is stored in inductor L1. Besides, capacitors C1, C2 and C3 are discharged delivering power to the dc bus.

Second stage [t1, t2] (Figure 4b): Switch S is turned off and inductor L1 is discharged, consequently charging inductors L2 and L3. Even though L1 is fully discharged, it still delivers some energy from the battery to capacitor C1. This is because of the leakage inductance inherent to inductor L1, which is charged during the first stage and now discharged. It can also be noticed that currents I_i, I_{L2} and I_{L3} charge the output capacitors, thus keeping the output voltage constant. Although the capacitors are charged, they contribute to the output current because the charging process is very fast.

Third stage [t2, t3] (Figure 4c): Switch S is off, whereas inductors L1 and L2 are fully discharged and the voltages across them are zero. Capacitor C1 provides energy to the load since all diodes are reverse biased and there is no energy transfer from the input voltage source to the capacitors. The output voltage remains nearly constant in this case [3].
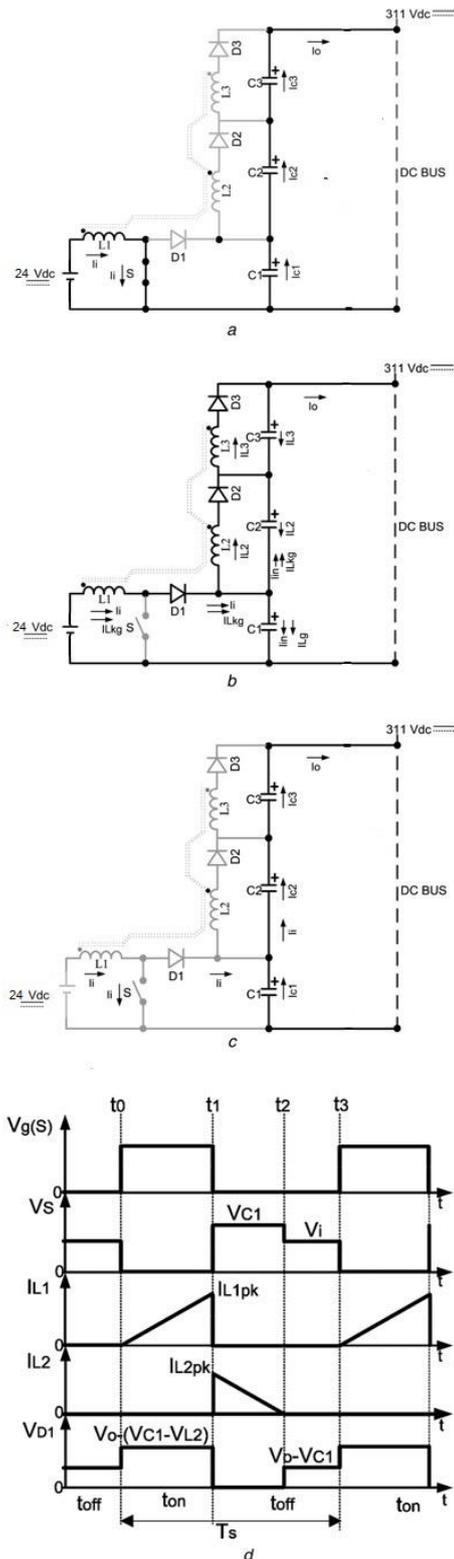
Figure 4 - - Qualitative analysis of the proposed converter in DCM [3].

D. Converter's Dimensioning

Based on the specifications of the converter, calculate the value of inductors and capacitors,

The static gain of the converter in DCM is

$$\frac{V_o}{V_i} = \frac{1}{1 - D_{max}} + N \cdot \left(\frac{1}{1 - D_{max}} - 1\right) \tag{1}$$

N1 and N2 are the number of turns of inductors L1 and L2, respectively. It is also worth to mention that the same number of turns was adopted for inductors L2 and L3, that is, N2 = N3. Substituting the parameters in Table 1 in (1)

$$\frac{N_2}{N_1} = N \tag{2}$$

$$N = \frac{V_o - \left(\frac{V_{i\_min}}{1 - D_{max}}\right)}{V_{i\_min}\left(\frac{1}{1 - D_{max}} - 1\right)} = 11 \tag{3}$$

The inductance values that represent the boundary condition CCM and DCM are

$$L_1 = \frac{V_{i\_min}}{2 \cdot P_o \cdot f_s}\left[V_{i\_min} \cdot D_{max}^2 + \frac{N_1^2 \cdot (1 - D_{max})^2}{N_1 + N_2^2} \cdot (V_o - V_{i\_min})\right]$$
$$= 8{,}63x10^{-6}H \tag{4}$$

$$L_2 = L_3 = \left(\frac{N_2 + N_1}{N_1}\right)^2 \cdot L_1 = 1{,}243x10^{-3}H \tag{5}$$

Vi(min) being the minimum output voltage, Td the switching period and Po the output power. The peak currents through the inductors are

$$D_{nom} = \sqrt{\frac{P_o \cdot 2 \cdot L_1}{V_i^2 \cdot T_s \cdot \left[1 + \frac{V_i}{(V_o - V_i)}\right]}} = 0{,}499 \tag{6}$$

$$I_{L1\_pk} = \frac{V_i \cdot D_{nom}}{f_s \cdot L_1} = 46{,}246 \, A \tag{7}$$

$$t_d = \frac{V_i \cdot D_{nom} \cdot (N_1 + N_2)}{f_s \cdot N_1 \cdot (V_o - V_i)} = 1{,}669x10^{-5}s \tag{8}$$

$$I_{L2\_pk} = I_{L3\_pk} = \frac{(V_o - V_i) \cdot t_d}{L_2} = 3{,}854 \, A \tag{9}$$

$$I_{L1_{rms}} = \frac{\sqrt{3} \cdot D_{nom}^{\frac{3}{2}} \cdot V_i}{3 \cdot L_1 \cdot f_s} = 18{,}859 \, A \tag{10}$$

$$I_{L2\_rms} = I_{L3\_rms} = \left[\frac{\sqrt{\frac{3 \cdot t_d^3 \cdot f_s \cdot (V_o - V_i)}{3 \cdot L_1}} \cdot \left(\frac{N_1}{N_1 + N_2}\right)^2}{}\right]$$
$$= 1{,}574 \, A \tag{11}$$

$$I_o = \frac{I_{L2\_pk}}{2} = 1.927 \, A \tag{12}$$

From the theoretical analysis, capacitor C1, C2 and C3 can be calculated by applying the following expression

$$C_1 = \frac{I_o \cdot D_{nom}}{f_s \cdot \Delta V_{C1}} = 2{,}061x10^{-5} \, F \tag{13}$$

$$C_2 = C_3 = \frac{10 \cdot P_o}{V_o^2 \cdot 2 \cdot \pi \cdot f_s} = 1{,}646x10^{-7}F \tag{14}$$

E. Results of the Simulation

The image below shows the simulated circuit in PSIM, closed loop.
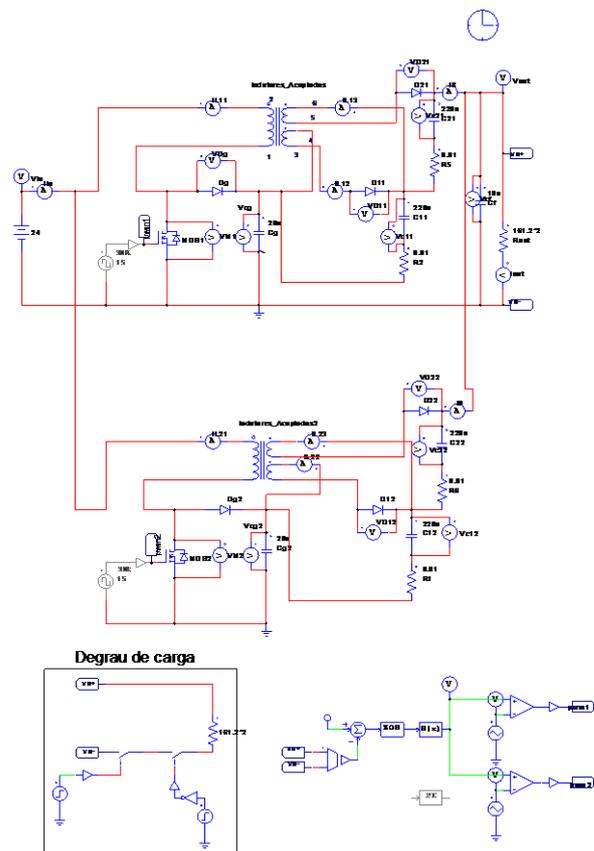
Figure 5 - Proposed Simulation Converter in closed loop.

The following waveforms resulted from simulation:

The current at the primary inductors and in the switches was the same: 33, 24 V with step phase of 180^0 between them; and the current in the secondary inductors and in the diodes' output was also the same: 2.5 V, as shown in Figures 6,7 and 8.
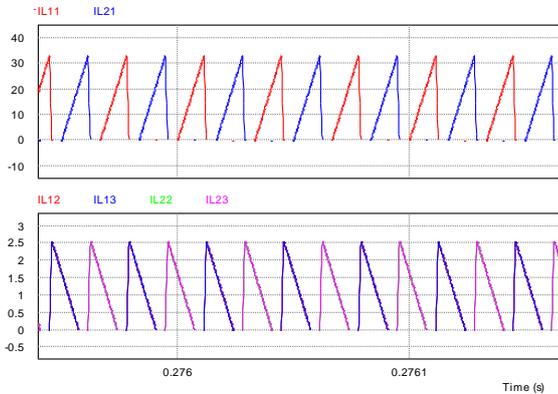
Figure 6 - Current in the inductors L1, L2 and L3 in the two interleaved converters
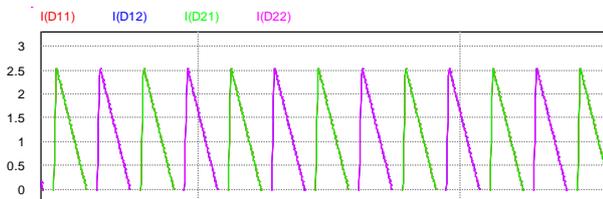
Figure 7 - Current in the diodes' output.
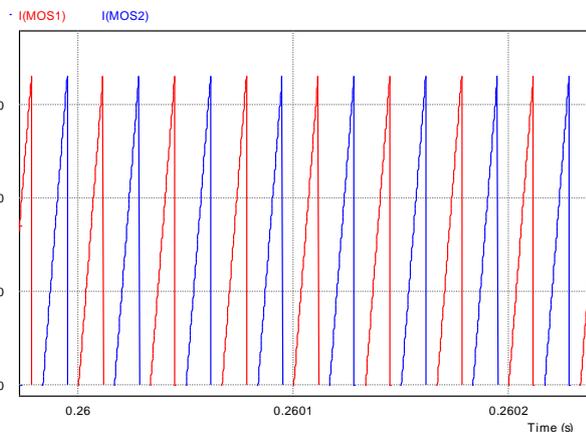
Figure 8 - Current in the switches.

The voltages in the diodes' output were 272,65V, much lower than the 436V proposed in [3]. The intercalation between two converters contributed to further decrease the voltage on the diodes' output, as shown in Figure 9.

Figure 9 - Voltage at the diodes' output

The voltages' peak in the switches were 50V, and the output voltage was 311V, as expected, with a voltage ripple of only 0.6V, shown in Figure 10.
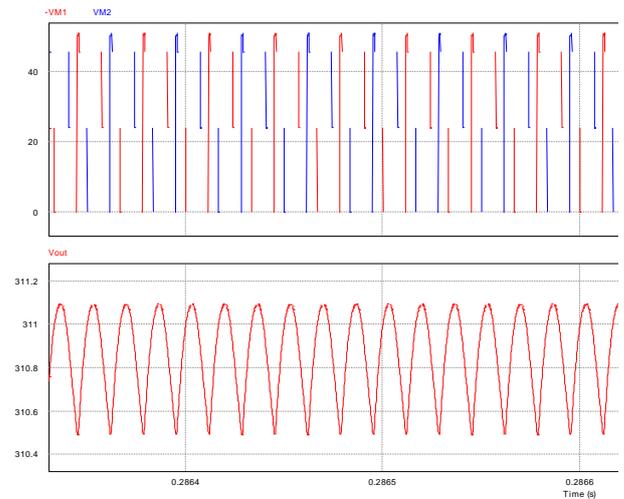
Figure 10 - Tension in the MOSFETS and in the Converter's Output Voltage ripple.

3. Conclusion

The proposed system reduces the voltage on the diodes, the voltage on the switches and the reduction of the inductors' size compared to the proposed converter [4] and the interleaving of the two converters by doubling the output frequency what leads to the reduction of the ripple of the output voltage as well as the reduction of the filter elements and has contributed to reduce even more the voltage in the diodes' output and doubles the output power in relation to the converter proposed [3].

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