Effect of sampling and computing times on a hysteresis vector controller applied to renewable distributed generation

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Abstract. Nowadays the use of renewable energies is increasing at a high rate, but there are limitations related to the low quality of the power sent to the utility. That is the reason why new control systems have been developed.

Due to the difficulty of having adequate equipment to implement the different control systems [1] they have been simulated, but taking into account the data acquisition times.

The paper considers the delay time in the switching status due to the data sampling and calculation of the parameters required for the control. The calculations used to obtain the phasors required to calculate the optimal switching and the switching time are shown.

In order to obtain the results, the starting point is a predictive vector control, described in [2], where the calculation times have been applied for sampling frequencies of 100kHz and 200kHz, comparing the results with the case of having a infinite sampling frequency.

Key words

Predictive current controllers, digital control, distributed power generation, power quality, renewable energies.

1. Introduction

The advantages of distributed generation are more important when they take part in a microgrid [3-5]. In order for these advantages to take place, the connection of the generating systems must be performed in suitable technical conditions whereas, on the other hand, if these conditions are not provided, the operation of the microgrid, already difficult, can be compromised.

The technical requirements for the connection of distributed generation affect all the aspects related to the quality of the energy sent to the grid. [6,7]. Power electronics has achieved a main role in the development of renewable energies in distributed generation, improving their efficiency [8].

The desired characteristics for a current control are: zero phase and amplitude errors, high dynamic response of the system, reduced harmonic distortion, good dc-link voltage utilization and limited switching frequency spectrum. In order to obtain these characteristics the

more widely used systems are current controlled VSI converters.

The most common control methods are vector controls and, among them, the predictive controls that calculate the optimal switching state, being more robust and adaptable to system variations. Hysteresis vector control keeps the current vector inside a specific area by deciding the suitable switching states.

In order to obtain the adequate switching state alter the calculation of the algorithm, it is necessary to use the data of the phasors that are going to be present in the instant when the switching is applied, so they must be predicted or estimated from previous values.

Vector hysteresis control methods have to be implemented using digital electronic devices, being affected by the sampling and computing times of the chosen device. The practical implementation of the control has to take into account these times in order to achieve the desired results.

The paper analyses the influence of the sampling and computing times in the vector hysteresis current controller presented in [2].

2. Phasor prediction and estimation

The proposed method is based in the hysteresis vector control [2] taking into account the sampling and computing times.

Being T_s the sampling time and T_c the computing time for the algorithm, it can occur that $T_c \leq T_s$ or $T_c > T_s$.

In the first case, being kT_s the present time, the computed switching state will be applied at instant k+1. In order to have the best possible state, the parameters of the system at instant k+1 must be predicted from the ones available at instant k. To do this, we are going to use one of the prediction methods that gives better results, Lagrange extrapolation [9].

$$Pn(x) = \sum_{k=0}^{n} Ln_k(x) \cdot f(x_k) \qquad (1)$$

where: (2)

We are going to use to obtain the prediction for the reference current phasor at time k+1, .

(3)

The value of the phasor at time k+1, , can be estimated as a function of the parameters of the circuit, performing the integration of the following function from values k to k+1.

(4)

(5)

Where is the voltage phasor applied during the interval (k, k+1), obtained from the switching state applied at time k, and is the grid estimated voltage phasor advance , for instant k+1, from data at time k.

Using the values of the current phasors, the current error can be predicted.

(6)

This is the expression that should be used in the hysteresis comparators. It is also required to calculate the value of the reference voltage, $\overline{V}_{k+1}^{p}$, obtained from the voltage in discrete mode.

(7)

Substituting $\bar{I}_{k+1}^{p}$, we obtain the expression for the voltage reference. Thus, at time kT_s+T_c it is noticed that current, $\bar{I}_{k+1}^{p}$, goes beyond the desired band and considering the grid voltage predicted for instant k+1, $\overline{V}_{k+1}^{p}$, the optimal switching state is chosen.

In the second case, being $(k-1)T_s$ the present time, a possible solution is to accommodate the sampling time to the computing time, but the estimation of the magnitudes will worsen. A better solution is dividing the operation in two parts, the time needed for the prediction of the phasors, usually shorter than the sampling time, T_s, and the computing time of the algorithm, $n*T_s$. Taking into account that the time

required for the prediction is short, two predictions can be performed, one for time $n*T_s$ and another for time T_s.
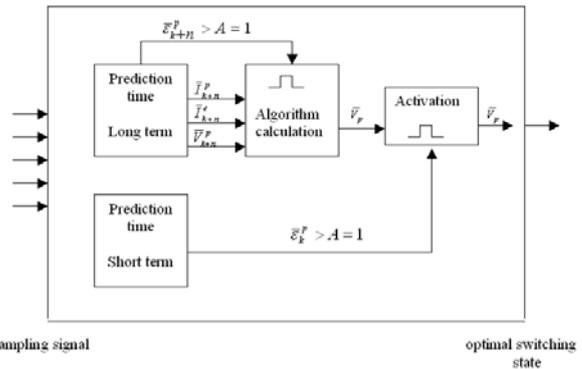

Figure 1. Calculation diagram for the hysteresis vector regulator using a predictive algorithm, with double phasor prediction.

The first one, "short term", gives a more accurate prediction of the current and its result is used to decide whether the switching has to take place or not (i.e. if the current error phasor goes out of the allowed area or not). In order to calculate the current error phasor we perform the same calculations that in the case $T_c \leq T_s$, but supposing that we are now in time k-1, obtaining:

(8)

(9)

(10)

The second one, "long term", gives the values of the phasors at instant k+n from the values at k-1 and is used to calculate the optimal switching state at instant k+n, that considers the delay time $n*T_s$, due to the calculation of the algorithm. The reference current , is obtained from:

(11)

Substituting in the equation for "short term", it becomes:

(12)

We also need to obtain using the following equation.

$$\bar{I}_{k+n}^e = \bar{I}_{k-1} + \frac{Tr+Tm}{L}\overline{V}_{p,k-1} - \frac{\overline{E}_{k+n+\pi/2}^e - \overline{E}_{k+\pi/2}^e}{wL} \qquad (13)$$

Moreover, the values at k+n for the grid voltage phasor, $\overline{E}_{k+n+\pi/2}^e$ and the reference voltage $\overline{V}_{k+n}^p$ are predicted.

$$\overline{E}_{k+n+\pi/2}^e = E_{k-1}\angle\left[\varphi_{k-1} + \omega\cdot(Tr+Tm) + \pi/2\right] \qquad (14)$$

$$\overline{V}_{k+n}^p = \overline{E}_{k+n}^e + \frac{L}{Tr}\left(\bar{I}_{k+n}^p - \bar{I}_k^p\right) \qquad (15)$$

In this last equation we substitute $\bar{I}_k^p$ y $\bar{I}_{k+n}^p$.

Using these two predictions, the operation of the system is significantly improved.

3. Comparison

An instantaneous hysteresis vector control [1] has been compared to two "real" controls with switching frequencies of 200kHz and 100 kHz respectively. The three methods have been simulated using MATLAB for a generation system connected to a 400 V grid, having an inductance of 0,8 mH. In order to compare their behaviour under diverse circumstances, the operation at 650, 350 and 150 A has been tested.

The tests have been carried out varying the DC voltage from 710 V down to the minimum value required for the bridge to operate properly. Every voltage level has been kept for 0,2 seconds and the test has been repeated at least 4 times.

Figure 2 shows THD at the three specified load levels for different DC voltages. It can be noticed that at high current levels the difference in THD is small, especially at high switching frequencies. The THD corresponding to 150 A and 100 kHz is not represented for clarity, and the values are above 0,085 for all DC voltages.
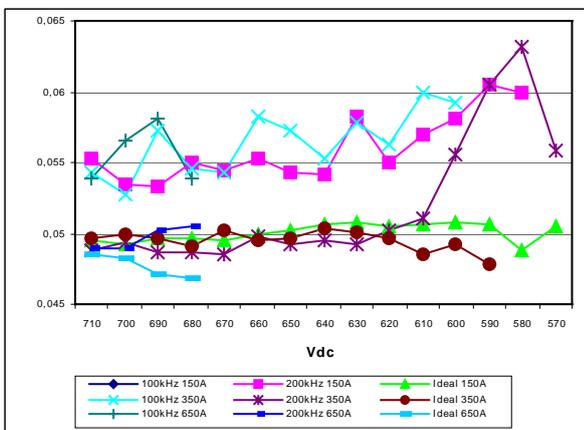

Figure 2. Average output current THD for predictive circular hysteresis controllers.

Figure 3 shows the variation of current THD for different output currents with a DC voltage Vdc=700V and with an error limit of 10% rated current. It shows that at low currents THD is very high.
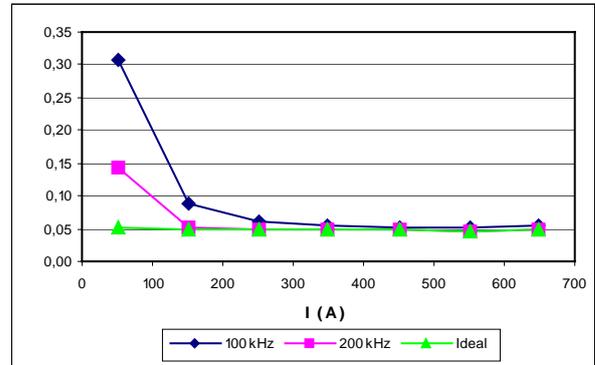

Figure 3. Current THD variation vs. current value.

Figure 4 shows switching frequency in the same conditions of figure 1. It can be noticed that at all current levels the switching frequency is higher in the cases with finite sampling time, increasing with DC bus voltage.
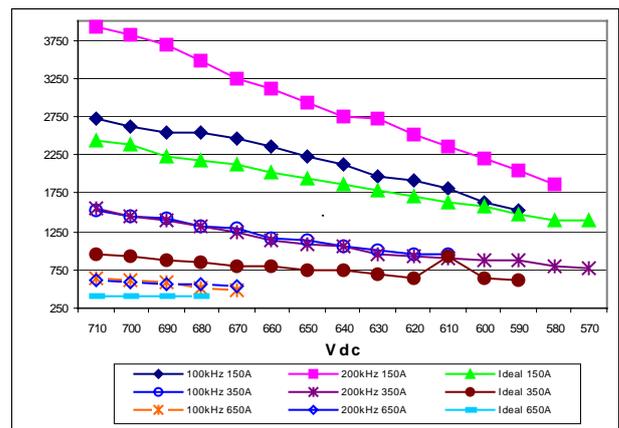

Figure 4. Average switching frequency (Hz) for predictive circular hysteresis controllers.

Figure 5 shows switching frequency vs. current variation. As current decreases the band is reduced and the switching frequency increases significantly. It can be noticed that switching frequency increases with the reduction of the band, whereas the actual value of the current has no influence. It can also be noticed that although switching frequency increases greatly, THD worsens clearly.
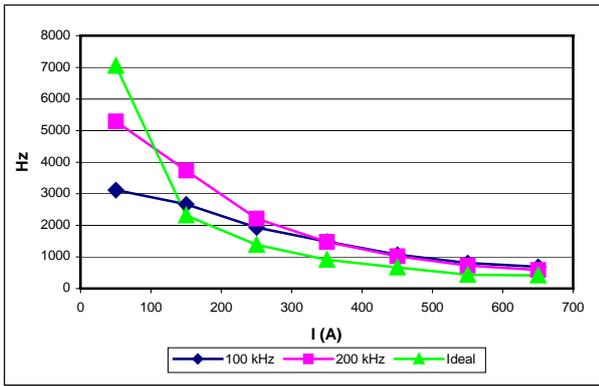
Figure 5. Switching frequency vs. current for different sampling frequencies.

Figure 6 shows current harmonics obtained at the different sampling frequencies. They have been obtained for a current of 350 A, in order not to take the harmonics in the extremes, and a dc voltage of 680 V, because, as can be seen in fig. 1 THD in this point is close to the minimum for each sampling frequency.

It can be noticed that current harmonics at 200 kHz are always lower that the ones corresponding at 100 kHz. Using a infinite sampling frequency, a significant reduction in the first harmonics can be noticed, although some of them surpass the values at 100 and 200 kHz.
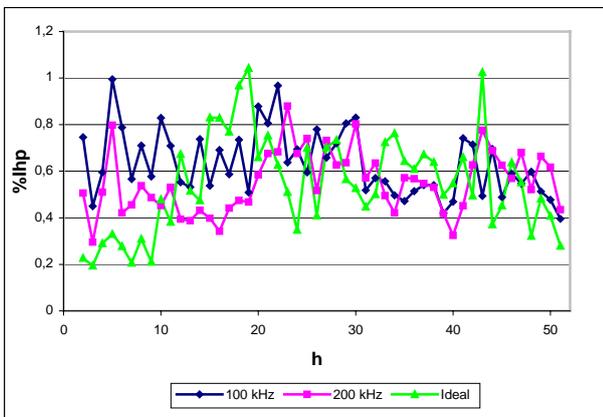

Figure 6. Current harmonic comparison for f_m=100 kHz, f_m=200 kHz and $f_m = \infty$ I_{out}=350 A, A=35 A, V_{dc}=700 V

4. Conclusions

As expected, considering the sampling and computing times worsens the results, causing higher switching frequencies and higher distortion.

It can be noticed in figures 7 and 8 that the current phasor goes out of the error area. With a sampling frequency of 200 kHz it almost does not go out, but at 100 kHz these excursions are much more frequent and, beside, it takes much longer for the system to return within the allowed error area.
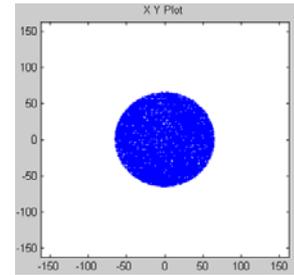With an infinite sampling frequency, the system never lives the allowed error area.

Figure 7. Current error phasor area for predictive circular hysteresis controllers with $f_m = \infty$. I_{out}=650 A, B=65 A, V_{dc}=680 V.
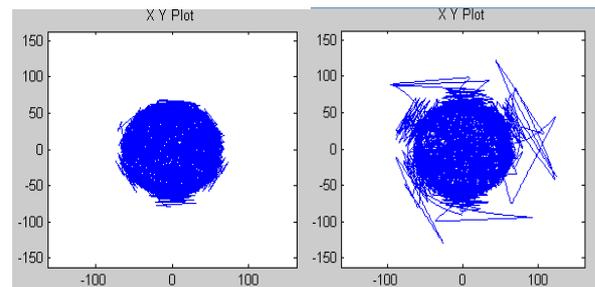

Figure 8. Current error phasor area for predictive circular hysteresis controllers with, f_m=200 kHz and f_m=100 kHz. I_{out}=650 A, B=65 A, V_{dc}=700 V.

At high current levels, the drawback of the sampling time is less important, as can be seen in the simulation results. These results also show that with high sampling frequencies the THD is similar to the one in the ideal case, although switching frequency increases significantly. At low switching frequencies and low current levels, THD also increases clearly.

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