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A Series Compensation Device for the LV Power Quality Improvement

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Abstract. A series compensation device employable in a Low Voltage distribution grid is presented in the paper. This compensator is connected in series with sensitive loads in a distribution system and is able to inject into the grid a controllable voltage to improve Power Quality. The series compensator is employable for compensating voltage dips, flicker and voltage variations. The compensation device can be also used for limiting the short circuit currents, in case of faults located downstream the compensator. The performances of the proposed series compensator and the associate control scheme are demonstrated through digital batch simulations and Control Hardware In the Loop (CHIL) real time simulations.

Key words
Series compensator, Voltage dips, Power Quality, Short circuit currents limitation, Control Hardware in the Loop.

1. Introduction
The number of grid connected electronic loads (LED lighting systems, electric vehicles, air-conditioners and others) is continuously increasing. This type of loads represent one of the main key points for the implementation of demand-response mechanisms [1].
As known, electronic loads are both disturbing loads and loads sensitive to grid disturbances (f.i. voltage unbalances, voltage dips or interruptions).
Actual regulations impose to DSOs a continuous improvement of distribution grids reliability in order to guarantee:

- voltage regulation;
- high power quality (PQ) levels.

PQ levels can also be customized in accordance with the specific needs of each sensitive load or group of loads.
An effective solution to these issues is offered by power electronics. In particular this paper presents the study of a compensation device connected in series to the distribution line, in order to supply the sensitive loads connected downstream the device with controlled voltages, ensuring a desired Power Quality level.
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Such devices work as voltage generators injecting controlled voltages into the grid which are added to network voltages, ensuring the nominal voltages to the loads, even during grid disturbances as voltage dips, network unbalances and flicker [2][3]. These devices have a "global" impact on improving the PQ so they are usually installed at the beginning of a distribution feeder, or before a group of loads.
Another possible function of series compensators is the short circuit current limitation, in case of a grid fault downstream of their connection point [4]÷[8].
In this paper, different control modes, both linear and non-linear, have been taken into account for the compensator. The machine has been designed to compensate for voltage dips with a minimum residual voltage of 40% V_N and a maximum duration of 400 ms, with a maximum downstream load of 150 kVA. Simulation models have been developed for the compensation device for all the considered configurations, and the different voltage compensation functionalities and current limitation have been verified by digital simulation also in presence of distributed generation.
The feasibility of the control of the device and the possibility of implementing it on a "general purpose" microprocessor has been verified by means of Control Hardware In the Loop real-time simulations for one of the considered non-linear control methods.
The paper shows the main results of this study.

2. The series compensation device
A schematic view of the considered series compensator and of a distribution grid model with the series compensator connected along a low voltage distribution line are reported in Fig. 1, respectively (a) and (b).
The device mainly consists of an inverter with its output AC reactances and three single phase transformers (Y/yn) whose secondary windings are connected in series to the distribution lines. The transformers winding ratio, K_{TR}, is chosen to match the inverter output voltage to the line voltage (K_{TR} = 1). The device is completed by an energy storage (capacitor bank) on the DC side and passive filters for lowering the harmonic content of the voltages injected on the AC side. The main design parameters are reported in Table I.

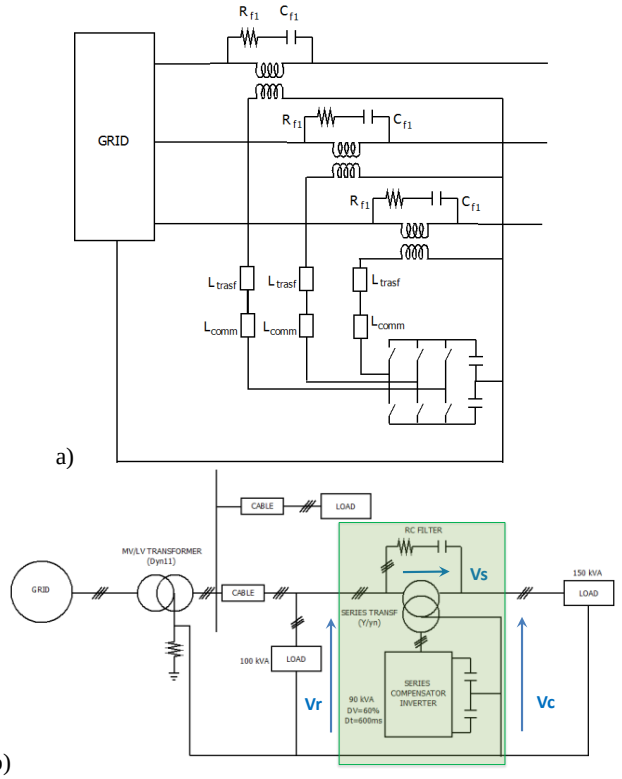


Fig. 1. Schematic view of the series compensator (a) and of the complete system configuration (b).

The device works independently on each electrical phase; the injected controlled voltage (Vs) is added to the grid voltage (Vr) in order to guarantee a phase-to-neutral voltage without perturbation to the downstream load (Vc). The available regulation/compensation functions are:

- precise voltage regulation, when grid voltages are at the steady state in the range of 0,9 V_N ÷ 1,1 V_N;
- flicker compensation;
- voltage dips and swell compensation;

Also, short circuit currents limitation in case of downstream fault is implemented.

Voltage regulation/compensation functionalities are "always on" and they don't need any identification algorithms to be activated, avoiding possible delay in the nominal voltage restoration at "protected" loads. The short circuit current limitation is instead activated only when a downstream fault is detected through the simultaneous measurements of compensator currents (grid side) and downstream grid voltages.

Table I. – Series compensator and transformer design parameters

Series compensator			
Max dip compensable depth		40% V_N	
Max dip compensable duration		400 ms	
Nominal power	A_N	90 kVA	
DC voltage	V_{DC}	800 V	
AC phase voltage	V_{AC}	152 V	
Nominal current	I_N	197 A	
Max current	I_{max}	700 A	RMS
	I_{lim}	1500 A	pk
DC capacitors	C_{DC}	0.6 mF	
Inductance	L_{comm}	0.28 mH	X_{cc} = 11.5%
Filter 1 capacitor	C_{f1}	411 µF	Q = 10% A_N,
Filter 1 resistor	R_{f1}	0.4152 Ω	
Switching freq	f_{sw}	4266 Hz	
Transformer			
Nominal power (single phase transformer)	A_{NTR}	30 kVA	
Primary voltage (grid side)	V_{BT} grid side	152 V	Star connection
Secondary voltage (converter side)	V_{BT} converter side	152 V	Star to ground connection
Windings ratio	K_{TR}	1	
Inductance	L_{trasf}	0.098mH	X_{cc} = 4%

3. Possible control schemes

Different control strategies have been considered:

- multi-loops linear control with PWM modulation, based on Proportional-Integral (PI) regulators (Fig. 2);

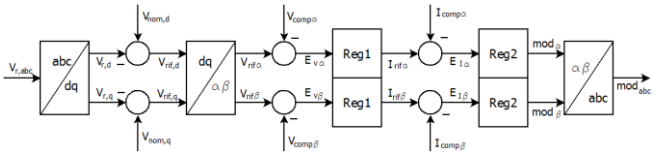


Fig. 2. Linear control scheme

- "hybrid" sliding mode control with a linear loop for generating three current references and a non-linear inner control loop based on sliding mode control (Fig. 3):

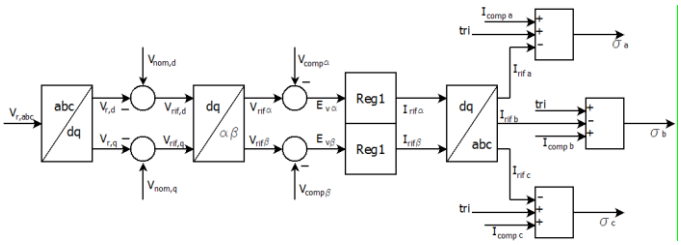


Fig. 3. "Hybrid" sliding mode control scheme

- "pure" sliding mode control, consisting of a non-linear loop that directly controls the generated voltages (Fig. 4):

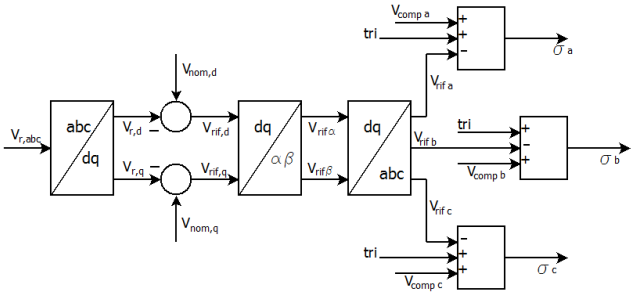


Fig. 4. "Pure" sliding mode control scheme

Both the sliding mode controls are based on the direct comparison of the references quantities and measurements (current or voltage depending on the specific approach) [9].

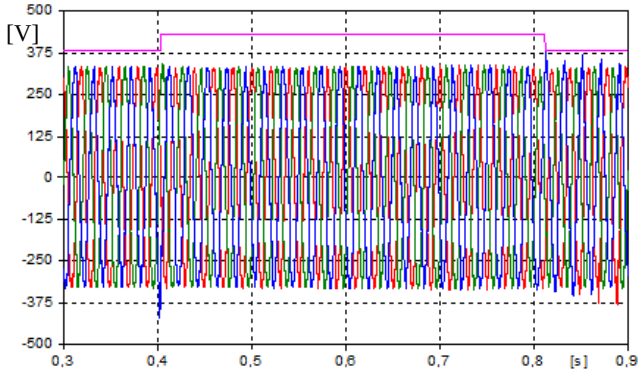
Considering Fig. 4, the references $V_{rifd,q}$ are calculated as the error between the grid voltages ($V_{rd,q}$) and the nominal ones ($V_{nomd,q}$) both expressed in park components. These references, transformed into a,b,c system ($V_{rifa,b,c}$), are compared with the series compensator actual injected voltages $V_{compa,b,c}$. These errors, each representing the sliding surface (σ) for one different electrical phase, are used for defining the inverter switches states, according to:

STATE	Sliding surface	Upper switches	Lower switches
STATE1	if σ>0	ON	OFF
STATE2	if σ<0	OFF	ON

A fixed frequency triangular signal is added to the errors ("tri" in Fig. 4) in order to allow fixed switching frequency operations of the power converter.

The "pure" sliding mode strategy allows to avoid the dynamics of linear regulators, resulting in better dynamic performances if compared to those obtained with linear control and "hybrid" sliding mode control. For comparison, Fig. 5 shows a three phase voltage dip compensation, in presence of DGs, with "hybrid" (a) and "pure" (b) sliding mode control. In case of the hybrid solution, the internal PI regulator is designed to obtain a closed loop bandwidth of 700 Hz and 80° of phase margin. As indicated in the figure, the "pure" control presents a better performance during the beginning of the dip compensation and the grid restoration since the response of the compensator is not related to the time constant of the internal PI regulator.

a)



b)

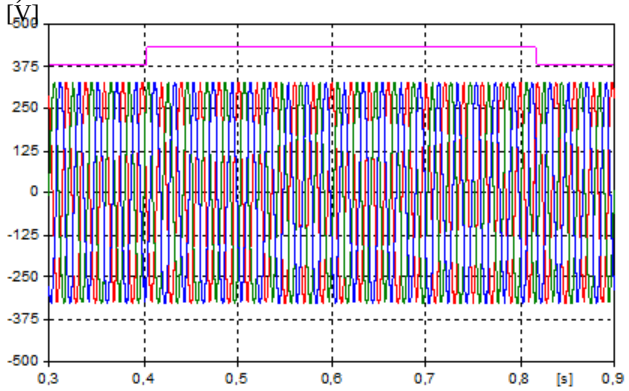


Fig. 5. Comparison between "hybrid" (a) and "pure" (b) sliding mode control performances (voltage dip detection signal – magenta curve)

For these reasons, all simulation results reported in the next sections refers to the "pure" sliding mode control.

For all the considered control approaches, it was supposed that an external power converter, with its own control, manages the recharge of the DC side capacitors directly from the grid voltages.

4. Simulation results

A simulation model of a 90 kVA series compensator device, connected in series to the LV distribution grid, has been implemented within the ATPDraw[1] digital simulator environment, in accordance to the scheme shown in Fig. 1b. Different simulations have been developed to characterize all the features offered by the device.

A. Flicker compensation

In case of a flicker phenomenon, with voltage variations at frequency 5 Hz and of amplitude 5% V_N, the calculated short term flicker[2] P_{st} of the grid side voltages is equal to 23,44 (Fig. 6). Thanks to the voltages injected by the series compensator device (Fig. 7) the load is supplied with a voltage close to the nominal one and the residual P_{st} is equal to 1,1459 (Fig. 8).

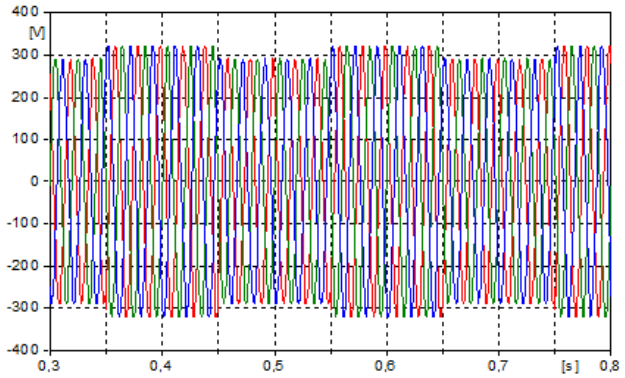


Fig. 6. Grid voltages with flicker

[1] ATPDraw 5.9 p4.

[2] The short term flicker index is calculated on 1 s of simulated time, instead of 600 s, for shortening simulations.

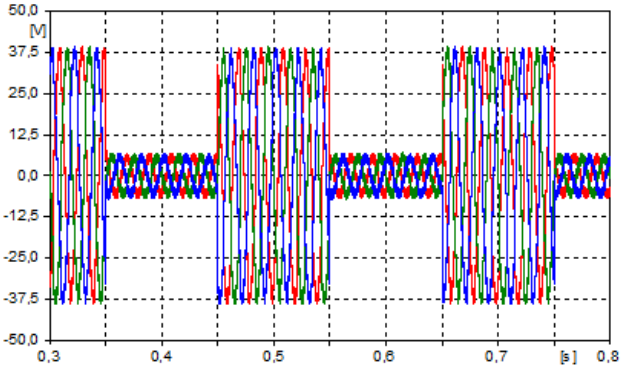


Fig. 7. Series compensator injected voltages

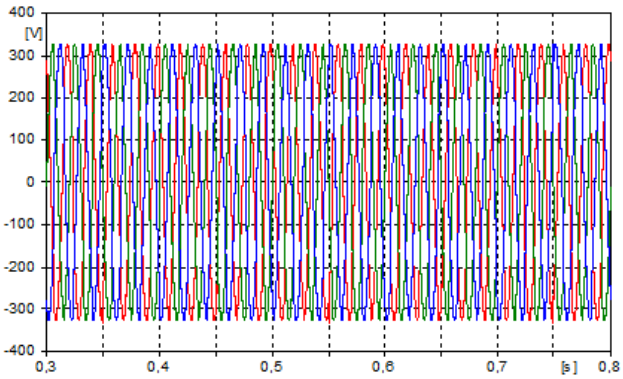


Fig. 8. Load voltages

B. Compensation of a three phase RL load variation

The device is able to regulate the load voltages to the nominal values also in case of grid voltage variation due to the connection of a load. Fig. 9 e Fig. 10 show main simulation results in case of insertion of a RL load of 120 kVA and cosϕ=0,9 downstream the compensator.

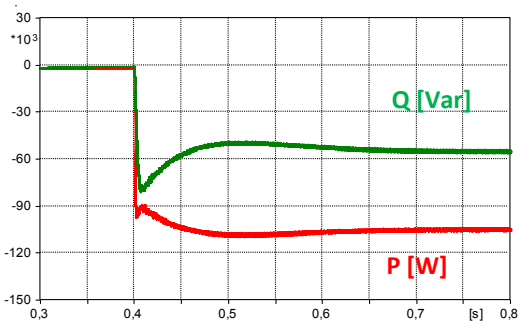
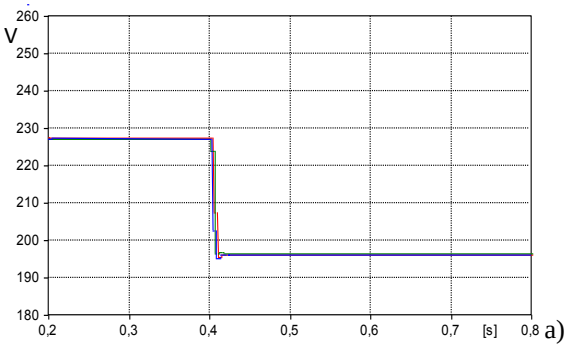


Fig. 9. Load active and reactive power (negative power is absorbed)



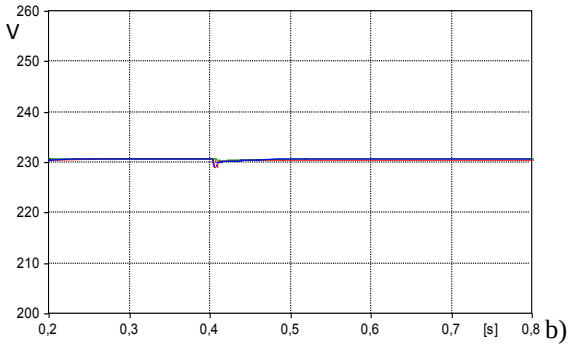


Fig. 10. Load voltages: without (a) and with (b) compensator device

C. Voltage dips compensation

The compensator can improve the power quality level "seen" by the downstream loads thanks to its capability to compensate symmetrical and asymmetrical voltage dips caused by a fault in the MV or LV distribution grid. In particular, in the example reported hereafter a LV grid fault is considered: the fault is located in a feeder next to the one in which the compensator is installed (underlying the same busbar).

Even though this fault causes an unbalanced voltage dip (Fig. 11), load voltages (Fig. 12) are regulated at the nominal values, resulting in symmetrical load currents.

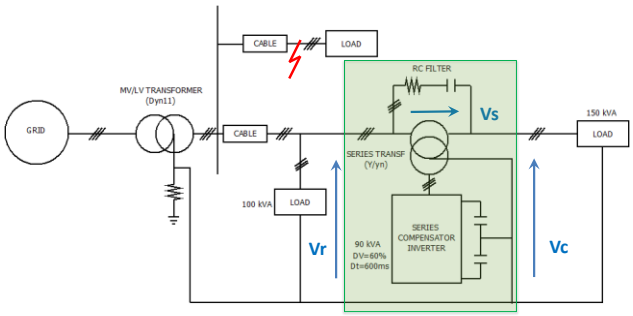
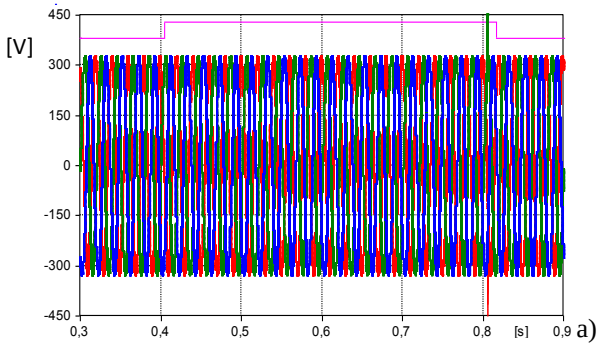


Fig. 11. Grid voltages (Vr) and voltage dip detection signal (magenta curve)



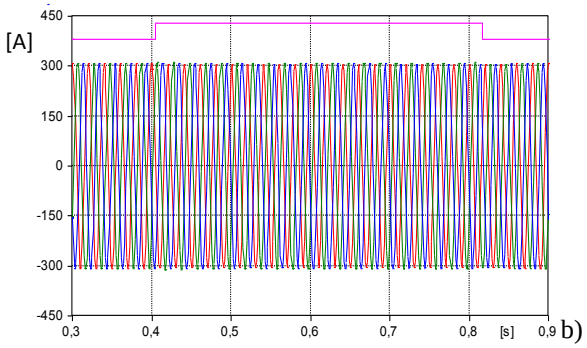


Fig. 12. Load voltages (a) and currents (b) with the voltage dip detection signal (magenta curve)

D. Short circuit current limitation

In case of downstream faults, as shown in Fig. 13, it's possible to use the series compensator device to limit the short circuit current to a desired value. The value of the current limit should be chosen lower than "natural" short circuit current of the grid, but high enough to maintain selectivity of grid protections installed all along the distribution feeder.

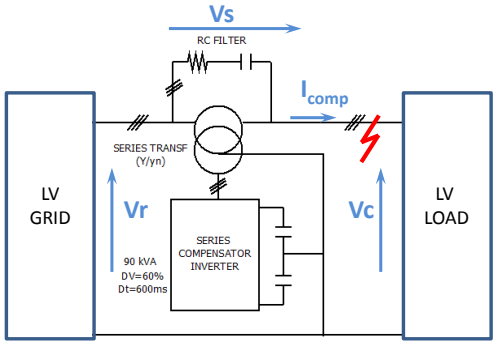
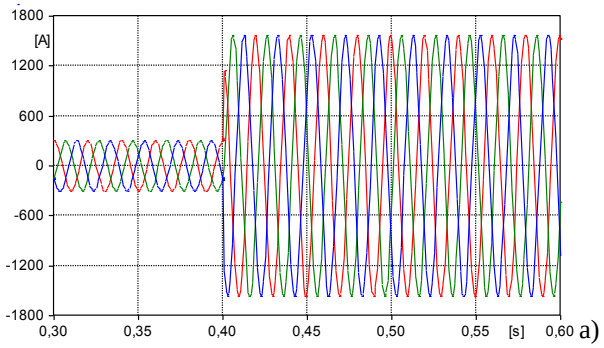


Fig. 13. Schematic representation of the system in case of grid fault downstream the compensator

To guarantee the current limitation function it's necessary to make a proper design of the device, in particular in terms of the maximum currents that can flow through the device components. Two conditions should be verified simultaneously:

- RMS load voltage less than 90% V_N;
- A compensator current higher than a given threshold, defined taking into account possible temporary overloads (in the example I_{pkmax} = 800 A ≈ 2,1 $I_{load,nominal}$).

As reported in Fig. 14 e Fig. 15 the series compensator allows to limit the short circuit current at a defined value in accordance with its capabilities.



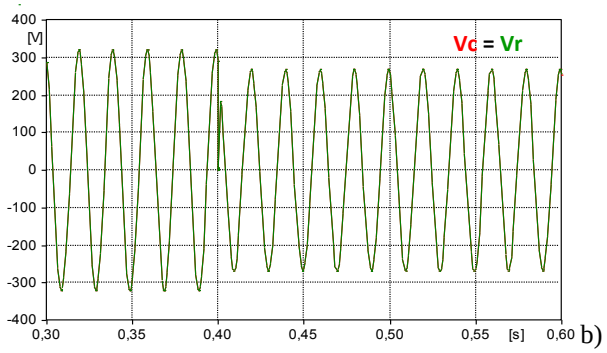


Fig. 14. Short circuit current (a) and grid and load voltages (b): without the device

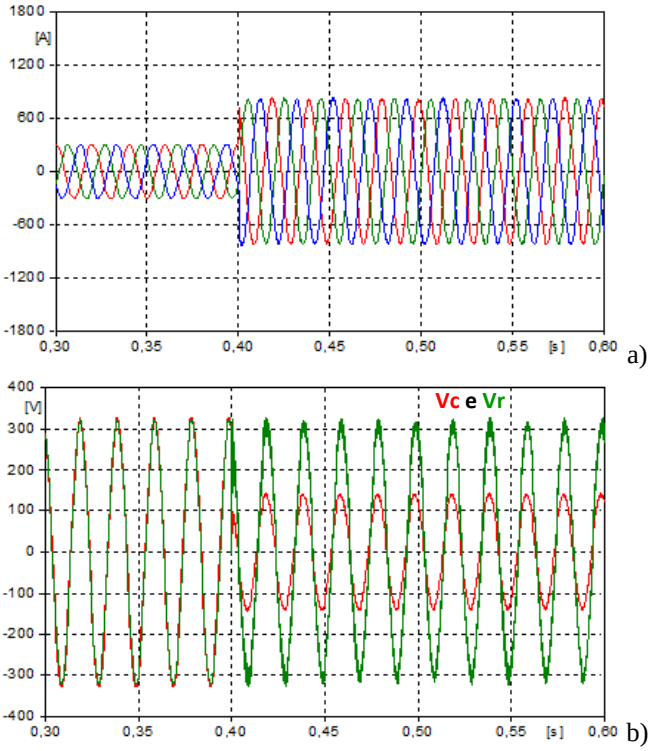


Fig. 15. Short circuit current (a) and grid and load voltages (b): with the device

5. Real time simulations

To verify the feasibility of the compensator in terms of implementation of the control strategies on a real microprocessor, Control Hardware in the Loop (CHIL) simulations have been developed with a Real Time simulator.

The "pure" sliding mode control has been implemented on a general purpose microprocessor (ARM CORTEX M4) with a suited number of digital and analog I/O channels. The used microcontroller, though cost effective, offers good performances in terms of computational speed compared to the switching frequency of the series compensator. In Fig. 16 the controller implemented ad-hoc for CHIL simulations is shown.

All the functionalities presented in the first part of the paper have been verified: in particular Fig. 17 shows the unbalanced voltage dip compensation in case of a fault in LV distribution grid, as presented in the section 4-C.

The behaviors of the system with sliding mode are the same obtained in batch digital simulations (Fig. 11 and

Fig. 12), demonstrating the effectiveness of algorithms implementation in the real controller.

Fig. 16. Real controller with ARM CORTEX M4 microprocessors

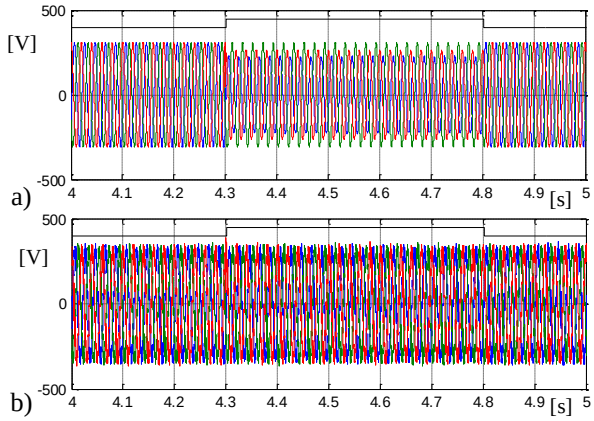


Fig. 17. Voltage dip compensation: grid (a) and load (b) voltages with the voltage dip detection signal

6. Conclusions

The paper presents the design and modelling of a 90 kVA series compensator device for LV distribution grid. The device is adopted for regulating/compensating voltages at sensitive loads connected downstream in case of grid voltage variations. Also, the compensator is used for limiting short circuit currents in case of downstream grid faults.

The study presented in the paper underlines the good performances of the device (in particular for a "pure" sliding mode control strategy) for voltage regulation during steady state grid operations, for flicker phenomena, and also in case of MV or LV upstream faults.

The results of Control Hardware In the Loop simulations, developed with a Real Time simulator, have shown similar behaviours as the ones obtained with batch digital simulations, cross-validating the simulation models and confirming the feasibility of the implementations of the analysed control strategies on a real general purpose microprocessor.

Acknowledgement

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References

[1]. P.K. Steimer, "Enabled by high power electronics - Energy efficiency, renewables and smart grids", Power Electronics Conference (IPEC 2010), 21-24 June 2010, Sapporo (Japan).

[2]. G. D'Antona, R. Faranda, H. Hafezi, G. Accetta, D. Della Giustina, "Open UPQC: a possible solution for power quality. Series unity analisys", Speedam 2014, Sorrento, Italy.

[3]. J. Lakkireddy , R. Rastgoufard, I. Leevongwat, P. Rastgoufard, "Steady State Voltage Stability Enhancement Using Shunt and Series FACTS Devices", Power Systems Conference (PSC), 10-13 March 2015, Clemson (South Carolina, USA).

[4]. M. Hojo, Y. Fujimura, T. Ohnishi, T. Funabashi, "Experimental Studies on Fault Current Limiter by Voltage Source Inverter with Line Voltage Harmonics Compensation", European Conference on Power Electronics and Applications, 2-5 September, 2007, Aalborg.

[5]. S. S. Choi, T. X. Wang, D. Mahinda Vilathgamuwa, "A Series Compensator With Fault Current Limiting Function", IEEE Transactions on Power Delivery, Vol.:20, Issue: 3, July 2005.

[6]. K. Duangkamol, Y. Mitani, K. Tsuji,M. Hojo, "Fault Current Limiting and Power System Stabilization by Static Synchronous Series Compensator", International Conference on Power System Technology, 4-7 December, 2000, Perth.

[7]. S. Polmai, T. Ise, M. Yamada, "Control of Fault Current Limiter by Series-Connected Voltage Sag Compensator", Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 6-11 March, 2011, Fort Worth (USA).

[8]. M. J. Sanjari, A. J. Ghanizadeh, and G.B. Gharehpetian, "Dual functional series compensator to reduce fault current in a distribution system with DG units", International Journal of Engineering, Science and Technology, Vol. 3, No. 11, 2011.

[9]. V. Utkin, J. Guldner, J. Shi, Sliding Mode Control in Electro-mechanical Systems, 2009, Taylor and Francis group, LLC.