Fault tolerant shunt active power filter : topology reconfiguration using optimised fault detection algorithm

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Abstract

This paper proposes a fault tolerant shunt three phase active filter topology. It mainly details converter reconfiguration and examines a fast and reliable optimised fault diagnosis method. This method avoids spurious semi conductor fault detection due to semi conductor switching.

The converter topology is based on classical three-leg active power filter topology but includes bi-directional switches for converter reconfiguration after fault detection. The resulting post fault power structure is a two-leg topology with fault leg connected to the middle point of the filtering capacitor.

A new fault diagnosis method is proposed, based on classical voltage measurements. It includes combinatory logic to analyse and validate error signals. An unique control is applied before and after fault detection, which avoids any controller reconfiguration. Simulation results obtained with Saber CAD tools validate the theoretical study and the modelisation.

Keywords : active power filter, fault tolerant converter topology, fault detection, converter reconfiguration, fault tolerant control

Introduction

The reliability of power electronic equipments becomes extremely important in general in industrial applications. The fault mode behaviour of static converters, protection and fault tolerant control of voltage source inverter systems has been covered in a large number of papers. Most of them are focused on induction motor drive applications.

D. Kastha and B. K. Bose considered various fault modes of a voltage source PWM inverter system for induction motor drive [1]. They have studied rectifier diode short circuit, inverter transistor base driver open and inverter transistor short-circuit conditions. However, they do not propose to reconfigure the inverter topology.

C. Thybo was interested in fault tolerant control of induction motor drive applications using analytical redundancy, providing solutions to most frequent occurring faults [2].

E. R. C. Da Silva and al investigated fault detection of open-switch damage in voltage source PWM motor drive systems [3]. They mainly focused on detection and identification of the power switch in which the fault has occurred. In another paper, they investigated the utilization of a two-leg based topology when one of the inverter legs is lost. Then the machine operates with only two stator windings [4]. They proposed to modify PWM control to allow continuous free operation of the drive.

More recently, E. R. C. Da Silva and al have studied fault tolerant active power filter system [5], [6]. They proposed to reconfigure power converter and PWM control and examined a fault identification algorithm.

This present paper deals with fault tolerant shunt active three-phase filter and mainly details the reconfiguration of the inverter and proposes a robust fault diagnosis method. We study a fast and reliable fault detection algorithm avoiding spurious fault detection due to power semi-conductors switching. More, it

allows to compensate the fault as fast as possible to avoid, after its occurrence, the occurrence of a secondary fault.

First, a fault tolerant inverter based on standard three-phase power structure is presented. Fault diagnosis is detailed. Then, shunt active filter control is presented for three-leg and two-leg structures. The major advantage of this control principle is to be suited if there is fault or not.

Finally, we present simulation results illustrating fault diagnosis and control developed in the present paper.

I.   System description

Fig. 1 presents a classical three-leg shunt active power system. It is composed of a grid (e_{si} for i = {1, 2, 3}), a non-linear load, a voltage source converter. The load is a three-phase diode rectifier feeding a series (R, L) load. The grid is supposed to be balanced with equal series resistances r_s and inductances l_s for each phase. The static converter is a voltage source inverter with equal series resistances r_f and inductances l_f for each phase.
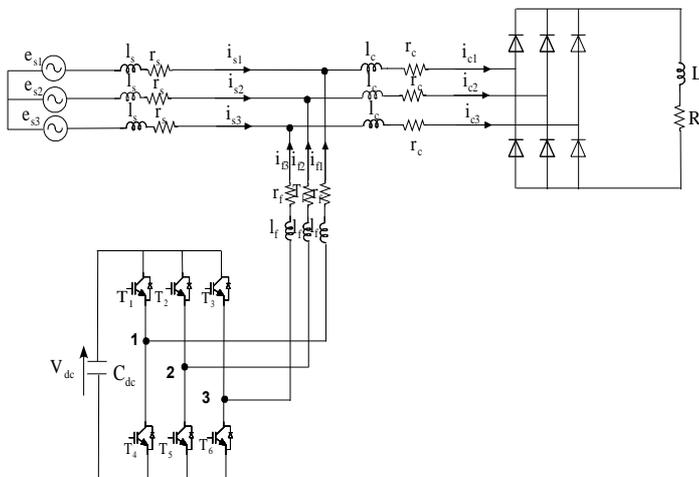

Fig.1 : Classical three-leg shunt active filter topology.

The output currents of the shunt active filter are controlled to provide reactive power and harmonic currents generated by the non-linear load to ensure filtering. The capacitor C_{dc} of the DC filter side is an energy storage capacity. Fig. 2 presents a fault tolerant topology. It is based on standard topology of fig. 1 with power switches T_i (i = {1, .. , 6}) and includes bi-directional devices T_{ri} (i = {1, 2, 3}) (triacs in this case to simplify control) allowing the connection between the grid and the middle

point O of the capacitor C_{dc}. Consequently, triacs allow reconfiguring the inverter module after the fault diagnosis. By this way, for the leg number k, if one of the semi-conductor T_i or its associated switch driver is faulty, the leg including T_i could be isolated and the point k directly connected to the middle point 0 by switching on the triac T_{rk}.
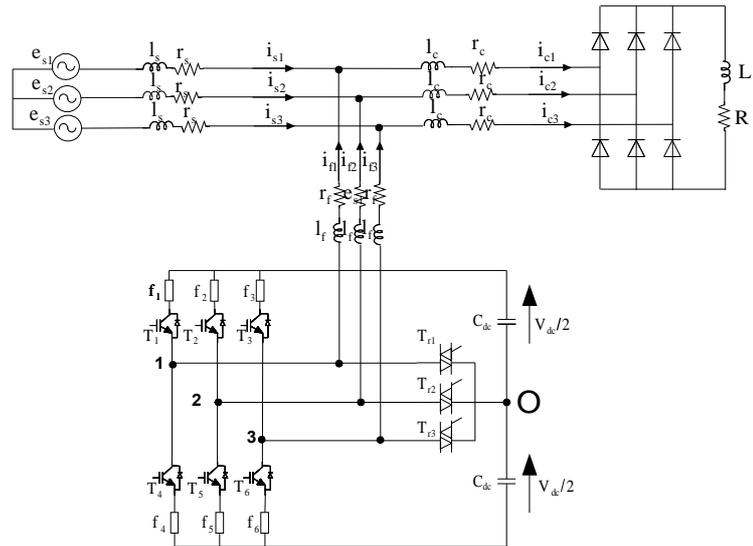

Fig. 2 : Fault tolerant shunt active filter topology with triacs and fuses.

Several faulty cases can occur : power switch or power switch driver can be faulty. In each case, it results in the following models :

- a switch is open instead of being normally closed. It results in an open phase. Only triacs are useful and allow to select the leg to be isolated;

- a switch is closed instead of being normally open. It results in a short-circuit of the capacitor, increasing i_{sk} current and decreasing to zero regulated capacitor voltage v_{dc}. To isolate the faulty switch as fast as possible, one can place 6 isolated devices such as fast active fuses f_i (i = {1, 2, ..,6}) as illustrated in figure 2.

However, using such fuses, only the faulty device will be isolated and the other one on the same leg will be still physically connected. A fault could always occur on this second one, which could cause damage and perturbations if it affects its switching control (semi-conductor closed instead of being open due to switching error). More, the antiparallel diodes (diodes are internal diodes in most of power modules) of the faulty leg are still connected and can perturb the filtering.

Despite of cost considerations, one way of definitively disconnecting the faulty leg consists in using power switches T_{ri} ($i = \{4, 5, 6\}$) instead of the 6 fuses. By including bi-directional devices (triacs in this case to simplify control) one can physically disconnect the faulty leg as presented in fig.3.
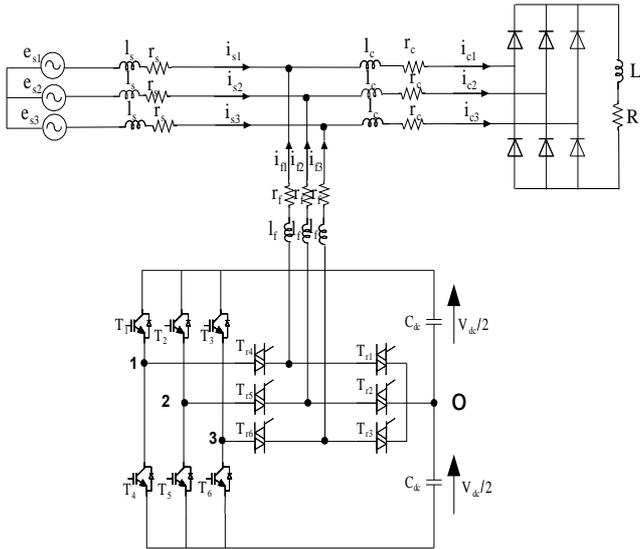

Fig. 3 : Fault tolerant shunt active filter topology with triacs.

In summary, in a fault case on the leg number k, the compensation is achieved by the following steps :

- detection of the faulty switch of the leg number k (detailed in next section);
- removing the commands of the 2 switching drivers of the leg number k;
- disconnect the second device of the leg number k by switching off the suited triac T_{ri} if triacs are used instead of fuses;
- connection of the DC side phase k to the point O of the capacitor energy storage by switching on the suited triac T_{rk};
- applying the suited control strategy.

II. Fault diagnosis method

Fault detection (see Fig. 4) is based on the comparison between measured and estimated V_{kO} voltages for $k = \{1, 2, 3\}$, respectively noted V_{kOm} and V_{kOth}. Voltage V_{kOth} can be expressed as :

$$V_{kOth} = (2.C_k-1).V_{dc}/2$$

with $C_k = \{O, 1\}$ depending on the conducting state of the top semi-conductor of the leg number k.

However, semi-conductors switching disturb measured V_{kOm} voltage. Consequently the error voltage signal defined by $\varepsilon_k = V_{kOm} - V_{kOth}$ for $k = \{1, 2, 3\}$ is constituted of picks induced by each switching on k arm and during about 0.1 μs if IGBTs are used.

To avoid spurious fault detection due to power semi-conductors switching, we think of transforming the "voltage" signal $\varepsilon_k (t)$ in a "time" signal $int_k(t)$. From signal $\varepsilon_k (t)$, we defined the signal $int_k(t)$, constituted of picks having as maximal value the time during which $\varepsilon_k(t)$ is different from zero.
The calculation of $int_k(t)$ is achieved for each phase by first taking the absolute value of $\varepsilon_k(t)$, applying the results to an hysteresis comparator and integrating the comparator output as presented in fig.4. The output of the hysteresis comparator is equal to 0 if $\left|\varepsilon_{k(t)}\right| = 0$ and equal to 1 if $\left|\varepsilon_{k(t)}\right| \neq 0$. The maximal value after integration of this comparator output square signal results in the time during which V_{kOm} and V_{kOth} are different, if integration is initialised to 0 after each square waveform integration. Consequently, we detect the fault using a "time based" fault criterion instead of "voltage based" fault criterion. To do this, we applied signal after integration to a second hysteresis comparator having a band width several times larger than switching time of the semi-conductor. The final result is noted x_k. By this way, we avoid spurious fault detections due to semiconductor switching.
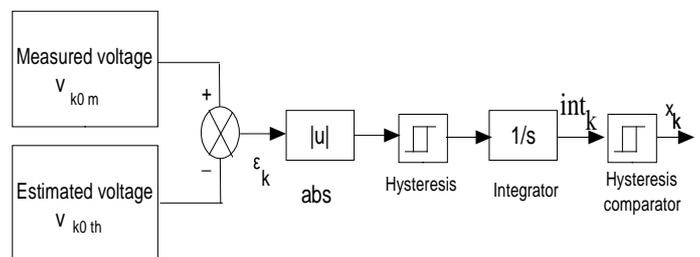

Fig. 4 : Block diagram of the detection algorithm for the phase k.

When a fault is detected in a leg number k, the previous switching control orders C_k and

not(C_k) for the 2 semiconductors of this leg must be set to '0'.

III. Active filter control

Fig. 5 presents a block diagram of the proposed control system. The major advantage of this control principle is to be suited if there is fault or not. Consequently, no control reconfiguration is necessary. The task of this control is to determine the current harmonic references to be generated by the active filter. They are defined using classical active and reactive power method proposed by Akagi [7], associated with 2 filters.
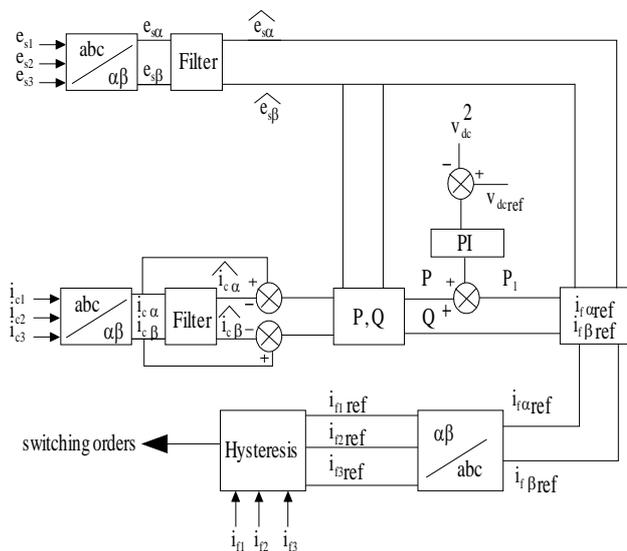

Fig. 5 : block diagram of the control system.

(α, β) voltage components ($e_{s\alpha}$ and $e_{s\beta}$) and currents ($i_{c\alpha}$ and $i_{c\beta}$) are defined by the classical Concordia transformation :

$$\begin{bmatrix} x\alpha \\ x\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x1 \\ x2 \\ x3 \end{bmatrix}$$

The originality of this control is that it extracts the harmonic components directly from the $\alpha\beta$ axis by using "multi-variable" filter, as given by the expressions :

$$\hat{x}\alpha = \frac{k}{s}[x\alpha(s) - \hat{x}\alpha(s)] - \frac{\omega}{s}\hat{x}\beta(s)$$

$$\hat{x}\beta = \frac{k}{s}[x\beta(s) - \hat{x}\beta(s)] + \frac{\omega}{s}\hat{x}\alpha(s)$$

This filter and its principle are detailed in [8]. The powers P and Q are calculated by :

$$P = v_\alpha.i_\alpha + v_\beta.i_\beta$$
$$Q = v_\alpha.i_\beta - v_\beta.i_\alpha$$

Then, (α, β) current references are calculated (see fig. 6) by :

$$i_{f\alpha}^{ref} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2}P1 - \frac{v_\beta}{v_\alpha^2 + v_\beta^2}Q$$

$$i_{f\beta}^{ref} = \frac{v_\beta}{v_\alpha^2 + v_\beta^2}P1 + \frac{v_\alpha}{v_\alpha^2 + v_\beta^2}Q$$

Finally filter current references are defined by :

$$\begin{bmatrix} i_{f1}^{ref} \\ i_{f2}^{ref} \\ i_{f3}^{ref} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{f\alpha}^{ref} \\ i_{f\beta}^{ref} \end{bmatrix}$$

IV. Simulation results

This section presents simulation results obtained with Saber simulator for the proposed fault detection and fault tolerant topology. General simulation parameters are given in appendix 1.

Fig. 6 presents results in an open circuit case (fault of the bottom switch of the leg number 3), introduced at t = 200 ms. The value of the capacitor voltage reference V_{dc}^{ref} is set to 1600V for both before fault three-leg topology and post fault two-leg topology. The value of l_f is 300µH and the hysteresis band is equal to 30A. These parameters are chosen to reduce THD of $i_{sk}(t)$ below 5%. Results presented in fig. 6 show that after fault compensation, the proposed fault tolerant system preserved the main performance features. More, the mean switching frequency remains equal to 8 kHz.
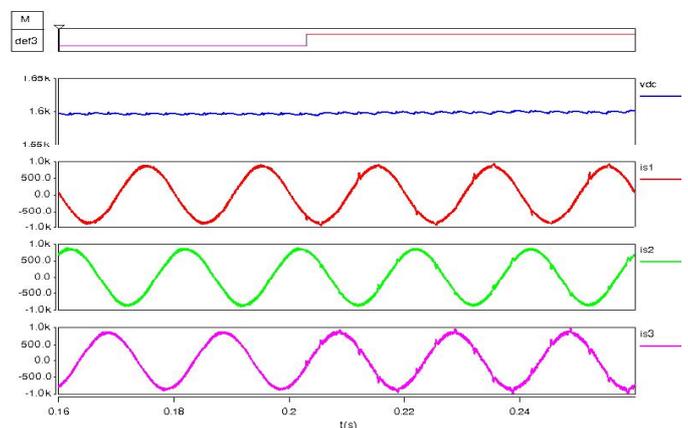

Fig. 6 : case of an open circuit with an unique reference voltage V_{dc}^{ref} =1600 V.
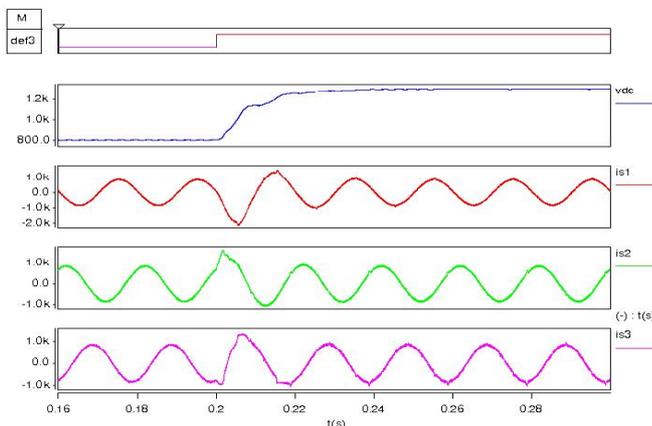
Fig. 7 : case of an open circuit with 2 reference voltages.

Fig. 7 presents results in an open circuit case (fault of the bottom switch of the leg number 3), introduced at t = 200 ms. The value of the capacitor voltage reference V_{dc}^{ref} is set to 800 V for the before fault three-leg topology and set to 1300 V for the post fault two-leg topology. The value of l_f is 150μH and the hysteresis band is equal to 20 A. These parameters are chosen to reduce THD of $i_{sk}(t)$ below 5%. Results presented in fig. 7 show that after fault compensation, the proposed fault tolerant system preserved the main performance features. More, the mean switching frequency is equal to 8 kHz before fault and equal to 8.4 kHz after fault.

V.   Conclusion

In this paper, we presented a fault tolerant active power filter topology and associated fault diagnosis method, control and converter reconfiguration. This fault tolerant system can achieve continuous free operation even if a complete loss of one of the converter legs has happened.
The semi conductor fault detection method is robust to semi conductors switching and includes combinatory logic to perform reliability. The power converter topology can be quickly reconfigured by using bi-directional devices such as triacs to simplify control. By this way, the faulty leg can be isolated and a solution to physically disconnect this leg is proposed.
Simulation results demonstrate that when optimising active filter parameters, the same control strategy can be used in healthy and faulty cases.

Of course, the proposed fault tolerant filter is more expensive than classical structures but it allows to operate for a long time even if a leg is completely lost. The "faulty" mode preserves the main performance features. More, power semi conductors switching frequency remains lower than 10 kHz.

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Appendix : simulation parameters

Grid : 230V, 50 Hz
Non-linear load : R = 0,6 Ω, L = 2,5 mH,
        l_c = 15μH, r_c = 0,4 mΩ
Filtering capacitor : C_f = 17,6 mF