



Shunt Active Power Filter with Selective Harmonics Compensation for LV distribution grid

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Abstract. A Shunt Active Power Filter (SAPF) employable in a Low Voltage distribution grid four-wires model is presented. The use of this device helps to improve Power Quality compensating harmonic currents, reactive power and current unbalances of a disturbing loads. Each compensating function can be activated or disabled according to the specific requirements of the application. A selective harmonic compensation is also possible, in order to avoid possible resonances at specific frequencies. A current hysteresis modulation with predictive calculation of threshold bands achieving fixed switching frequency is adopted for a fast dynamic response. The compensation performance of the proposed active power filter and the associate control scheme under steady state and transient conditions is demonstrated through digital simulations.

Key words

Shunt Active Power Filter, Selective Harmonic Compensation, Power Quality, Predictive Hysteresis Band Current Modulation.

1. Introduction

The number of grid connected electronic loads is continuously increasing during last years. In fact, LED lighting systems, electric vehicles, air-conditioners and many other systems based upon power electronics are gaining popularity. Moreover, electronic loads represent one of the main key point for the implementation of demand-response mechanisms [1].

On one side, electronic loads are disturbing loads injecting harmonics, reactive power and/or flicker into the grid; on the other side, such loads are sensitive to grid disturbances, like voltage unbalances, voltage dips or interruptions. A high level of Power Quality is then needed to assure proper operations of electronic/sensitive loads connected to distribution grids.

Shunt Active Power Filters (SAPF) are an effective solution for improving the Power Quality of distribution grids, that compensate harmonics and reactive power of disturbing loads taking advantage of capability of power electronic converters of generating arbitrary currents.

The paper describes the implementation of a SAPF, to be connected in Low Voltage (LV) distribution grids, close to disturbing or sensitive load. The device is able to compensate harmonic currents, reactive power and current unbalances of a disturbing load and each compensating function can be activated or disabled according to the specific requirements of the application. Also, selective harmonic compensation (SHC) is possible in order to avoid possible resonances at given frequencies. A current hysteresis predictive band modulation is adopted for a fast dynamic response. A predictive algorithm for the dynamic calculation of upper and lower hysteresis limits is adopted as well, for assuring fixed switching frequency in every condition [2] \div [4].

The circuit has been designed for load compensation up to 9 kVA and a simulation model has been implemented within the ATPDraw digital simulation environment. Simulation results, relevant to different operating conditions and typologies of loads, are shown in the paper.

2. The Shunt Active Power Filter

A schematic view of the proposed SAPF circuit topology is reported in Fig. 1.



Fig. 1. Schematic view of the SAPF and of complete system configuration.

The circuit is based on a three-phase bridge with two capacitors on the DC side, C1 and C2, connected in series, so that their central point is available for connecting to the 4th wire and to ground through a small valued resistor. In such a way, zero sequence currents see a complete mesh and unbalanced loads can be compensated. The equivalent DC capacitance has been

chosen in order to maintain the ripple on the DC voltage less than 1.5% of its nominal value, when a single phase load of power equal to 33% of SAPF nominal power is compensated, according to the formula:

$$\Delta V_{CC\%} = \frac{4A_N}{3\pi\omega_0 V_{CCN}^2 C_{CC}} \tag{1}$$

Output filters are designed setting the reactive power they process, as a percentage of the nominal power of the SAPF. The filters resistors are included for damping possible oscillations arising during transients. It has been decided to use a damping factor of χ =0.7, so that the resistor can be designed according to the relation:

$$R_{f,i} = \frac{1}{2\chi} \sqrt{\frac{L_{eq}}{C_{f,i}}} \qquad (2)$$

where i=1,2 and L_{eq} is the total equivalent inductance seen by the filter toward the grid. Adopted design parameters are reported in Table I.

Table I. - SAPF design parameters

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Nominal pwer	A _N	9 kVA	
DC voltage	V _{DC}	600 V	
AC voltage	V _{AC}	214 V	line-to-line
DC capacitors	C _{DC}	9 mF each	C _{eq} 4.5 mF
Inducatnce	L ₁	2.7 mH	$X_{cc} = 16.5\%$
	L ₂	0.48 mH	$X_{cc} = 3\%$
Filter 1 capacitor	C _{f1}	3.14 µF	$Q = 0.5\% A_N,$
Filter 1 resistor	R _{f1}	8.7 Ω	
Filter 2 capacitor	C _{f2}	67.5 μF	$Q = 10.3\% A_N,$
Filter 2 resistor	R _{f2}	3.8 Ω	

The disturbing/sensitive load is connected directly at the output of the SAPF. In the implemented model, a simplified Thévenin equivalent of a LV distribution grid is considered and the load and the SAPF are connected to it through a LV line of length 200 m.

3. SAPF control scheme for Selective Harmonic Compensation

The designed closed control loop of the SAPF has three main objectives:

- maintaining the central point of the DC capacitors at ground level;
- regulating the DC voltage at a reference level;
- compensating load harmonic currents with a Selective Harmonics Compensation strategy (SHC), reactive power and unbalances.

The block scheme of adopted control approach is shown in Fig. 2. The main outputs of the control are three current references, one for each phase, to be passed to the modulator for the generation of the actual SAPF current [5]. As reported in the scheme, the DC capacitor central point voltage is compared to a reference value, namely 0 V, and the result is processed by a Proportional-Integral (PI) regulator with anti-windup. The output regulator directly contributes to the total current reference. The measured DC voltage is compared with a reference value and the resulting error is processed through a PI regulator, whose output is employed, together with Clarke components of grid voltages, to calculate two current references over axes $\alpha\beta$, which are added to other references coming from the control branches which compensate harmonics.





The SHC strategy (green block) has been implemented starting from the measure of the grid currents and comparing the measured values with fixed references, namely 0 A. The resulting errors are transformed for each harmonic order over rotating axis dq by a generalised Park transform, which takes into account also negative sequences, according to the formula:



where k is the harmonic order to be compensated. The results, four signals for each harmonics, are processed through regulators in the form:

$$H_k(s) = \frac{K_{lk}T_k}{1+sT_k} \tag{4}$$

where $K_{Ik} = 2.2/(n_{pk}T_s)$, $T_k = (K_{Ik}A_k)^{-1}$ and $n_{pk}T_s$ is the response time to step change of the regulator input, A_k is the desired attenuation factor for the k-th harmonics and T_k is employed to adjust the DC gain of the regulator.

As reported above, the outputs of regulators (4) are added together, transformed over $\alpha\beta$ axes and added to reference currents coming from the DC voltage regulation branch. Finally, the sum is reported in abc reference and contributes to the total reference current. The SAPF also compensate the reactive power of its own output filters. Also, the load current (blue arrow) is added to the total reference in a feedforward (FFW) compensation scheme. The FFW path assures a fast dynamic response of the SAPF to load changes, but it does not allow the selective compensation of harmonics. For that reason, the FFW can be disabled in case grid resonances may arise, and compensation of harmonics close to resonant frequency are also inhibited.

The regulators have been designed to obtain the following dynamics performances:

- DC voltage regulator response time to step variation: 500 ms;
- Harmonics compensation attenuation:1/100 response time to step variation: 250 ms DC gain: 44. The DC voltage regulation loop has a dynamic slower than the current regulation loop, so that fast variation of load active power can be also compensated.

4. The predictive hysteresis band current modulation

The three current references obtained are compared with the generated inverter currents and these errors, one for each phase, are sent to a modulation stage for the determination of the pattern of turn-ON and turn-OFF commands of the circuit switches.

The proposed modulation is a hysteresis band modulation, for which if one of the current errors hits an upper threshold value the upper switch of the relevant bridge leg is switched OFF, while the lower one is switched ON. In such a way, the SAPF current decreases, until the current error hits a lower threshold limit, where switches status is inverted.

The implemented modulation strategy adapts the calculation of the threshold limits and it links commutations also to a clock signal in order to assure fixed switching frequency and null mean value of the current error over 20 ms (grid voltage period) [6][7]. The hysteresis band limits for the k-th switching period are predictively calculated during the (k-1)-th period, measuring the slope of the current. The final algorithm for the modulation is reported in hereafter and the evolution of SAPF current is shown in Fig. 3:

- 1. If current error hits upper threshold limit: upper switch OFF, lower switch ON;
- 2. If current error hits lower threshold limit: upper switch ON, lower switch OFF;
- 3. Clock rising edge: calculate lower threshold band for the next switching period
 - a. If current error is negative: upper switch ON, lower switch OFF;
 - b. Otherwise: upper switch OFF, lower switch ON;

- 4. Clock falling edge: calculate upper threshold band for the next switching period:
 - a. If current error is positive: upper switch OFF, lower switch ON;

b. Otherwise: upper switch ON, lower switch OFF. The adopted modulation strategy offers the advantages of

• fast dynamic responses to load/reference changes;

• known harmonic content of currents, due to fixed switching frequency.

In the implemented simulation model of the SAPF, the switching frequency was fixed at 12.8 kHz, equivalent to a switching period of 78.125 μ s, which is also the clock frequency, while the upper (lower) threshold limits are bound within the range (-)1.4 A \div (-)4.6 A above (under) the current reference values.



Fig. 3. Visual description of the modulation algorithm and time evolution of SAPF current.

5. Simulation results

A simulation model of the 9 kVA SAPF has been implemented within the ATPDraw digital simulator environment. The model includes all the elements reported in Fig. 1. Also different type of loads have been considered:

- RL three phase model;
- RL single phase model;
- three phase diode rectifier bridge.

Performed simulations cover steady state compensation of all kinds of load and transient behaviours, f.i. load connection and disconnection, the behaviour of the active filter in case of unbalanced supply grid voltages and in presence of capacitive load and resonances.

A. Compensation of a three phase RL load

The load is represented as a three phase RL circuit, connected in series. Since the load is linear, no harmonic currents should be compensated; the inductive component of the load would require an amount of reactive power from the grid, that should be compensated by the SAPF. Load parameters are a total apparent power of 7.742 kVA, a power factor of 0.9 (active power 6.96 kW and reactive power 3.39 kVAr). The active and reactive powers of the load, of the SAPF and the one supplied by the grid are shown in Fig. 4; in particular it has been evaluated the

transient occurring during connection of this kind of load (t = 0.3 s). After the initial transient, SAPF compensates only the reactive power of the load, while the active power is supplied by the grid. The residual reactive power supplied by the grid is due to the partial compensation of the reactive power of SAPF, since the regulators present finite DC gain. SAPF output current, for one phase only, is shown in Fig. 5, together with the reference and the hysteresis bands.



Fig. 4. Active and reactive power - compensation of linear load reactive power.



B. Compensation of a single phase RL load

In this case the single phase RL load is connected to phase "c". Load parameters are the same as in the previous case ($R_{load} = 5.33 \ \Omega$, $L_{load} = 8.27 \ mH$), but the SAPF should take into account current unbalances, so it should supply both the reactive power and the oscillating component of the active power of the load. Simulation results are given in Fig. 7. As explained before, part of the reactive power of SAPF output filter is not compensated. Residual oscillations of grid supplied active power have amplitude 1.3% of the load oscillations amplitude.

The DC voltage of the SAPF is shown in Fig. 8. In this case, the amplitude of the 100 Hz oscillations on the DC voltage is below 1% of the nominal voltage level (600 V). In Fig. 6 the grid and single phase load currents (with an offset to see better the waveforms) are shown, thanks to the SAPF compensation the grid current are symmetric.



Fig. 7. SAPF compensation of a single-phase RL load. a) reactive powers, b) active powers.



Fig. 8. DC voltage of SAPF during compensation of a single-phase load.



Fig. 8. Grid currents (grey, brown and magenta) and single phase load currents (blu, green=0, red=0) with SAPF during compensation of a single-phase load.

C. Compensation of a diode bridge rectifier load

A three-phase diode bridge rectifier has been considered as a disturbing load. The rectifier has also input inductances on the AC side, so that it absorbs active and reactive power (8 kVA; 7.5 kW; 2.5 kVAr) and harmonic components. The connection transient of the diode bridge rectifier starts at time t = 0,32 s: the SAPF is able to fully compensate the load harmonic currents within 4 grid cycles (80 ms), as shown in Fig. 9, while reactive power compensation is nearly instantaneous, Fig. 10.



Fig. 9. Compensation of load harmonic currents (phase "a") during the connection of a disturbing load.



Fig. 10. Compensation of reactive power during the connection of a disturbing load.

Load, SAPF and resulting grid currents are shown in Fig. 11 (only phase "a" currents are shown for simplicity). In Fig. 12 the amplitude of the harmonic spectra of load and grid currents are shown. Even though the FFW compensation of load currents tends to compensate every currents harmonics, only regulators for odd harmonics were activated in the control. The Total Harmonic Distortion (THD) of the load current is 26.67%, while the grid current THD is reduced to 1%.



Fig. 11. Compensation of harmonic currents of a distorting load (phase "a").



D. Behaviour in case of unbalanced supply grid voltages In presence of a disturbing load, as the one considered before, it's interesting to evaluate the capability of the active filter to compensate also in presence of unbalanced supply grid voltages. As the SAPF is a shunt device it can't compensate network voltage unbalance due to network poor quality even if it has to assure, also in this operational condition, the mitigation of the effect of the disturbing load in the grid currents. The hypothesis is to have supply voltages with an unbalance of 2% (Fig. 13).



Fig. 14 shows the simulation results and it's possible to confirm the SAPF compensation effect: the THD of the load is 26.67%, while the residual grid current has a THD of 1.26%, to be compared to the result reported in §5C.



Fig. 14. Load, grid and SAPF currents (phase "a") with unbalanced supply grid voltages.

E. Behaviour in case of grid resonances

To complete the characterization of the SAPF it has been evaluated what happens if there is a possible resonance in the grid in particular in presence of capacitive loads (in particular in the simulations a capacitive load of 5% A_{SAPF} has been considered). At t = 0.6 s the capacitive load is connected to the grid in parallel to the SAPF and to the diode bridge rectifier load described in section 5C. Both the solutions with and without the FFW components (blu and red arrows in Fig. 2) have been considered for the control of the SAPF.

<u>Closed loop control without current harmonic selection</u>

Considering the FFW contribution in the control scheme in Fig. 2 (red and blue arrows) the device is very fast but the selective harmonic compensation is not guaranteed. In fact, in Fig. 15 (where the grid, load and SAPF currents are shown) it's clear that before the capacitve load connection the system is able to compensate the diode bridge rectifier load but after t = 0.6 s there is an effect of high frequency components. This phenomenon is related to the fact that the capacitive load causes, with the grid impedance, an high frequency resonance (around the 60th harmonic order) that is supplied by the active filter (without selection of the harmonics) as shown in Fig. 16. Considering the grid current THD before and after the capacitive load it increases from 1% to 23.4%.



Fig. 15. Load, grid and SAPF currents (phase "a") during the connection of a capacitive load without selective harmonic compensation.



Fig. 16. Grid current spectrum before and after the capacitive load connection (phase "a") without selective harmonic compensation.

Closed loop control with current harmonic selection

In this case the SAPF is controlled with the closed control scheme in Fig. 2 without the FFW components (red and blue arrows) and it is settled to compensate the load characteristic harmonics (5^{th} , 7^{th} , 11^{th} , 13^{th} , 17^{th} and 19^{th}). The grid currents present the same waveform before and after the capacitive load connection (Fig. 17). Also the THD value remain quite the same, rising from $3.7\%^1$ to 4%.



Fig. 17. Load, SAPF and grid currents (phase "a") during the connection of a capacitive load with selective harmonic compensation.

6. Conclusions

The paper presents the performances of a 9 kW Shunt Active Power Filter (SAPF) for the improvement of

Power Quality and for power factor correction for disturbing or sensitive loads. The proposed SAPF acts as a controlled current generator, whose reference current is nominally equal to the disturbing components of load currents. The adopted control approach allows obtaining fast dynamic responses to load changes, but it can be modified to obtain selective harmonics compensation, at the cost of slower dynamics. The proposed modulation strategy is an hysteresis band current control, modified so that in each switching period the current threshold limits are predicted for the following period in order to guarantee fixed switching frequency. Such a modulation allows very fast responses to reference changes while assuring a "defined" harmonic spectrum of the SAPF currents. The SAPF behaviour has been simulated for different kinds of load: three-phase RL balanced, singlephase RL and three-phase diode bridge rectifier, both at the steady state and transient conditions and in case of unbalanced supply voltages. In each case, the SAPF reached a good degree of compensation of disturbing current components of the load, with fast dynamic responses to rapid load changes. Also, the system response to possible grid and load resonances has been analysed through simulations. In this case, it emerged that a possible control strategy for the SAPF is to disable the direct compensation of load currents (FFW) and to suitably select the harmonics to be compensated.

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¹ The THD value with disturbing load is worst than in the case with the FFW (1%) due to the finite DC gain of the regulators ("REG" in Fig.2).