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Development of 8 MVA class Power Stack for Offshore Wind Power Conversion

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Abstract. Offshore wind power generation is one of the viable solutions for the safety of energy consumption, and the growing concerns for environmental protection and the petroleum crisis. The advantages of wind power generation which are comparatively stable wind speed in the sea, fewer developing interest relative sides, and non-trying for land with other projects, large scale of offshore wind farm building becomes a new trend for wind power industry. Offshore wind power can becomes a viable alternative only if that is able to meet certain reliability, performance, and cost criteria. In this paper, the authors developed and evaluated power stack by considering their influence on the performance. The evaluations is demonstrated experimentally.

Key words

Wind power, Multi-level converter, Neutral Point Clamped (NPC) converter, Power stack.

1. Introduction

Over the last decade, there has been a growing interest in renewable energy. As one of the renewable energy resources, wind power is attracting considerable attention and becoming most developing renewable energy resources. Especially, offshore wind power generation system can generate higher power than onshore wind power generator system due to stronger wind and stable. The size of windmill has been also increasing from the economical point of view. In order to develop and evaluate the power stack in the laboratory, a 8MVA class power stack and experimental platform were developed. The power stack and experimental platform includes: 3-level IGBTs, liquid cooled heat sink, bus-bar, 3-level gate driver, PWM controller, etc.
This paper deals with development of each part for 8MVA class power stack. This paper also reports the features of power stack with the results of a full power test obtained by 3-level experimental platform which is developed.

2. Development of Power Stack

A. Three Level Converter

It is hard to connect a single power semiconductor switch directly to medium voltage grid (3.3kV). For this reason, multilevel converters has emerged as the solution for working with higher voltage levels [1]-[4].

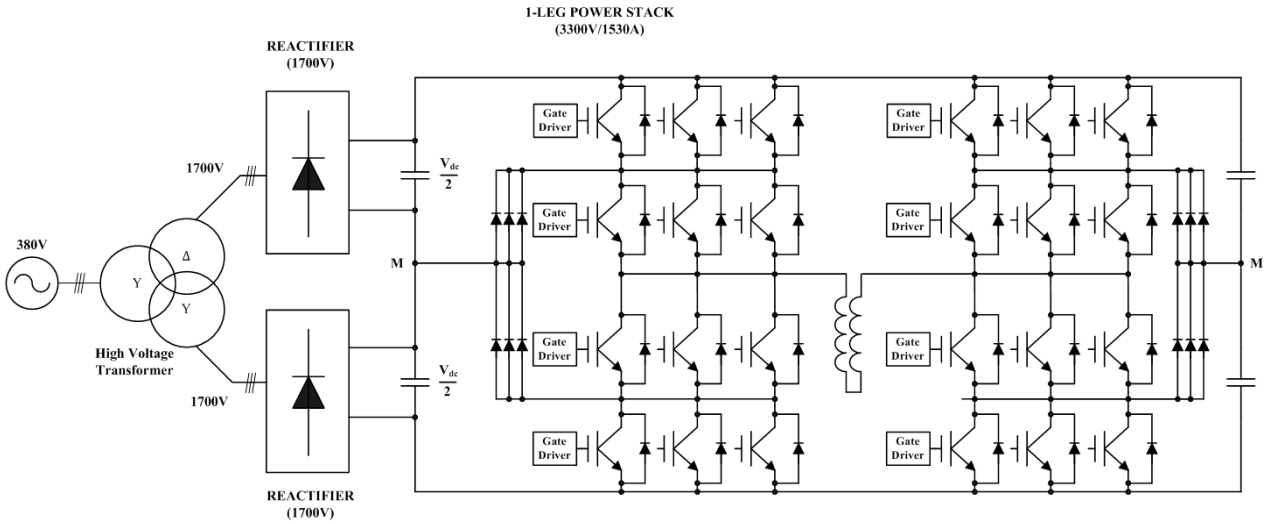


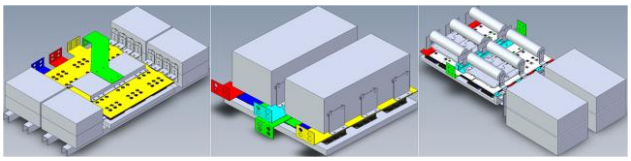
Fig. 1. Overall structure for the power stack test

Multilevel converters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only phase leg of converters with different numbers of levels, for which the action of the power semiconductor is represented by an ideal switch with several positions. A two-level converter generates an output voltage with two levels with respect to the negative terminal of capacitor, while the three-level converter generates three voltages [4]. In this paper, we applied the most popular structure, the diode-clamped converter based on the neutral point converter with SVPWM technique.

As shown in Fig. 1, each leg in three-level converter is constituted by four controllable switches with two clamping diodes. Two equal capacitors splits the DC bus voltage into three voltage levels. Clamping diodes blocks the reverse voltage of the capacitor and provide connection to the neutral point.

B. Design of Power Stack

The converter power stack was designed in consideration of the electrical characteristics, the environment at the place of installation and assembly performance. The power stack is designed three types as shown in the Fig. 2.



(a) Design 1 (b) Design 2 (c) Design 3

Fig. 2. Design of power stack

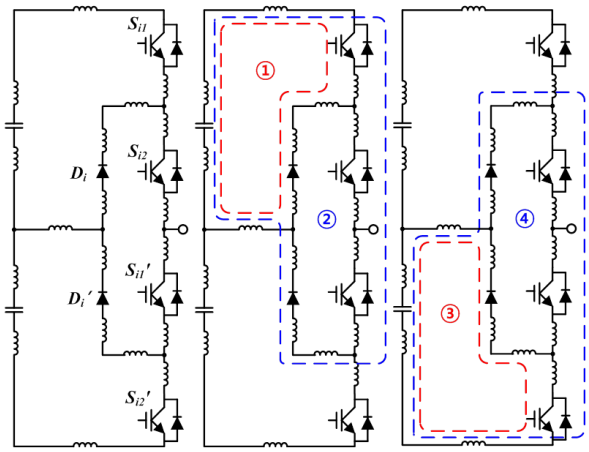
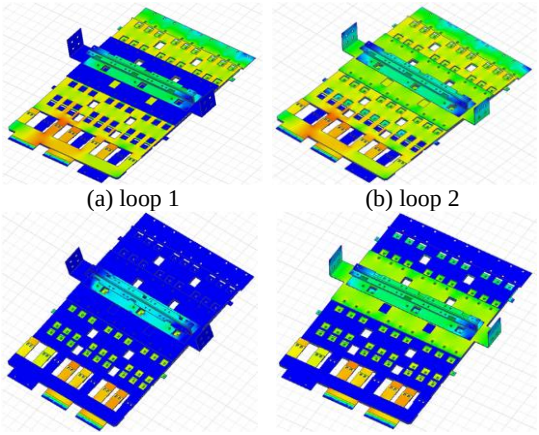


Fig. 3. Commutation loop

Among those designs, design 3 was selected because the design 3 has the advantages which is easy installation and assembly. It is possible to simplify the structure due to the weight distribution and easy assembly. However, this structure has disadvantage in the surge voltage because the length between main capacitor and power switch is long. Therefore it is important to minimize the surge voltage. To minimize the surge voltage, the analysis was performed with the parasitic inductance of commutation loop in the bus-plate. The simulation was used for Q3D and the results of the parasitic inductance in the commutation loop are shown in the Fig. 3 and the Table I. In case that di/dt of the power module maintains below 2,000 A/us, the surge voltage was reduced to less than 350 V in the simulation of the parasitic inductance and current density.



(a) loop 1 (b) loop 2

(c) loop 3 (d) loop 4

Fig. 4. Current density of bus-plate

Table I. - BUS-plate inductance

Loop	Bus-plate inductance (nH)	Power module inductance (nH)	Total inductance (nH)
1	75.3	30	105.3
2	78.5	60	123.3
3	67.4	30	97.4
4	72.5	60	132.5

C. *Gate Drive*

The Gate drive was implemented by using CPLD. The gate drive is composed of a CPLD logic, PWM generation, di/dt protection, and protection logic using saturation voltage. Fig. 5 shows the gate drive block-diagram. soft turn-on and soft turn off logic was implemented using variable resistors. Fig. 6 shows waveforms at normal condition and fault condition. At normal condition, PWM output was operated well. When the fault occurs, the PWM output was blocked immediately.

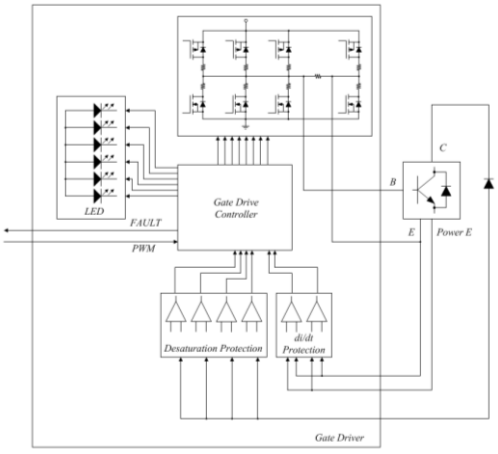
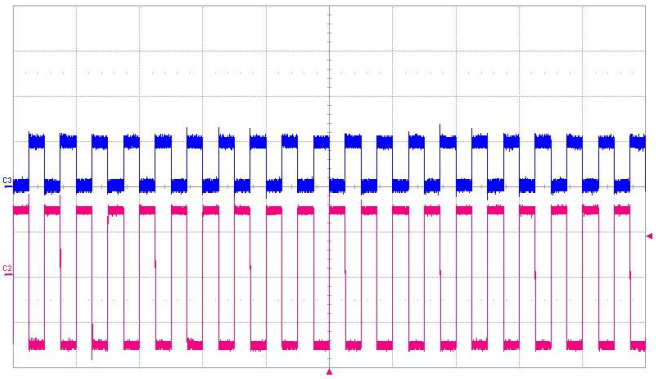
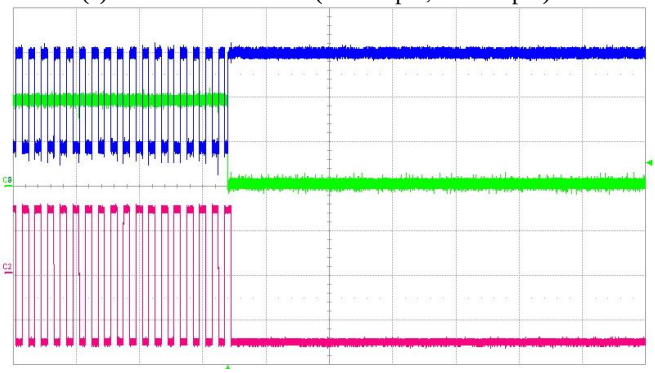


Fig. 5. Gate drive block-diagram



(a) At normal condition (blue: input, red: output)



(b) At fault condition (blue: input, green: fault, red: output)

Fig.6. waveforms at normal and fault condition

In order to test the gate drive, the Gate drive pulse tester was fabricated. Fig. 7 shows the DC chopper for gate drive test. The switches S_2, S_3 are for the 1-arm of the chopper. The switch S_1 is for system protection. By using this tester, it is possible to perform the switching logic test and the arm short test. Fig.9 shows the test results. The switching of the IGBT was performed well. At dc-link voltage 2,500V, the maximum current was 1,300A.

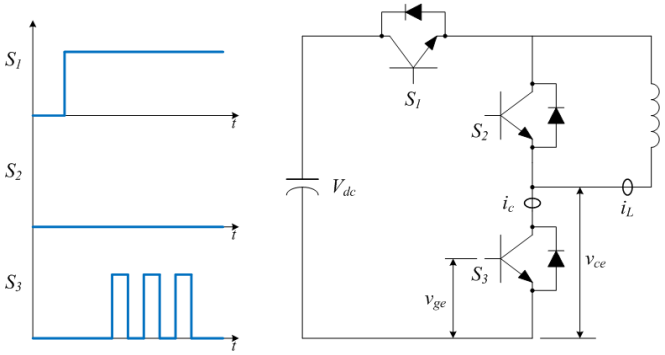


Fig. 7. DC chopper for gate drive test

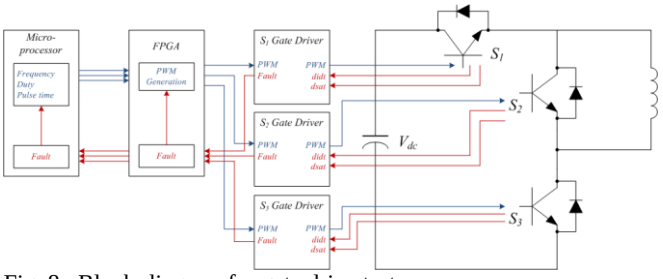


Fig. 8. Block-diagram for gate drive test

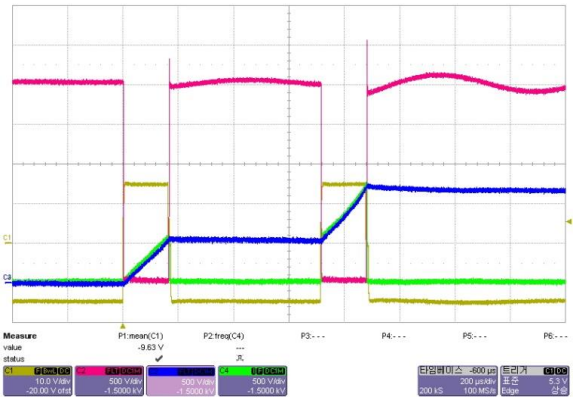


Fig. 9. Waveforms of gate drive test
(Red:V_{CE}, Blue: I_{load}, Green: I_{igbt}, Yellow: V_{BE})

3. Experimental Results

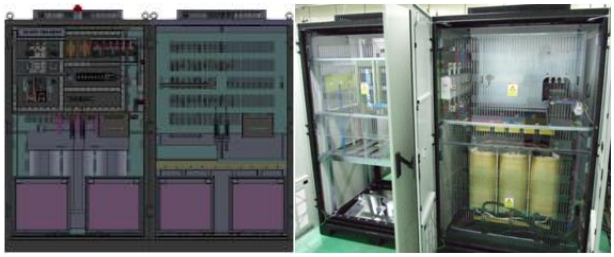


Fig. 10. 3D drawing and picture of power supply and reactor

Table II. - Specification of power supply

	Specification
Input voltage	380V(±10), 3Φ
Output voltage	DC 2,500~6,000V
Output Power	200kVA
Cooling	Forced air cooling

In order to test the developed power stack, the high voltage power supply and the reactor for the load were fabricated. Table II shows the specification and Fig. 10 shows 3D drawing and picture of the power supply and the reactor.

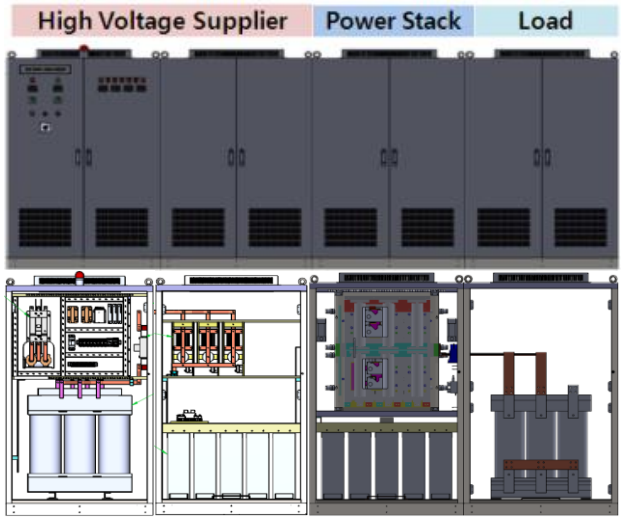
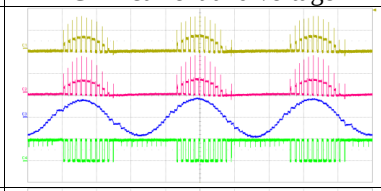
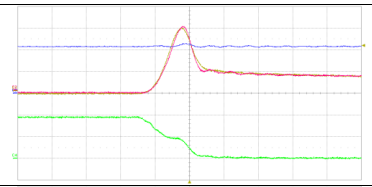
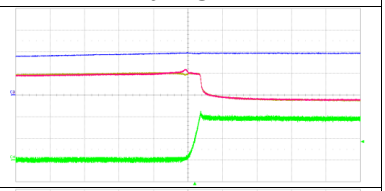
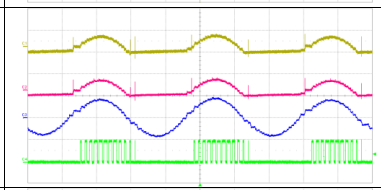
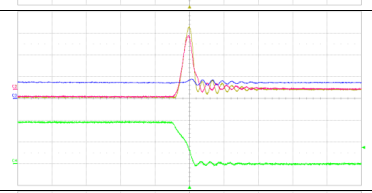
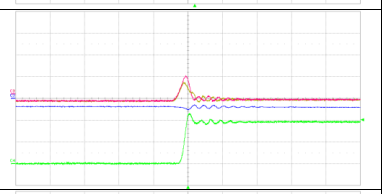
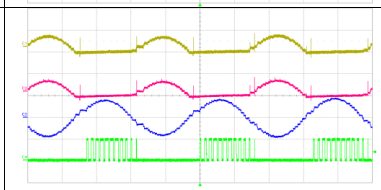
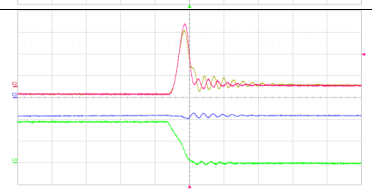
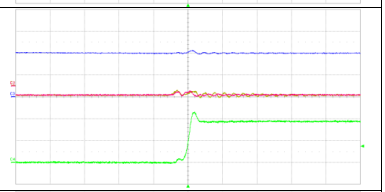
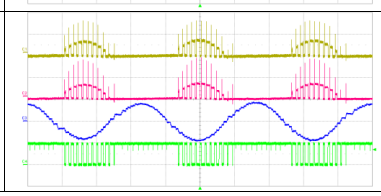
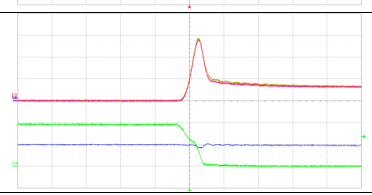
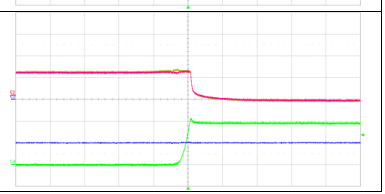


Fig. 11. 3D drawing and picture of whole system

The prototype 1-leg power stack which is 3.3kV and 7MW class was fabricated. Fig. 11 shows the 3D drawing of the whole system.

Table III. - Distributed current test for parallel IGBT

	IGBT current and voltage	Turn-ON	Turn-OFF
IGBT 1			
IGBT 2			
IGBT 3			
IGBT 4			

The power stack was tested by using the reactor load for the performance evaluation. Fig. 12 shows phase current and phase voltage at the maximum point. The maximum current was 1,530A_{rms}. Green waveform is phase voltage 1kV/div and blue waveform is phase current 1kA/div.

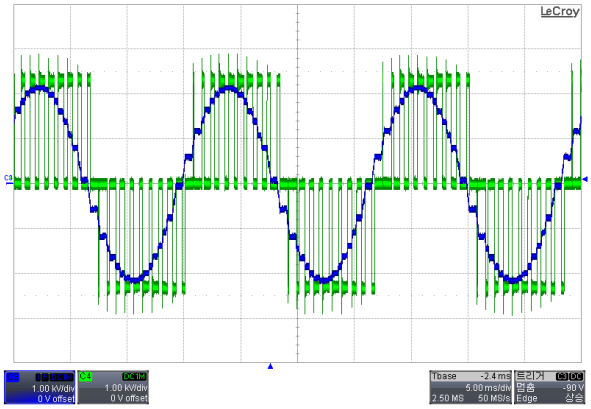


Fig. 12. Waveforms at DC-link 5,200V

4. Conclusion

This paper presents an experimental evaluation of 8MVA class power stack for wind power generation. For the evaluation, the power stack, the converter test system and cooling system are developed. In order to operate the converter system, three level PWM method and NPC converter topology were applied. The power stack was successfully operated at the maximum point where DC-link voltage is 5.2kV and peak phase current is approximately 2.2kA. And surge voltage was lowered. From the experimental results, the power stack was operated well. The converter system has been successfully implemented.

Acknowledgement

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References

[1] J. S. Lai and F. Z. Peng, “Multilevel converters–A new breed of power converters,” *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 509–517, 1996.

[2] L. Tolbert, F.-Z. Peng, and T. Habetler, “Multilevel converters for large electric drives,” *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 36–44, 1999.

[3] R. Teodorescu, F. Beaabjerg, J. K. Pedersen, E. Cengelci, S. Sulistijo, B. Woo, and P. Enjeti, “Multilevel converters — A survey,” *European Power Electronics Conf. (EPE’99)*, Lausanne, Switzerland, 1999.

[4] J. Rodriguez, J.S. Lai, F.Z. Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications," *IEEE Trans. Ind. Elec.*, vol. 49, pp.724-738. 2002.

[5] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point clamped PWM inverter,” *IEEE Trans. Ind. Applicat.*, vol. IA-17, pp. 518–523, 1981.

[6] T. A. Meynard and H. Foch, “Multi-level choppers for high voltage applications," *Eur. Power Electron. Drives J.*, vol. 2, no. 1, p. 41, 1992.

[7] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, “Comparison of multilevel inverters for static var compensation,” in *Conf. Rec. IEEE-IAS Annu. Meeting*, pp. 921–928, 1994.

[8] P. Hammond, “A new approach to enhance power quality for medium voltage ac drives,” *IEEE Trans. Ind. Applicat.*, vol. 33, pp. 202–208, 1997.

[9] E. Cengelci, S. U. Sulistijo, B. O. Woom, P. Enjeti, R. Teodorescu, and F. Blaabjerge, “A new medium voltage PWM inverter topology for adjustable speed drives,” in *Conf. Rec. IEEE-IAS Annu. Meeting*, St. Louis, MO, pp. 1416–1423, 1998.